DS92LV040A 4 通道总线 LVDS 收发器

1 特性

- 总线 LVDS 信令
- 传播延迟：驱动器最大值为 2.3 ns，接收器最大值为 3.2 ns
- 低功耗 CMOS 设计
- 驱动器 100% 转换时间典型值为 1 ns，接收器典型值为 1.3 ns
- 高信号传输速率功能（155 Mbps 以上）
- V_{ID} 0.1 V 至 2.3 V 共模范围 = 200 mV
- 70 mV 接收器灵敏度
- 支持打开和终止端口引脚故障保护
- 3.3 V 运行电压
- 无毛刺加电/断电（已禁用驱动器和接收器）
- 每总线 LVDS 负载的轻型总线负载（典型值 5 pF）
- 平衡输出阻抗
- 44 引脚 WQFN 封装中提供的产品
- 断电时高阻抗总线引脚 (V_{CC} = 0 V)

2 应用

专为双终端设计 应用

3 说明

DS92LV040A 属于总线 LVDS 收发器系列产品，专用于高速、低功耗背板或电缆接口。器件由 3.3 V 单电源供电运行，并包括四个差动线路驱动器和四个接收器。要将总线负载降至最低，驱动器输出端和接收器输入端需进行内部连接。此外，该器件还具备 一只 直通式外引脚，以支持短接线柱在其引脚和连接器之间轻松实现 PCB 路由。

驱动器可将 3 V LVTTL 电平（单端）转换为差动总线 LVDS (BLVDS) 输出电平。该功能可以在支持高速运行的同时将功耗降至最低并降低 EMI。此外，该差动信令可提供大于 ±1 V 的共模噪声抑制。

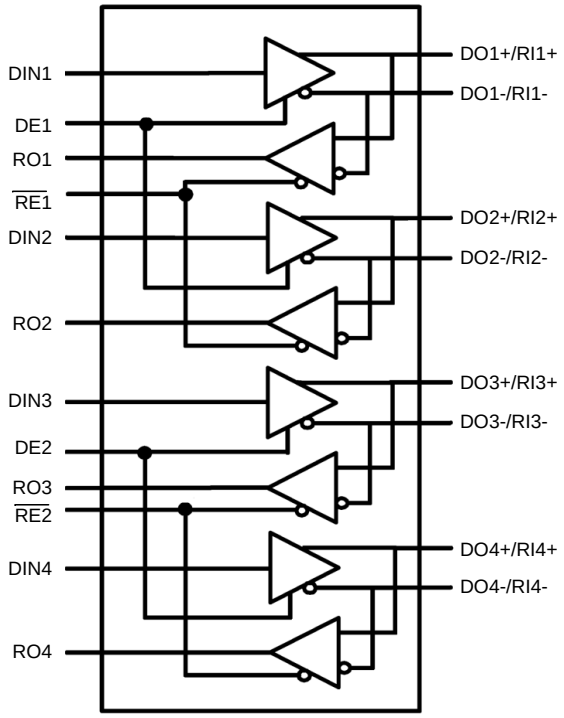
接收器阈值小于 +0/70 mV。接收器可将差动总线 LVDS 转换为标准 (LVTTL/LVCMOS) 电平。（请参阅 *应用信息* 部分了解详细信息。）

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DS92LV040A	WQFN (44)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化功能图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (April 2013) to Revision E **Page**

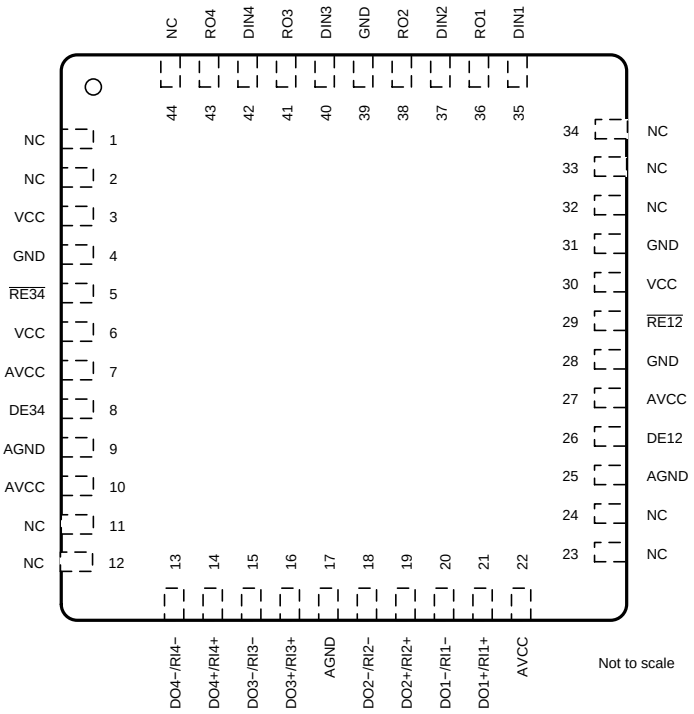
- 添加了*器件信息表*、*ESD 额定值表*、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1
- Added "Driver Short Circuit Current Duration" to the *Absolute Maximum Ratings* ... 4
- Deleted Note 4: "Only one output at a time should be shorted..." from the *DC Electrical Characteristics* table ... 5

Changes from Revision C (April 2013) to Revision D **Page**

- Changed layout of National Data Sheet to TI format ... 3

5 Pin Configuration and Functions

NJN Package
WQFN (44 Pin)
Top View



Pin Functions

PIN NAME	PIN #	INPUT/ OUTPUT	DESCRIPTIONS
DO+/RI+	14, 16, 19, 21	I/O	True Bus LVDS Driver Outputs and Receiver Inputs.
DO−/RI−	13, 15, 18, 20	I/O	Complimentary Bus LVDS Driver Outputs and Receiver Inputs.
D_{IN}	35, 37, 40, 42	I	LVTTL Driver Input. No pull up or pull down is attached to this pin
RO	36, 38, 41, 43	O	LVTTL Receiver Output.
$\overline{RE12}$	29	I	Receiver Enable LVTTL Input (Active Low). This pin, when low, configures receiver outputs, RO1 and RO2 active. When this pin is high, RO1 and RO2 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes RO1 and RO2 to be TRI-STATE
$\overline{RE34}$	5	I	Receiver Enable LVTTL Input (Active Low). This pin, when low, configures receiver outputs, RO3 and RO4 active. When this pin is high, RO3 and RO4 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes RO3 and RO4 to be TRI-STATE
DE12	26	I	Driver Enable LVTTL Input (Active High). This pin, when high, configures driver outputs, DO1+/RIN1+, DO1−/RIN1− and DO2+/RIN2+, DO2−/RIN2− active. When this pin is low, driver outputs 1 and 2 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes driver outputs 1 and 2 to be active
DE34	8	I	Driver Enable LVTTL Input (Active High). This pin, when high, configures driver outputs, DO3+/RIN3+, DO3−/RIN3− and DO4+/RIN4+, DO4−/RIN4− active. When this pin is low, driver outputs 3 and 4 are TRI-STATE. If this pin is floating, a weak current source to V_{CC} causes driver outputs 3 and 4 to be active
GND	4, 28, 31, 39	Ground	Ground for digital circuitry (must connect to GND on PC board). These pins connected internally.
V_{CC}	3, 6, 30	Power	V_{CC} for digital circuitry (must connect to V_{CC} on PC board). These pins connected internally.
AGND	9, 17, 25	Ground	Ground for analog circuitry (must connect to GND on PC board). These pins connected internally.
AV_{CC}	7, 10, 22, 27	Power	Analog V_{CC} (must connect to V_{CC} on PC board). These pins connected internally.
NC	1, 2, 11, 12, 23, 24, 32, 33, 34, 44	N/A	Reserved for future use, leave open circuit.
DAP		GND	Must connect to GND plane through vias to achieve the theta ja specified under Absolute Maximum Ratings. The DAP (die attach pad) is the heat transfer material that is centered on the bottom of the WQFN package. Refer to application note AN-1187 () for attachment details.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)ccr(3)

	MIN	MAX	UNIT
Supply Voltage, V_{CC}		4	V
Enable Input Voltage (DE, $\overline{RE}$)	−0.3	V_{CC} +0.3 V	V
Driver Input Voltage (D_{IN})	−0.3	V_{CC} +0.3 V	V
Driver Short Circuit Current Duration	Continuous		
Receiver Output Voltage (R_{OUT})	−0.3	V_{CC} +0.3 V	V
Bus Pin Voltage (DO±/RI±)	−0.3	3.9	V
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)(2)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(3)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(4)	±1000	

(1) All typicals are given for V_{CC} = +3.3 V and T_A = +25°C, unless otherwise stated.
(2) ESD Rating: HBM (1.5 kΩ, 100 pF) > 4 kV EIAJ (0 Ω, 200 pF) > 250.
(3) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(4) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply Voltage		3		3.6	V
	Receiver Input Voltage		0		2.4	V
T_A	Ambient Free Air Temperature		−40		85	°C
	Slowest Input Edge Rate, $\Delta t/\Delta V$ (20% to 80%)(1)	Data			1	ns/V
		Control			3	ns/V

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, Z_O = 50 Ω, t_r, t_f = <1 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1 ns/V; control signals equal to or faster than 3 ns/V. In general, the faster the input edge rate, the better the AC performance.

6.4 Thermal Information

THERMAL METRIC(1)		DS92LV040A NJN (WQFN) 44 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Package must be mounted to pc board in accordance with AN-1187 (SNOA401) to achieve thermals.

6.5 DC Electrical Characteristics(1)

Over recommended operating supply voltage and temperature ranges unless otherwise specified.(2)(3)

PARAMETER		TEST CONDITIONS		PIN	MIN	TYP	MAX	UNIT
V_{OD}	Output Differential Voltage	R_L = 27Ω, 图 1		DO+/RI+, DO−/RI−	200	300	460	mV
ΔV_{OD}	V_{OD} Magnitude Change					5	27	mV
V_{OS}	Offset Voltage				1.1	1.3	1.5	V
ΔV_{OS}	Offset Magnitude Change					5	10	mV
V_{OHD}	Driver Output High Voltage	R_L = 27Ω				1.4	1.65	V
V_{OLD}	Driver Output Low Voltage	R_L = 27Ω			0.95	1.1		V
I_{OSD}	Driver Output Short Circuit Current	V_{OD} = 0V, DE = V_{CC}, Driver outputs shorted together				|30|	| 45|	mA
V_{OHR}	Receiver Voltage Output High(4)	V_{ID} = +300 mV	I_{OH} = −4 mA	R_{OUT}	V_{CC}−0.2			V
		Inputs Open			V_{CC}−0.2			V
		Inputs Terminated, R_L = 27Ω			V_{CC}−0.2			V
V_{OLR}	Receiver Voltage Output Low	I_{OL} = 4.0 mA, V_{ID} = −300 mV				0.05	0.100	V
I_{OD}	Receiver Output Dynamic Current	V_{ID} = 300mV, V_{OUT} = V_{CC}−1.0V			−50	|33|		mA
		V_{ID} = −300mV, V_{OUT} = 1.0V				|36|	60	mA
V_{TH}	Input Threshold High(5)	DE = 0V, Over common mode range		DO+/RI+, DO−/RI−		−40	0	mV
V_{TL}	Input Threshold Low(5)				−70	−40		mV
V_{CMR}	Receiver Common Mode Range				$\|V_{ID}\|/2$		2.4 − $\|V_{ID}\|/2$	V
I_{IN}	Input Current	DE = 0V, $\overline{RE}$ = 2.4V, V_{IN} = +2.4V or 0V			−20	±1	+20	µA
		V_{CC} = 0V, V_{IN} = +2.4V or 0V			−20	±1	+20	µA
V_{IH}	Minimum Input High Voltage			D_{IN}, DE, $\overline{RE}$	2.0		V_{CC}	V
V_{IL}	Maximum Input Low Voltage				GND		0.8	V
I_{IH}	Input High Current	V_{IN} = V_{CC} or 2.4V			−20	±2.5	+20	µA
I_{IL}	Input Low Current	V_{IN} = GND or 0.4V			−20	±2.5	+20	µA
V_{CL}	Input Diode Clamp Voltage	I_{CLAMP} = −18 mA			−1.5	−0.8		V
I_{CCD}	Power Supply Current Drivers Enabled, Receivers Disabled	No Load, DE = $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND		V_{CC}		20	40	mA
I_{CCR}	Power Supply Current Drivers Disabled, Receivers Enabled	DE = $\overline{RE}$ = 0V, V_{ID} = ±300mV				27	40	mA
I_{CCZ}	Power Supply Current, Drivers and Receivers TRI-STATE	DE = 0V; $\overline{RE}$ = V_{CC}, DIN = V_{CC} or GND				28	40	mA
I_{CC}	Power Supply Current, Drivers and Receivers Enabled	DE = V_{CC}; $\overline{RE}$ = 0V, DIN = V_{CC} or GND, R_L = 27Ω				70	100	mA
I_{OFF}	Power Off Leakage Current	V_{CC} = 0V or OPEN, D_{IN}, DE, $\overline{RE}$ = 0V or OPEN, $V_{APPLIED}$ = 3.6V (Port Pins)		DO+/RI+, DO−/RI−	−20		+20	µA
C_{OUTPUT}	Capacitance at Bus Pins			DO+/RI+, DO−/RI−		5		pF
c_{OUTPUT}	Capacitance at R_{OUT}			R_{OUT}		5		pF

(1) The DS92LV040A functions within datasheet specification when a resistive load is applied to the driver outputs.
(2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified except V_{OD}, ΔV_{OD} and V_{ID}.
(3) All typicals are given for V_{CC} = +3.3 V and T_A = +25°C, unless otherwise stated.
(4) V_{OH} fail-safe terminated test performed with 27 Ω connected between RI+ and RI− inputs. No external voltage is applied.
(5) Propagation delays, transition times, and receiver threshold are ensured by design and characterization.

6.6 AC Electrical Characteristics

Over recommended operating supply voltage and temperature ranges unless otherwise specified.(1)

PARAMETER		TEST CONDITIONS(2)	MIN	TYP	MAX	UNIT
DIFFERENTIAL DRIVER TIMING REQUIREMENTS						
t_{PHLD}	Differential Prop. Delay High to Low(3)	R_L = 27Ω, 图 2, 图 3, C_L = 10 pF	1	1.5	2.3	ns
t_{PLHD}	Differential Prop. Delay Low to High(3)		1	1.5	2.3	ns
t_{SKD1}	Differential Skew $\|t_{PHLD}–t_{PLHD}\|$ (duty cycle)(4) (3)			80	160	ps
t_{CCSK}	Channel to Channel Skew (all 4 channels)(3)(5)			220	400	ps
t_{TLH}	Transition Time Low to High (20% to 80%)		0.4	0.75	1.3	ns
t_{THL}	Transition Time High to Low (80% to 20%)		0.4	0.75	1.3	ns
t_{PHZ}	Disable Time High to Z	R_L = 27Ω, 图 4, 图 5, C_L = 10 pF		5	10	ns
t_{PLZ}	Disable Time Low to Z			5	10	ns
t_{PZH}	Enable Time Z to High			5	10	ns
t_{PZL}	Enable Time Z to Low			5	10	ns
f_{MAXD}	Ensured operation per data sheet up to the Min. Duty Cycle 45/55%,Transition time ≤ 25% of period(3)		85	125		MHz
DIFFERENTIAL RECEIVER TIMING REQUIREMENTS						
t_{PHLDR}	Differential Prop. Delay High to Low(3)	图 6, 图 7, C_L = 15 pF	1.6	2.4	3.2	ns
t_{PLHDR}	Differential Prop Delay Low to High(3)		1.6	2.4	3.2	ns
t_{SDK1R}	Differential Skew $\|t_{PHLD}–t_{PLHD}\|$ (duty cycle)(4)(3)			85	160	ps
t_{CCSKR}	Channel to Channel Skew (all 4 channels)(3)(5)			140	300	ps
t_{TLHR}	Transition Time Low to High (10% to 90%)(3)		0.85	1.25	2	ns
t_{THLR}	Transition Time High to Low (90% to 10%)(3)		0.85	1.03	2	ns
t_{PHZ}	Disable Time High to Z	R_L = 500Ω, 图 8, 图 9, C_L = 15 pF		3	10	ns
t_{PLZ}	Disable Time Low to Z			3	10	ns
t_{PZH}	Enable Time Z to High			3	10	ns
t_{PZL}	Enable Time Z to Low			3	10	ns
f_{MAXR}	Ensured operation per data sheet up to the Min. Duty Cycle 45/55%,Transition time ≤ 25% of period(3)		85	125		MHz

(1) Generator waveforms for all tests unless otherwise specified: f = 25 MHz, Z_O = 50 Ω, t_r, t_f = <1 ns (0%–100%). To ensure fastest propagation delay and minimum skew, data input edge rates should be equal to or faster than 1 ns/V; control signals equal to or faster than 3ns/V. In general, the faster the input edge rate, the better the AC performance.
(2) C_L includes probe and fixture capacitance.
(3) Propagation delays, transition times, and receiver threshold are ensured by design and characterization.
(4) t_{SKD1} $|t_{PHLD}–t_{PLHD}|$ is the worst case pulse skew (measure of duty cycle) over recommended operation conditions.
(5) Chip to Chip skew is the difference in differential propagation delay between any channels of any devices, either edge.

7 Parameter Measurement Information

7.1 Test Circuits and Timing Waveforms

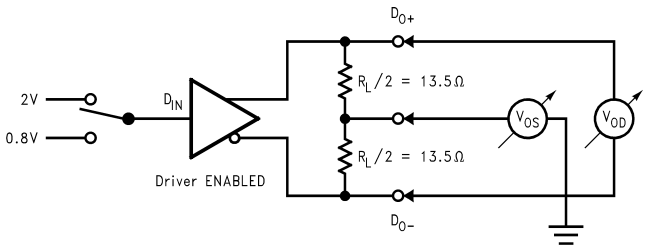


图 1. Differential Driver DC Test Circuit

Test Circuits and Timing Waveforms (接下页)

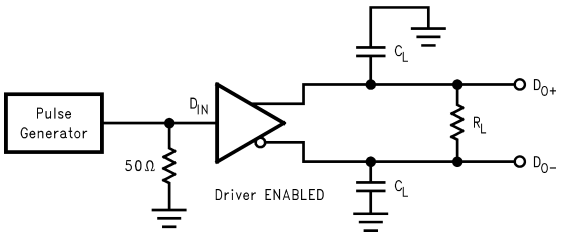


图 2. Differential Driver Propagation Delay and Transition Time Test Circuit

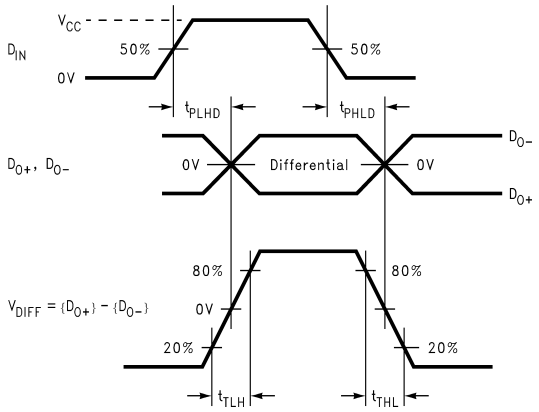


图 3. Differential Driver Propagation Delay and Transition Time Waveforms

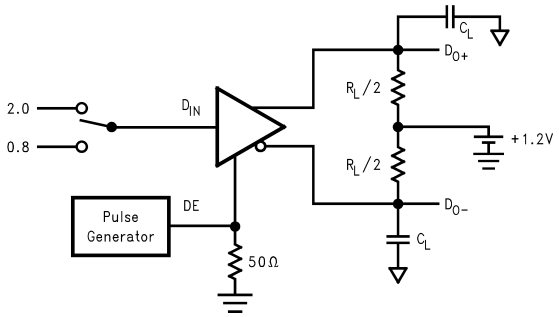


图 4. Driver TRI-STATE Delay Test Circuit

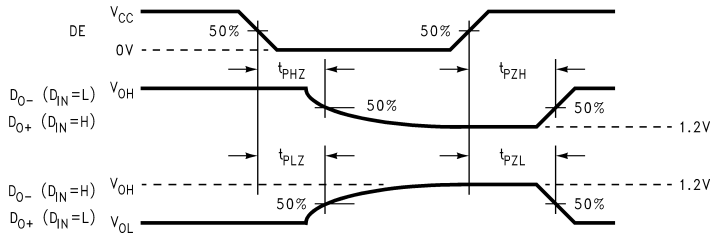


图 5. Driver TRI-STATE Delay Waveforms

Test Circuits and Timing Waveforms (接下页)

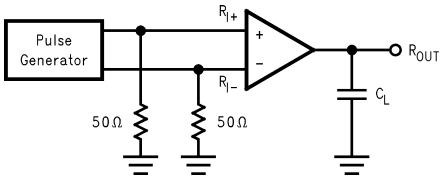


图 6. Receiver Propagation Delay and Transition Time Test Circuit

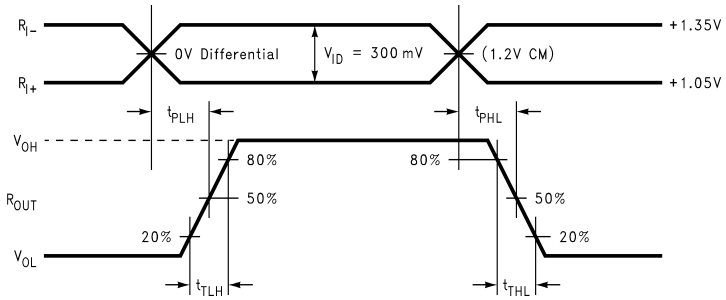


图 7. Receiver Propagation Delay and Transition Time Waveforms

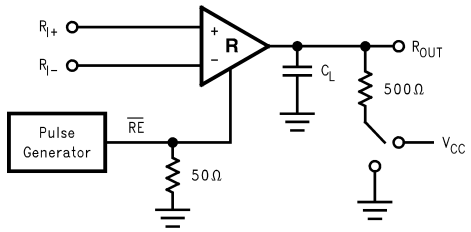


图 8. Receiver TRI-STATE Delay Test Circuit

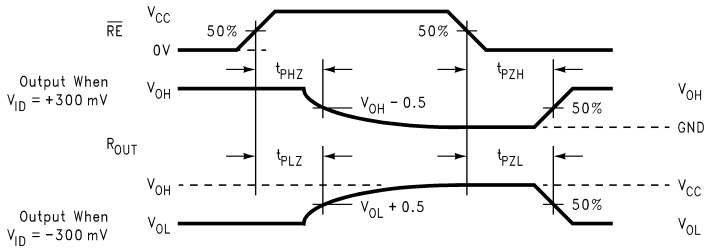


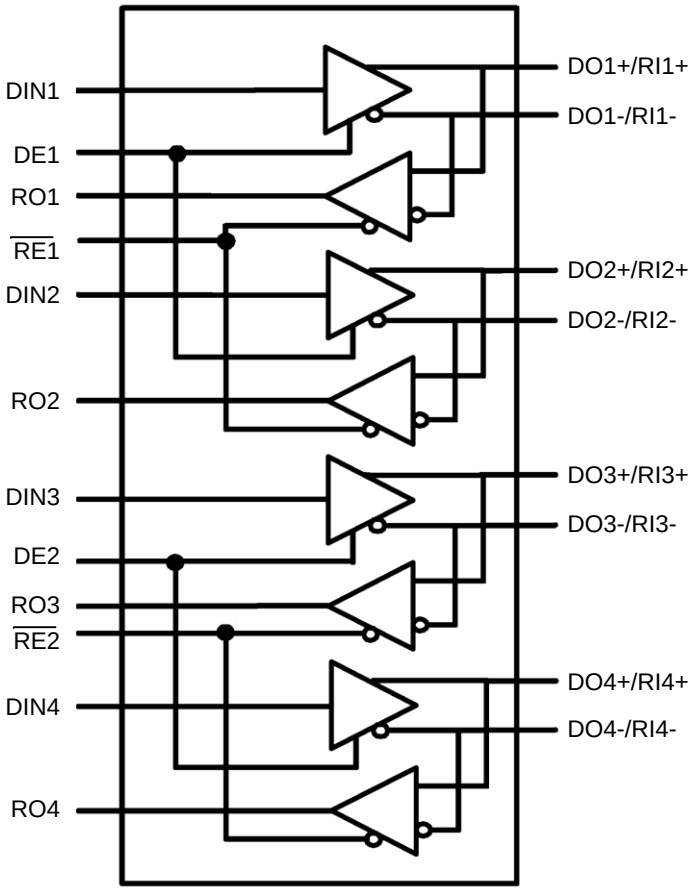
图 9. Receiver TRI-STATE Delay Waveforms

8 Detailed Description

8.1 Overview

BLVDS drivers and receivers are intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Z_O) is in the range of 50 Ω to 100 Ω. Two termination resistors of Z_O Ω each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuity as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

8.2 Functional Block Diagram



8.3 Feature Description

The DS92LV040A differential line driver is a balanced current mode design. A current mode driver, generally speaking has a high output impedance (100 Ω) and supplies a reasonably constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). The current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state.

Feature Description (接下页)

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case between 20 MHz–50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static ICC requirements of the ECL/PECL designs. LVDS requires 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers. The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

8.4 Device Functional Modes

表 1. Functional Table

MODE SELECTED	DE	$\overline{RE}$
DRIVER MODE	H	H
RECEIVER MODE	L	L
TRI-STATE MODE	L	H
LOOP BACK MODE	H	L

表 2. Transmitter Mode

INPUTS		OUTPUTS	
DE	D_{IN}	DO+	DO−
H	L	L	H
H	H	H	L
H	0.8V< D_{IN} <2.0V	X	X
L	X	Z	Z

表 3. Receiver Mode

INPUTS		OUTPUT
$\overline{RE}$	(RI+) – (RI−)	
L	L (< −70 mV)	L
L	H (> 0 mV)	H
L	−70 mV < V_{ID} < 0 mV	X
H	X	Z

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS92LV040A is a Bus LVDS transceiver intended to be used in a differential backplane configuration. Transceivers or receivers are connected to the driver through a balanced media such as differential PCB traces. Typically, the characteristic differential impedance of the media (Z_O) is in the range of 50 Ω to 100 Ω. Two termination resistors of Z_O Ω each are placed at the ends of the transmission line backplane. The termination resistor converts the current sourced by the driver into a voltage that is detected by the receiver. The effects of mid-stream connector(s), cable stub(s), and other impedance discontinuity as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The output current is typically 12 mA. The current mode requires that a resistive termination be employed to terminate the signal and to complete the loop. Unterminated configurations are not allowed. The 12 mA loop current will develop a differential voltage of about 300 mV across a 27 Ω (double terminated 54Ω differential transmission backplane) effective resistance, which the receiver detects with a 230 mV minimum differential noise margin neglecting resistive line losses (driven signal minus receiver threshold (300 mV – 70 mV = 230 mV)). The signal is centered around +1.2 V (Driver Offset, V_{OS}) with respect to ground. Note that the steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 600 mV.

9.2 Typical Application

9.2.1 Multipoint Communications

In a multipoint configuration many transmitters and many receivers can be interconnected on a single transmission line. The key difference compared to multi-drop is the presence of two or more drivers. Such a situation creates contention issues that need not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over a single balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary.

The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies.

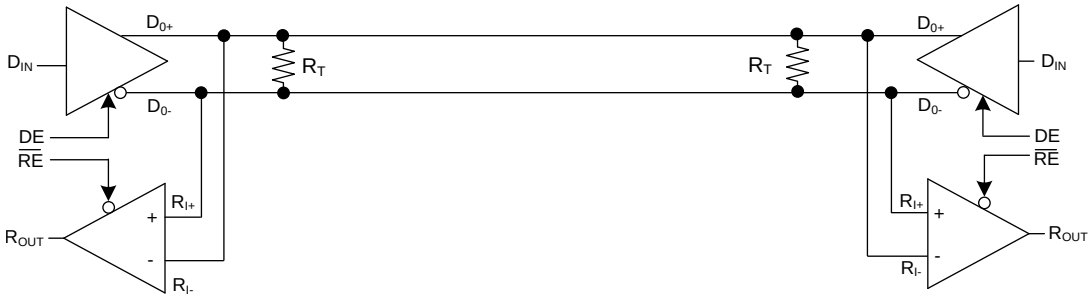


图 10. Bidirectional Half-Duplex Point-to-Point Applications

Typical Application (接下页)

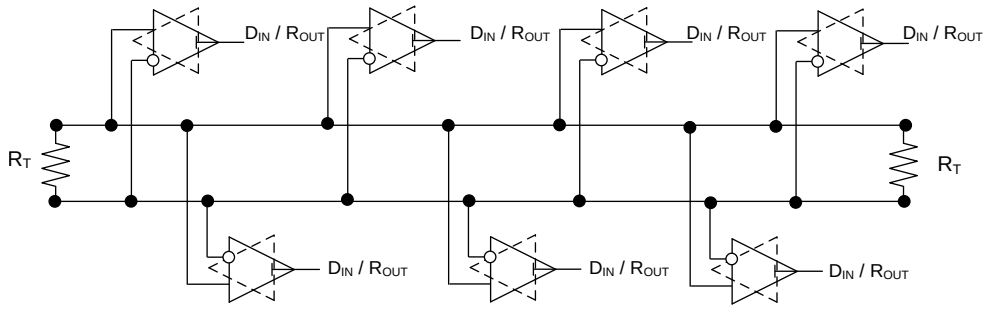


图 11. Multi-Point Bus Applications

9.2.2 Design Requirements

For this design example, use the parameters listed in 表 4.

表 4. Design Parameters

PARAMETERS	VALUES
Driver supply voltage	3 to 3.6 V
Driver input voltage	0.8 to 3.3 V
Driver signaling rate	DC to 200 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance (differential)	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage	3 to 3.6 V
Receiver input voltage	0 to (V_{CC} – 0.8) V
Receiver signaling rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

9.2.3 Detailed Design Procedure

9.2.3.1 Supply Voltage

The DS92LV040A is operated from a single supply. The device can support operations with a supply as low as 3 V and as high as 3.6 V.

9.2.3.2 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board level do a good job up into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors (in the nF to μF range) must be installed locally next to the integrated circuit.

9.2.3.3 Termination Resistors

Multipoint LVDS communication channel employs a current source driving a transmission line which is terminated with two resistive loads. These loads serve to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistors should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistors are within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistors should be between 90 Ω and 110 Ω. The line termination resistors are typically placed at the ends of the transmission line.

9.2.3.4 Interconnecting Media

The backplane and connectors should have a matched differential impedance. Use controlled impedance traces which match the differential impedance of your transmission medium (ie. backplane or cable) and termination resistor(s). Run the differential pair trace lines as close together as possible as soon as they leave the IC. This helps eliminate reflections and ensure noise is coupled as common-mode. In fact, it has been determined that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart since magnetic field cancellation is much better with the closer traces. Plus, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver. Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals which destroys the magnetic field cancellation benefits of differential signals and EMI will result.

Stub lengths should be kept to a minimum. The typical transition time of the DS92LV040A Bus LVDS output is 0.75 ns (20% to 80%). The extrapolated 100 percent time is 0.75/0.6 or 1.25 ns. For a general approximation, if the electrical length of a trace is greater than 1/5 of the transition edge, then the trace is considered a transmission line. For example, 1.25 ns/5 is 250 picoseconds. Let velocity equal 160 ps per inch for a typical loaded backplane. Then maximum stub length is 250 ps/160 ps/in or 1.56 inches. To determine the maximum stub for the backplane, determine the propagation velocity for the actual conditions (refer to application notes AN 905 and AN 808)

10 Power Supply Recommendations

The driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ±1 V. Board level and local device level bypass capacitance should be used and are covered Supply Bypass Capacitance.

11 Layout

11.1 Layout Guidelines

11.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in 图 12.

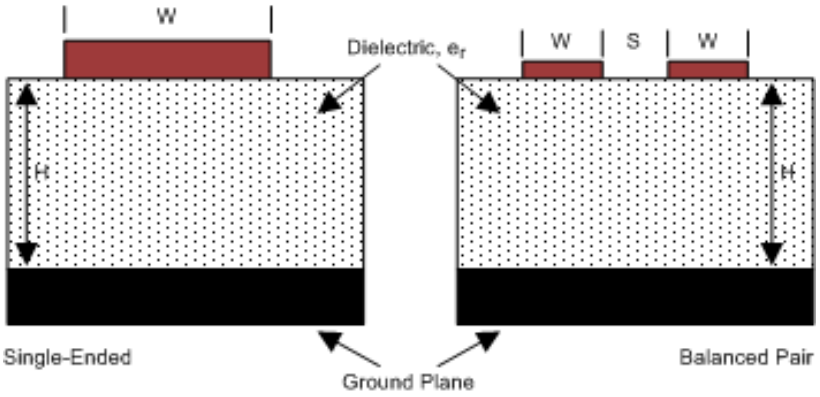


图 12. Microstrip Topology

Striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing the signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1(1), 2(2), and 3(3) provide formulas for Z_O and t_{PD} for differential and single-ended traces. (1) (2) (3)

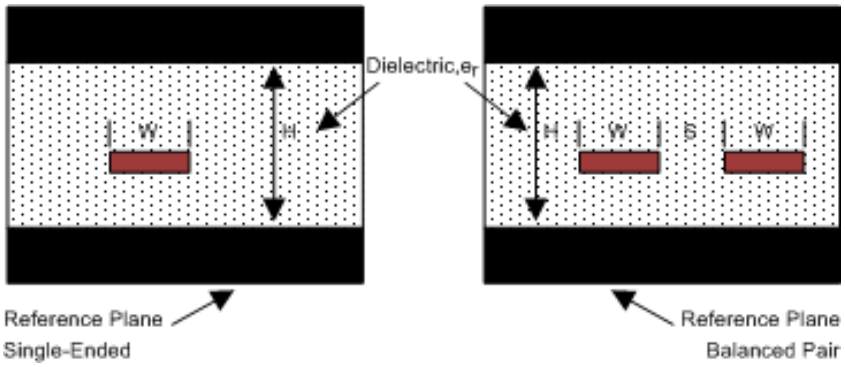


图 13. Stripline Topology

11.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with multipoint LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving multipoint LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz

(1) Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
(2) Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
(3) Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

Layout Guidelines (接下页)

- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

11.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to multipoint LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in 图 14.

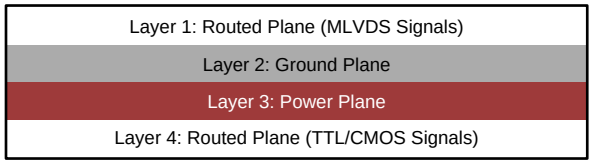


图 14. Four-Layer PCB Board

注

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in 图 15.

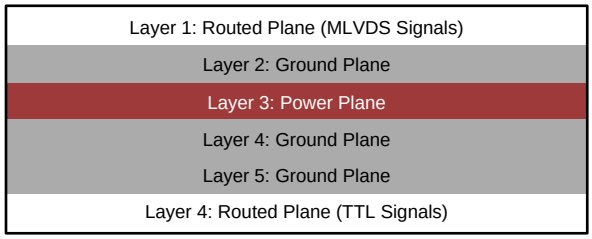


图 15. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

11.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an multipoint LVDS link to benefit from the electromagnetic field cancellation. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

If there are two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent multipoint LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

Layout Guidelines (接下页)

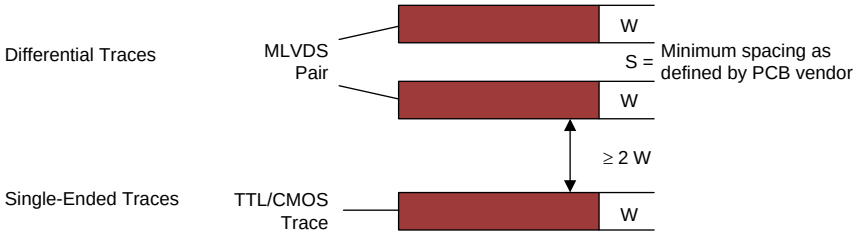


图 16. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

11.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

11.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

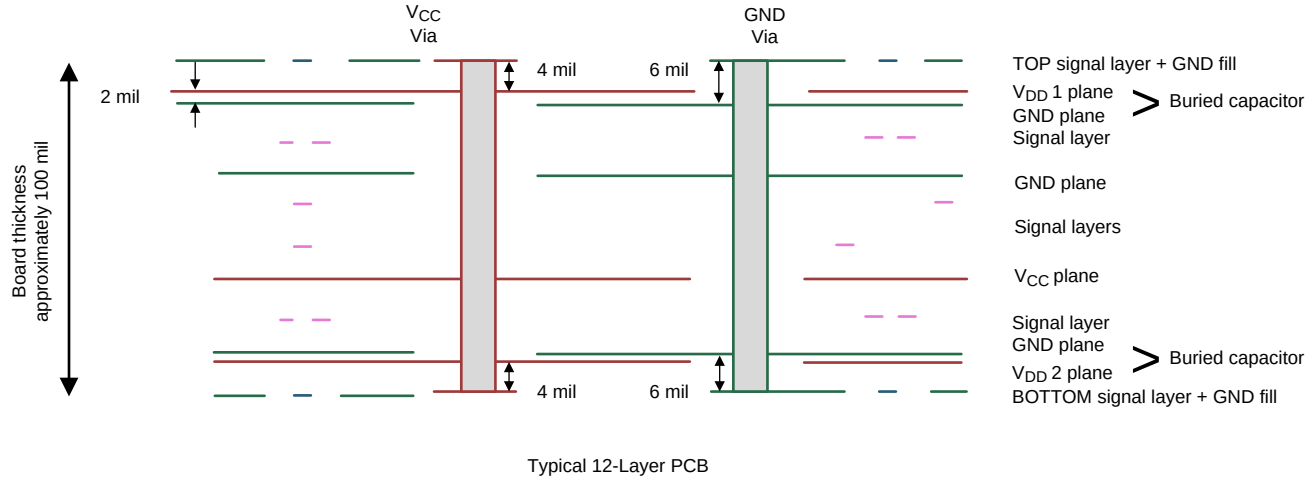


图 17. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402, 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in 图 18(a).

Layout Guidelines (接下页)

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in 图 18(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This results in a poor solder connection.

图 18. Typical Decoupling Capacitor Layouts

11.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in 图 19.

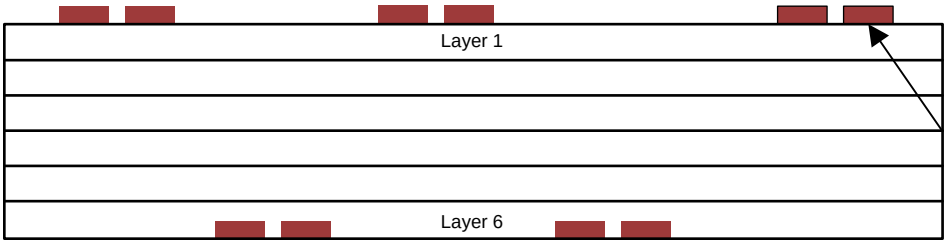


图 19. Staggered Trace Layout

Layout Example (接下页)

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in 图 20. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

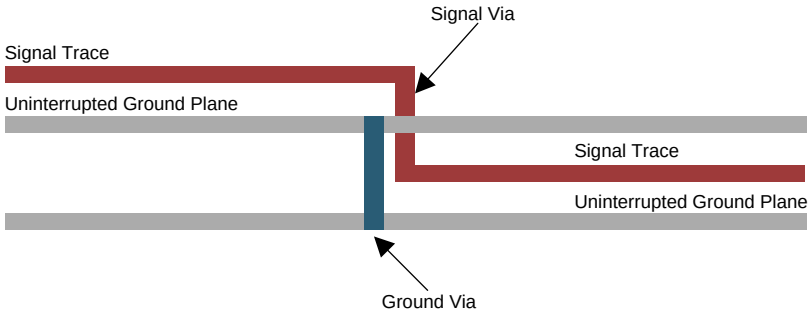


图 20. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

12 器件和文档支持

12.1 Documentation Support

12.1.1 Related Documentation

一般应用指南和提示可在以下应用手册中找到：), A)。

如需相关文档，请参阅：

- AN-808 (SNLA028)
- AN-977 (SNLA166
- AN-971 (SNLA165)
- AN-903 (SNLA034

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 Community Resources

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.4 商标

E2E is a trademark of Texas Instruments.
Rogers is a trademark of Rogers Corporation.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS92LV040ATLQA/NO.A	Active	Production	WQFN (NJN) | 44	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A
DS92LV040ATLQA/NOPB	Active	Production	WQFN (NJN) | 44	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A
DS92LV040ATLQAX/NO.A	Active	Production	WQFN (NJN) | 44	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A
DS92LV040ATLQAX/NO.B	Active	Production	WQFN (NJN) | 44	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
DS92LV040ATLQAX/NOPB	Active	Production	WQFN (NJN) | 44	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 85	LV040A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

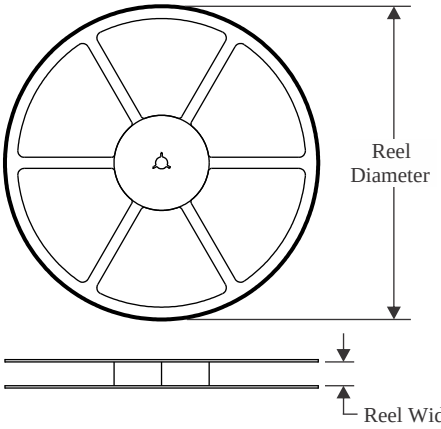
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

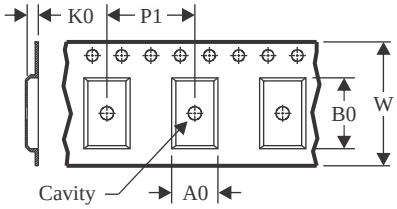
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

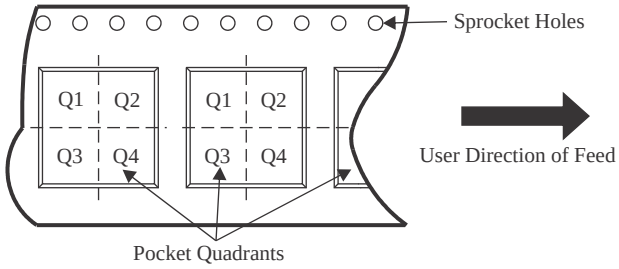


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

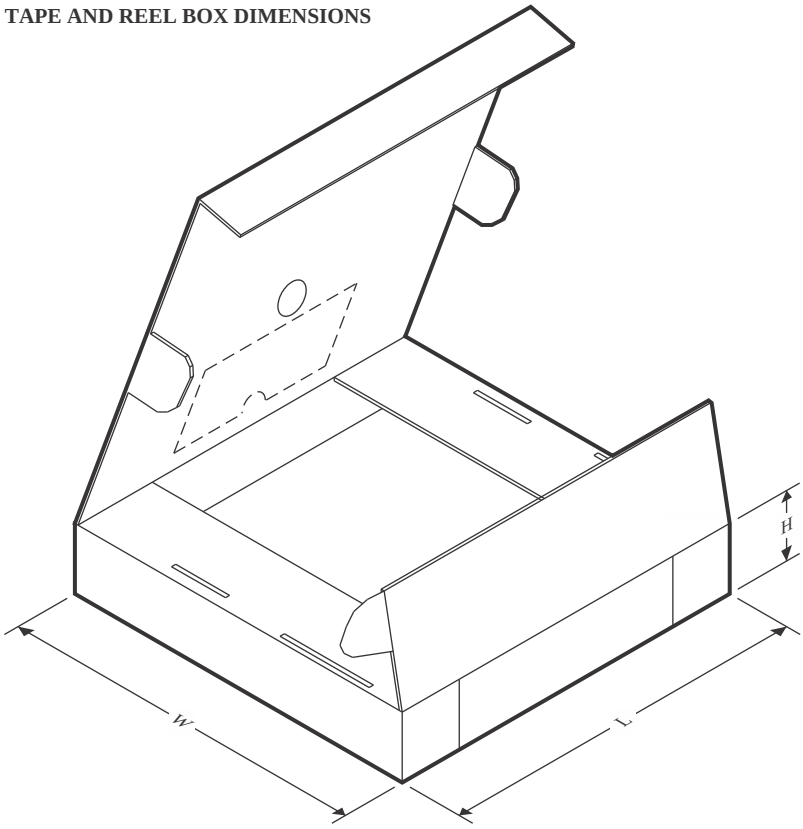
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

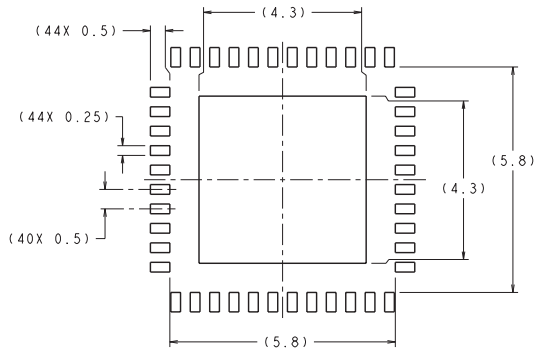
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS92LV040ATLQA/NOPB	WQFN	NJN	44	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS92LV040ATLQAX/ NOPB	WQFN	NJN	44	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



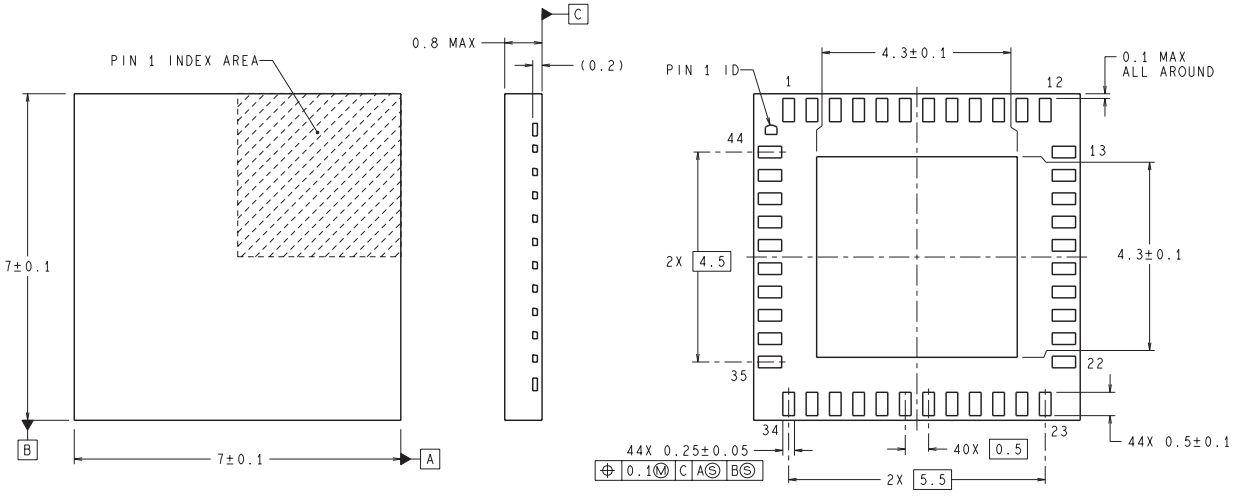
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS92LV040ATLQA/NOPB	WQFN	NJN	44	250	208.0	191.0	35.0
DS92LV040ATLQAX/ NOPB	WQFN	NJN	44	2500	356.0	356.0	36.0



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



LQA44A (REV B)

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