TEXAS INSTRUMENTS

TAS5754M

SLAS987 – JUNE 2014

Digital Input, Closed-Loop Class-D Amplifier with HybridFlow Processing

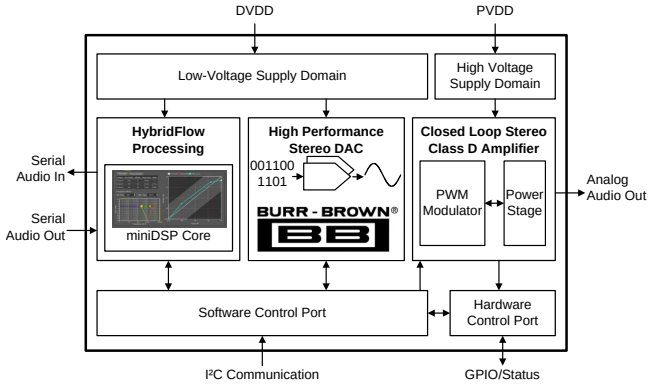
1 Features

- Flexible Audio I/O Configuration
  - Supports I^2S, TDM, LJ, RJ Digital Input
  - 8 kHz to 192 kHz Sample Rate Support
  - Stereo Bridge Tied Load (BTL) or Mono Parallel Bridge Tied Load (PBTL) Operation
  - BD Modulation with TAS5756M, 1SPW Modulation with TAS5754M
  - Supports 3-Wire Digital Audio Interface (No MCLK required)
- High Performance Closed-Loop Architecture (PVDD = 12V, R_{SPK} = 8 Ω, SPK_GAIN = 20dBV)
  - Idle Channel Noise = 62 µVrms (A-Wtd)
  - THD+N = 0.007 % (at 1 W, 1 kHz)
  - SNR = 103 A-Wtd (Ref. to THD+N = 1%)
- PurePath™ HybridFlow Processing Architecture
  - Several Configurable MiniDSP Programs (called HybridFlows)
  - Download Time <100 ms (typ)
  - Advanced Audio Processing Algorithms
- Communication Features
  - Software Mode Control via I^2C Port
  - Two Address Select Pins – Up to 4 Devices
- Robustness and Reliability Features
  - Clock Error, DC, and Short-Circuit Protection
  - Over Temperature and Overcurrent Protection

2 Applications

- LCD/LED TV and Multi-Purpose Monitors
- Sound Bars, Docking Stations, PC Audio
- Wireless Subwoofers, Bluetooth and Active Speakers

Figure 1. Simplified Block Diagram



3 Description

The TAS5754M device is a high-performance, stereo closed-loop amplifier with integrated audio processor with PurePath™ HybridFlow architecture. To convert from digital to analog, it uses a high performance DAC with Burr-Brown® mixed signal heritage. It requires only two power supplies: one DVDD for low-voltage circuitry and one PVDD for high-voltage circuitry. It is controlled via a software control port using standard I^2C communication. In the family, the TAS5756M uses traditional BD modulation, ensuring low distortion characteristics. The TAS5754M uses 1SPW modulation, reducing the idle current draw at the expense of slightly higher distortion.

The unique HybridFlow architecture allows the system designer to choose from several configurable DSP programs, specifically designed for use in popular audio end equipment such as bluetooth (BT) speakers, sound bars, docking stations, and subwoofers. This combines the flexibility of a fully programmable device with the fast download time and ease of use of a fixed function ROM device.

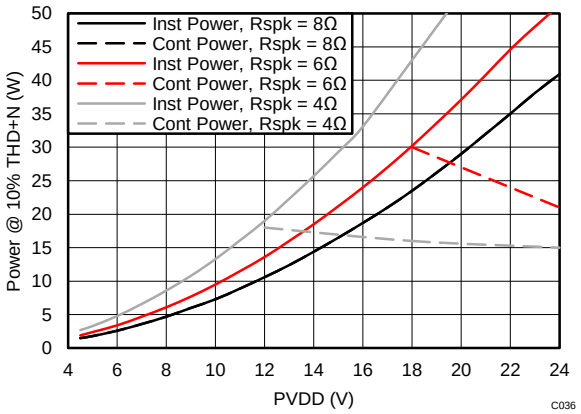
An optimal mix of thermal performance and device cost is provided in the 90 mΩ $r_{DS(on)}$ of the output MOSFETs. Additionally, a thermally enhanced 48-Terminal TSSOP provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5754M	TSSOP (48)	12.05 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Figure 2. Power at 10% THD+N vs PVDD



Note: Tested on TAS5754M-56MEVM.

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4 Revision History

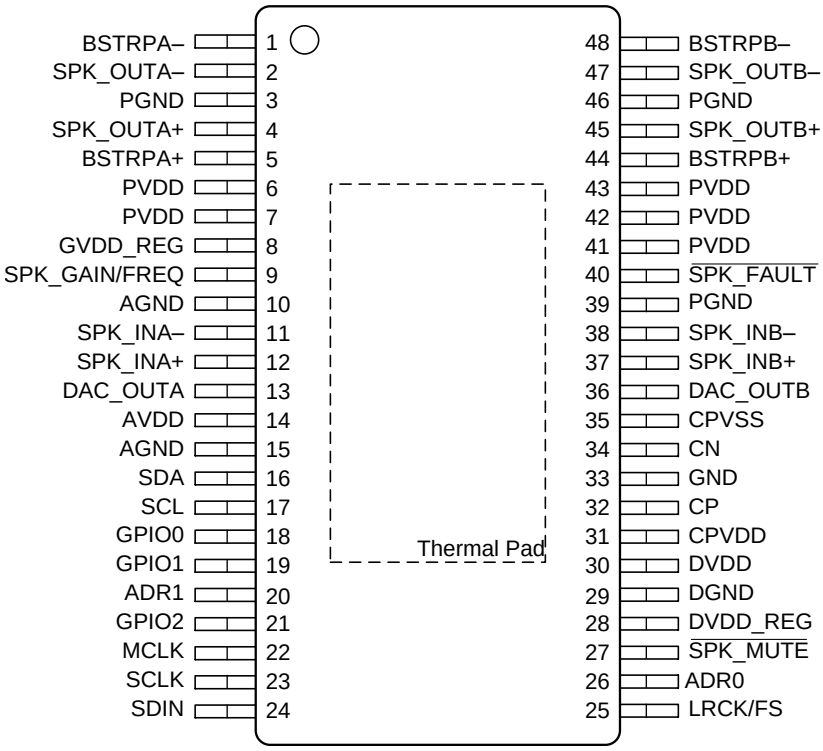
DATE	REVISION	NOTES
June 2014	*	Initial release.

5 Device Comparison Table

DEVICE NAME	MODULATION STYLE
TAS5754MDCA	1SPW (Ternary)
TAS5756MDCA	BD Modulation

6 Pin Configuration and Functions

48-Terminal TSSOP
DCA Package
(Thermal Pad Down)



Pin Functions

PIN		TYPE(1)	INTERNAL TERMINATION	DESCRIPTION
NAME	NO.			
ADR0	26	DI	Figure 13	Sets the LSB of the I^2C Address to 0 if pulled to GND, to 1 if pulled to DVDD
ADR1	20	DI		Sets the 2nd LSB of the I^2C Address to 0 if pulled to GND, to 1 if pulled to DVDD
AGND	10	G	—	Ground reference for analog circuitry (NOTE: This pin should be connected to the system ground)
	15			
AVDD	14	P	Figure 4	Power supply for internal analog circuitry
BSTRPA–	1	P	Figure 5	Connection point for the SPK_OUTA– bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTA–
BSTRPA+	5	P		Connection point for the SPK_OUTA+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTA
BSTRPB–	48	P		Connection point for the SPK_OUTB– bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTB–
BSTRPB+	44	P		Connection point for the SPK_OUTB+ bootstrap capacitor which is used to create a power supply for the high-side gate drive for SPK_OUTB+

(1) AI = Analog input, AO = Analog output, DI = Digital Input, DO = Digital Output, DI/O = Digital Bi-directional (input and output), P = Power, G = Ground (0 V)

Pin Functions (continued)

PIN		TYPE(1)	INTERNAL TERMINATION	DESCRIPTION
NAME	NO.			
CN	34	P	Figure 17	Negative pin for capacitor connection used in the headphone amplifier and line driver charge pump
CP	32	P	Figure 16	Positive pin for capacitor connection used in the headphone amplifier and line driver charge pump
CPVDD	31	P	Figure 4	Power supply for charge pump circuitry
CPVSS	35	P	Figure 17	–3.3-V supply generated by charge pump for the DAC
DAC_OUTA	13	AO	Figure 10	Single-ended output for Channel A of the DAC
DAC_OUTB	36	AO		Single-ended output for Channel B of the DAC
DGND	29	G	—	Ground reference for digital circuitry. Connect this pin to the system ground.
DVDD	30	P	Figure 4	Power supply for the internal digital circuitry
DVDD_REG	28	P	Figure 18	Voltage regulator derived from DVDD supply for use for internal digital circuitry. This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.
GND	33	G		Ground pin for device. This pin should be connected to the system ground.
GPIO0	18	DI/O	Figure 13	General purpose input/output pins (GPIOx) which can be incorporated in a HybridFlow for a given purpose. Refer to documentation of target HybridFlow to determine if any of these pins are required by the HybridFlow and, if so, how they are to be used. In most HybridFlows, presentation of a serial audio signal, called SDOUT, is done through GPIO2.
GPIO1	19			
GPIO2	21			
GVDD_REG	8	P	Figure 7	Voltage regulator derived from PVDD supply to generate the voltage required for the gate drive of output MOSFETs. This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry.
LRCK/FS	25	DI/O	Figure 14	Word select clock for the digital signal that is active on the serial port's input data line. In I^2S, LJ, and RJ, this corresponds to the left channel and right channel boundary. In TDM mode, this corresponds to the frame sync boundary.
MCLK	22	DI		Master clock used for internal clock tree and sub-circuit and state machine clocking
PGND	3	G	—	Ground reference for power device circuitry. Connect this pin to the system ground.
	39			
	46			
PVDD	6	P	Figure 3	Power supply for internal power circuitry
	7			
	41			
	42			
	43			
SCL	17	DI	Figure 12	I^2C serial control port clock
SCLK	23	DI/O	Figure 14	Bit clock for the digital signal that is active on the input data line of the serial data port
SDA	16	DI/O	Figure 11	I^2C serial control port data
SDIN	24	D1	Figure 14	Data line to the serial data port
SPK_INA–	11	AI	Figure 9	Negative pin for differential speaker amplifier input A
SPK_INA+	12	AI		Positive pin for differential speaker amplifier input A
SPK_INB–	38	AI		Negative pin for differential speaker amplifier input B
SPK_INB+	37	AI		Positive pin for differential speaker amplifier input B
$\overline{\text{SPK\_FAULT}}$	40	DO	Figure 19	Fault pin which is pulled low when an overcurrent, overtemperature, overvoltage, undervoltage, or DC detect event occurs
SPK_GAIN/FREQ	9	AI	Figure 8	Sets the gain and switching frequency of the speaker amplifier.
SPK_OUTA–	2	AO	Figure 6	Negative pin for differential speaker amplifier output A
SPK_OUTA+	4	AO		Positive pin for differential speaker amplifier output A
SPK_OUTB–	47	AO		Negative pin for differential speaker amplifier output B
SPK_OUTB+	45	AO		Positive pin for differential speaker amplifier output B
$\overline{\text{SPK\_MUTE}}$	27	I	Figure 15	Speaker amplifier mute which must be pulled low (connected to DGND) to mute the device and pulled high (connected to DVDD) to unmute the device.
Themal pad		G	—	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it through solder. For proper electrical operation, this ground pad must be connected to the system ground.

6.1 Internal Pin Configurations

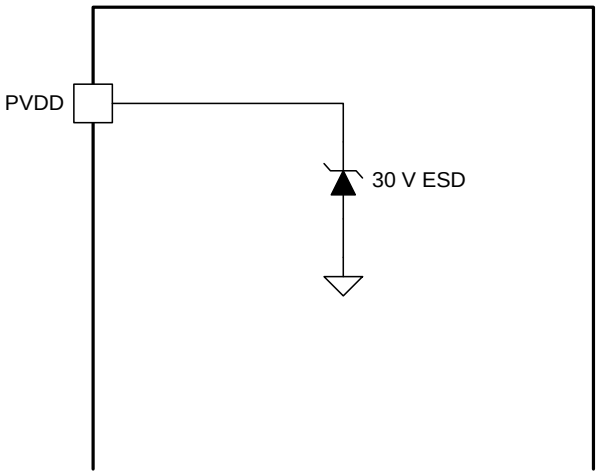


Figure 3. PVDD Pins

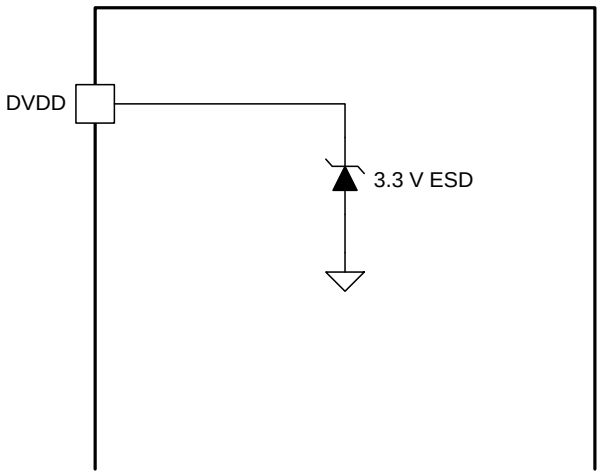


Figure 4. AVDD, DVDD and CPVDD Pins

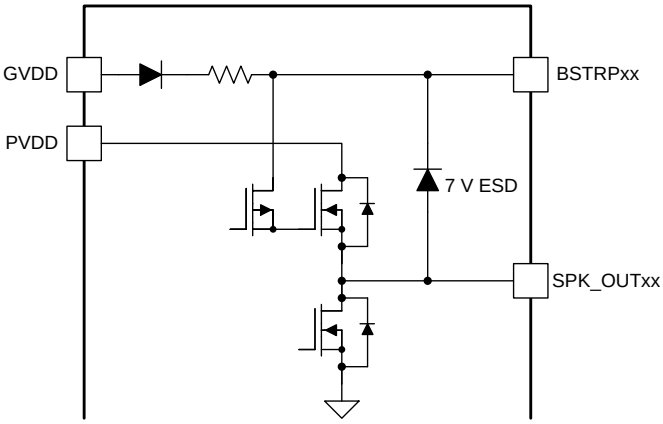


Figure 5. BSTRPxx Pins

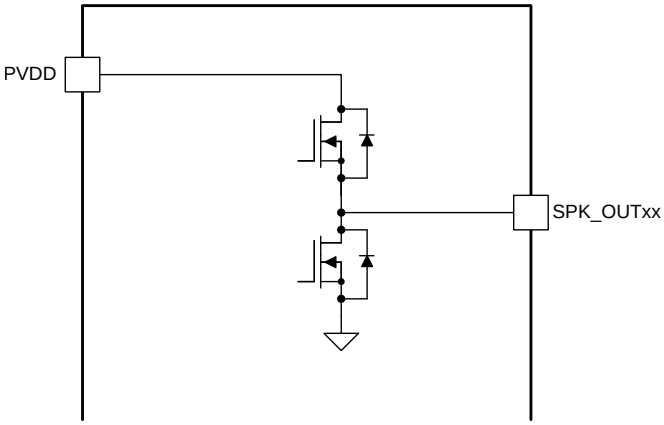


Figure 6. SPK_OUTxx Pins

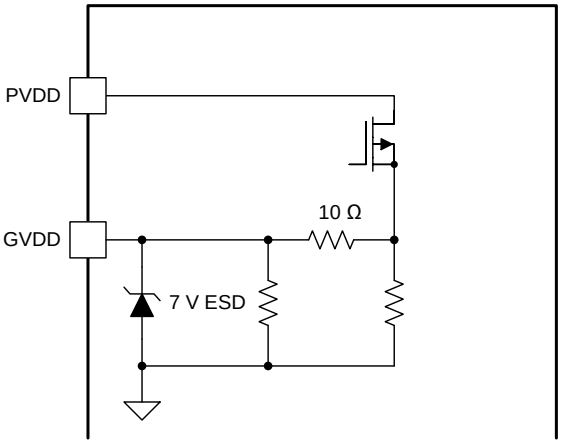


Figure 7. GVDD_REG Pin

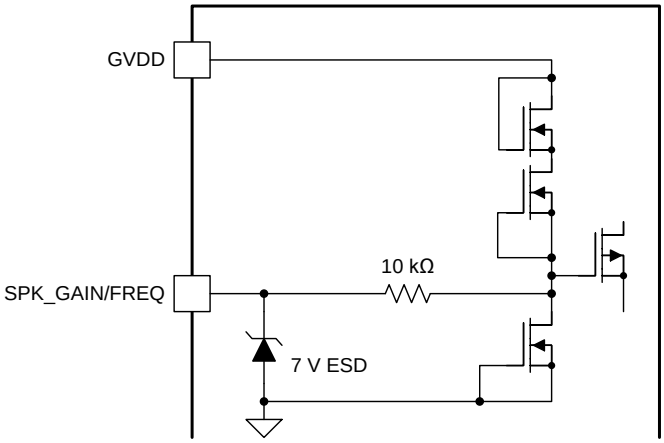


Figure 8. SPK_GAIN/FREQ Pin

Internal Pin Configurations (continued)

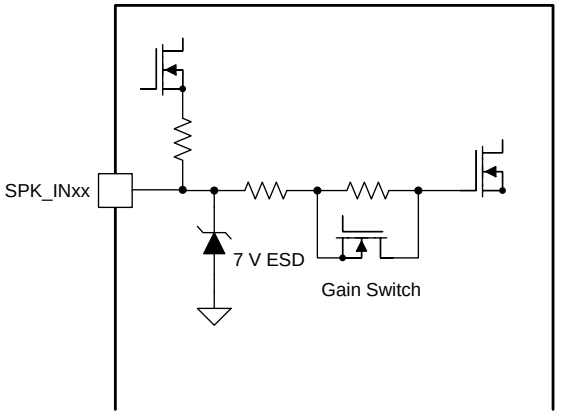


Figure 9. SPK_INxx Pins

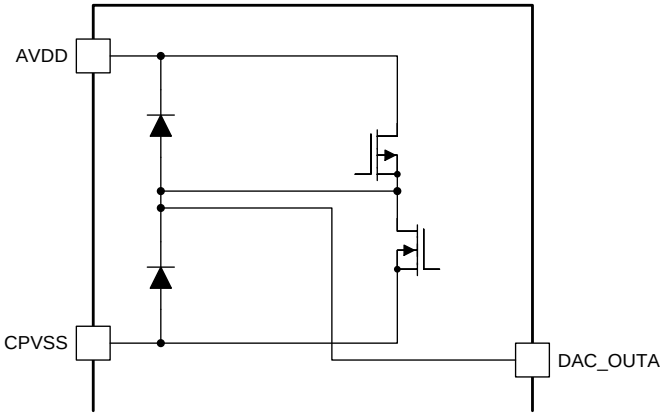


Figure 10. DAC_OUTx Pins

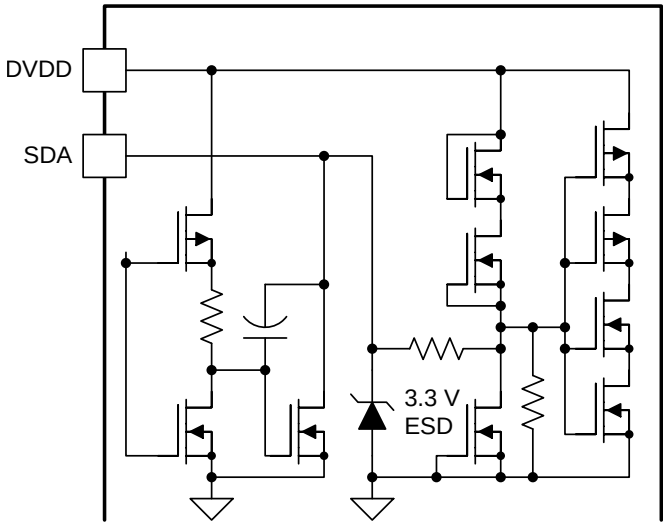


Figure 11. SDA Pin

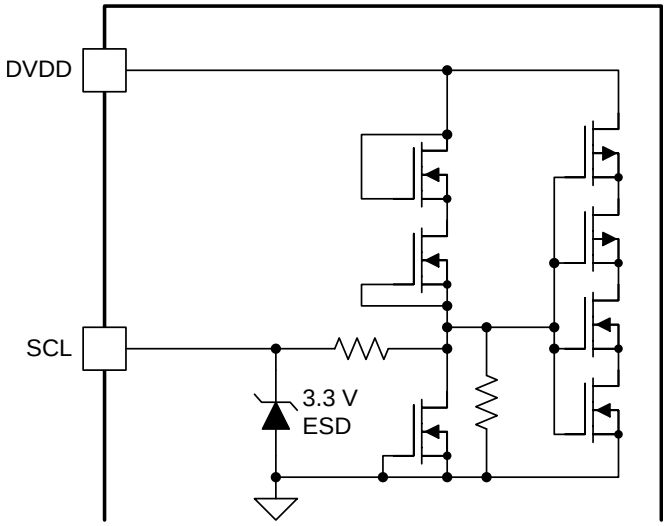


Figure 12. SCL Pin

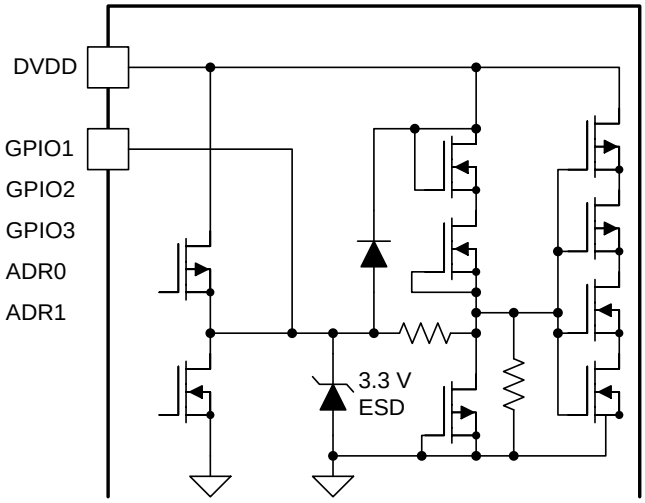


Figure 13. GPIO and ADR Pins

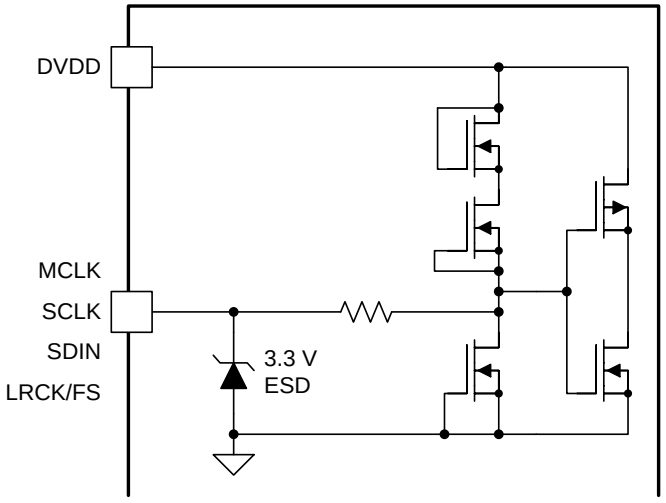


Figure 14. SCLK, BCLK, SDIN, and LRCK/FS Pins

Internal Pin Configurations (continued)

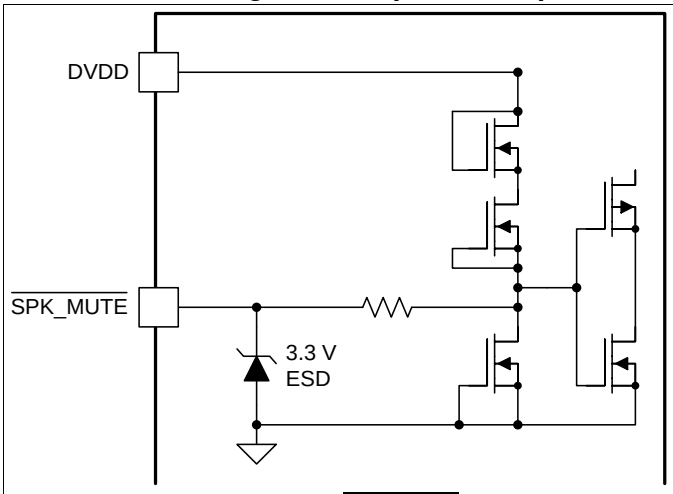


Figure 15. $\overline{\text{SPK\_MUTE}}$ Pin

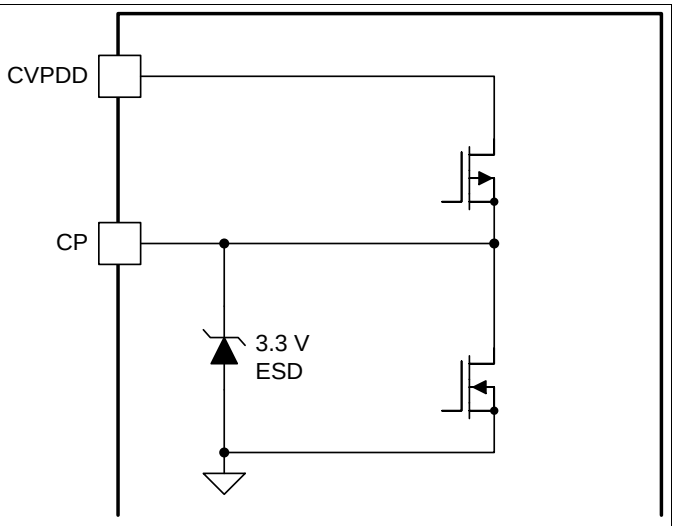


Figure 16. CP Pin

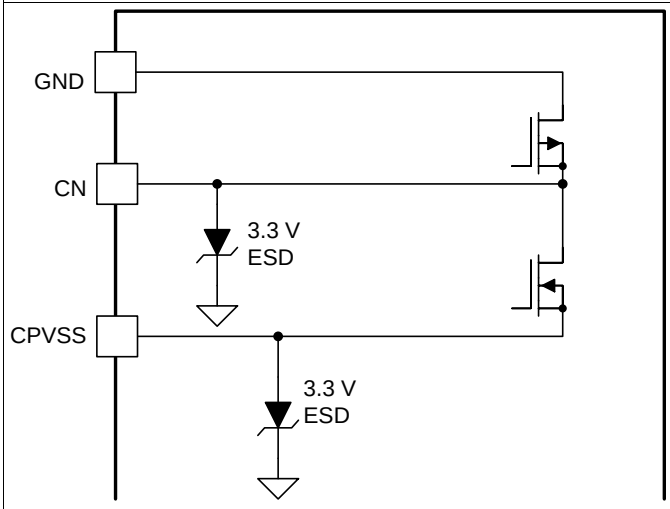


Figure 17. CN and CPVSS Pins

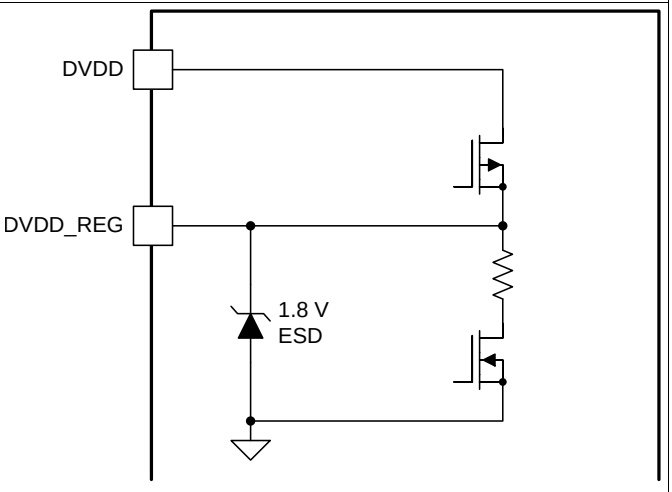


Figure 18. DVDD_REG Pin

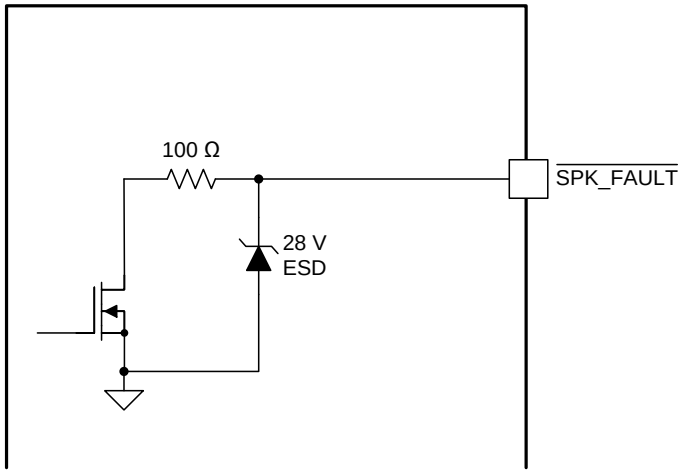


Figure 19. $\overline{\text{SPK\_FAULT}}$ Pin

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Low-voltage digital, analog, charge pump supply	DVDD, AVDD, CPVDD	–0.3	3.9	V
PVDD supply	PVDD	–0.3	30	V
Input voltage for SPK_GAIN/FREQ and SPK_FAULT pins	$V_{I(AmpCtrl)}$	–0.3	V_{GVDD}+0.3	V
DVDD referenced digital inputs(2)	$V_{I(DigIn)}$	–0.5	V_{DVDD}+0.5	V
Analog input into speaker amplifier	$V_{I(SPK\_INxx)}$	–0.3	6.3	V
Voltage at speaker output pins	$V_{I(SPK\_OUTxx)}$	–0.3	32	V
Ambient operating temperature, T_A		–25	85	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO1, GPIO2, LRCK/FS, MCLK, SCL, SCLK, SDA, SDIN, and SPK_MUTE.

7.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–40	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	–2	2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(POWER)}$	Power supply inputs	DVDD, AVDD, CPVDD	2.9		3.63	V
		PVDD	4.5		26.4	
R_{SPK}	Minimum speaker load in BTL mode		3			Ω
	Minimum speaker load in PBTL mode		2			Ω
$V_{IH(DigIn)}$	Input logic high for DVDD referenced digital inputs(1)(2)		$0.9\times V_{DVDD}$		V_{DVDD}	V
$V_{IL(DigIn)}$	Input logic low for DVDD referenced digital inputs(1)(3)		V_{DVDD}	0	$0.1\times V_{DVDD}$	V
L_{OUT}	Minimum inductor value in LC filter under short-circuit condition		1	4.7		µH

(1) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO1, GPIO2, LRCK/FS, MCLK, SCL, SCLK, SDA, SDIN, and SPK_MUTE.
(2) The best practice for driving the input pins of the TAS5754M device is to power the drive circuit or pull-up resistor from the same supply which provides the DVDD power supply.
(3) The best practice for driving the input pins of the TAS5754M device low is to pull them down, either actively or through pull-down resistors to the system ground.

7.4 Thermal Information

THERMAL METRIC(1)		TSSOP (48 PINS)			UNIT
		JEDEC STANDARD 2 LAYER PCB	JEDEC STANDARD 4 LAYER PCB	TAS5754M-56MEVM (AIP012A)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.8	27.6	19.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.4	14.4	14.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	9.4	9.4	
Ψ_{JT}	Junction-to-top characterization parameter	0.6	0.6	2.0	
Ψ_{JB}	Junction-to-board characterization parameter	8.1	9.3	4.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.0	1.0	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL I/O						
|IIH|1	Input logic high current level for DVDD referenced digital input pins(1)	$V_{IN(DigIn)} = V_{DVDD}$			10	µA
|IIL|1	Input logic low current level for DVDD referenced digital input pins.(1)	$V_{IN(DigIn)}$ = 0 V			–10	µA
V_{IH1}	Input logic high threshold for DVDD referenced digital inputs(1)		70%			V_{DVDD}
V_{IL1}	Input logic low threshold for DVDD referenced digital inputs(1)				30%	V_{DVDD}
$V_{OH(DigOut)}$	Output logic high voltage level(1)	I_{OH} = 4 mA	80%			V_{DVDD}
$V_{OL(DigOut)}$	Output logic low voltage level(1)	I_{OH} = –4mA			22%	V_{DVDD}
$V_{OL(\overline{SPK\_FAULT})}$	Output logic low voltage level for $\overline{SPK\_FAULT}$	With 100-kΩ pull-up resistor			0.8	V
I²C CONTROL PORT						
$C_{L(I2C)}$	Allowable load capacitance for each I²C Line				400	pF
$f_{SCL(fast)}$	Support SCL frequency	No wait states, fast mode			400	kHz
$f_{SCL(slow)}$	Support SCL frequency	No wait states, slow mode			100	kHz
V_{NH}	Noise margin at High level for each connected device (including hysteresis)		0.2 × V_{DD}			V
MCLK AND PLL SPECIFICATIONS						
D_{MCLK}	Allowable MCLK duty cycle		40%		60%	
f_{MCLK}	Supported MCLK frequencies	Up to 50 MHz	128		512	f_S(2)
f_{PLL}	PLL input frequency	Clock divider uses fractional divide D > 0, P = 1	6.7		20	MHz
		Clock divider uses integer divide D = 0, P = 1	1		20	MHz

(1) DVDD referenced digital pins include: ADR0, ADR1, GPIO0, GPIO1, GPIO2, LRCK/FS, MCLK, SCL, SCLK, SDA, SDIN, and $\overline{SPK\_MUTE}$.
(2) A unit of f_S indicates that the specification is the value listed in the table multiplied by the sample rate of the audio used in the TAS5754M device .

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SERIAL AUDIO PORT						
t_{DLY}	Required LRCK/FS to SCLK rising edge delay		5			ns
D_{SCLK}	Allowable SCLK duty cycle		40%		60%	
f_S	Supported input sample rates		8		192	kHz
f_{SCLK}	Supported SCLK frequencies		32		64	f_S (3)
f_{SCLK}	SCLK frequency	Either master mode or slave mode			24.576	MHz
SPEAKER AMPLIFIER (ALL OUTPUT CONFIGURATIONS)						
$A_{V(SPK\_AMP)}$	Speaker amplifier gain	SPK_GAIN/FREQ voltage < 3.0 V, see Adjustable Amplifier Gain and Switching Frequency Selection		20.3		dBV
		SPK_GAIN/FREQ voltage > 3.3 V, see Adjustable Amplifier Gain and Switching Frequency Selection		26.427		dBV
$\Delta A_{V(SPK\_AMP)}$	Typical variation of speaker amplifier gain			±1		dBV
f_{SPK_AMP}	Switching frequency of the speaker amplifier	Switching frequency depends on voltage presented at SPK_GAIN/FREQ pin and the clocking arrangement, including the incoming sample rate, see Adjustable Amplifier Gain and Switching Frequency Selection	176.4		768	kHz
K_{SVR}	Power supply rejection ratio	Injected Noise = 50 Hz to 60 Hz, 200 mV_{P-P}, Gain = 26dBV, input audio signal = digital zero		60		dB
$r_{DS(on)}$	Drain-to-source on resistance of the individual output MOSFETs	V_{PVDD} = 24 V, $I_{(SPK\_OUT)}$ = 500 mA, T_J = 25°C, includes PVDD/PGND pins, leadframe, bondwires and metallization layers.		90		mΩ
		V_{PVDD} = 24 V, $I_{(SPK\_OUT)}$ = 500 mA, T_J = 25°C		90		mΩ
OCE_{THRES}	SPK_OUTxx Over-Current Error Threshold			7.5		A
OTE_{THRES}	Over-Temperature Error Threshold			150		°C
$OVE_{THRES(PVDD)}$	PVDD Over-Voltage Error Threshold			27		V
$UVE_{THRES(PVDD)}$	PVDD Under-Voltage Error Threshold			4.5		V
SPEAKER AMPLIFIER (STEREO BTL)						
$\|V_{OS}\|$	Amplifier offset voltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20dBV gain, V_{PVDD} = 12 V		2	10	mV
		Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 26dBV gain, V_{PVDD} = 24 V		5	15	

(3) A unit of f_S indicates that the specification is the value listed in the table multiplied by the sample rate of the audio used in the TAS5754M device .

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CN(SPK)}$	Idle channel noise	V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 8 Ω, A-Weighted		62		μV_{RMS}
		V_{PVDD} = 15 V, SPK_GAIN = 20dBV, R_{SPK} = 8 Ω, A-Weighted		65		
		V_{PVDD} = 19 V, SPK_GAIN = 26dBV, R_{SPK} = 8 Ω, A-Weighted		78		
		V_{PVDD} = 24 V, SPK_GAIN = 26dBV, R_{SPK} = 8 Ω, A-Weighted		81		
$P_{O(SPK)}$	Maximum continuous output power per channel	V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		14		W
		V_{PVDD} = 24 V, SPK_GAIN = 26dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		40		
		V_{PVDD} = 24 V, SPK_GAIN = 26dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		33		
		V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		30		
		V_{PVDD} = 19 V, SPK_GAIN = 26dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		21		
		V_{PVDD} = 19 V, SPK_GAIN = 26dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		18		
		V_{PVDD} = 15 V, SPK_GAIN = 26dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		23		
		V_{PVDD} = 15 V, SPK_GAIN = 26dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		13		
SNR	Signal-to-noise ratio (referenced to 0dBFS input signal)	V_{PVDD} = 15 V, SPK_GAIN = 26dBV, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		102		dB
		V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		103		
		V_{PVDD} = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		105		
		V_{PVDD} = 19 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		103		
$THD+N_{SPK}$	Total harmonic distortion and noise	V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 4 Ω, P_O = 1 W		0.009%		
		V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 8 Ω, P_O = 1 W		0.006%		
		V_{PVDD} = 24 V, SPK_GAIN = 20dB, R_{SPK} = 4 Ω, P_O = 1 W		0.028%		
		V_{PVDD} = 15 V, SPK_GAIN = 20dB, R_{SPK} = 4 Ω, P_O = 1 W		0.018%		
		V_{PVDD} = 15 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, P_O = 1 W		0.017%		
		V_{PVDD} = 19 V, SPK_GAIN = 20dB, R_{SPK} = 4 Ω, P_O = 1 W		0.02%		
		V_{PVDD} = 19 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, P_O = 1 W		0.017%		
		V_{PVDD} = 24 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, P_O = 1 W		0.022%		

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$X\text{-talk}_{SPK}$	Cross-talk (worst case between left-to-right and right-to-left coupling)	V_{PVDD} = 15 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–102		dB
		V_{PVDD} = 12 V, SPK_GAIN = 20dBV, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–90		
		V_{PVDD} = 24 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–93		
		V_{PVDD} = 19 V, SPK_GAIN = 20dB, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1-kHz Sine, across f(S)		–93		
SPEAKER AMPLIFIER (MONO PBTL)						
$\lvert V_{OS} \rvert$	Amplifier offset voltage	Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20dBV gain, V_{PVDD} = 12 V		0.7	8	mV
		Measured differentially with zero input data, SPK_GAIN/FREQ pin configured for 20dB gain, V_{PVDD} = 24 V		4	14	
I_{CN}	Idle channel noise	V_{PVDD} = 15 V, SPK_GAIN = 20 dBV, RSPK = 8 Ω, A-Weighted		64		μV_{RMS}
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 8 Ω, A-Weighted		62		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, RSPK = 8 Ω, A-Weighted		83		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, A-Weighted		82		

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Maximum continuous output power per channel	V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		40		W
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		61		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		34		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		50		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		9		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		36		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		20		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		44		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		22		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, THD+N = 0.1%		13		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 2 Ω, THD+N = 0.1%, Unless otherwise noted		30		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 4 Ω, THD+N = 0.1%, Unless otherwise noted		16		
SNR	Signal-to-noise ratio (referenced to 0dBFS input signal)	V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		104		dB
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		105		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		107		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, A-Weighted, -120dBFS Input		105		

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion and noise	V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 4 Ω, P_O = 1 W		0.019%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 8 Ω, P_O = 1 W		0.014%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 4 Ω, P_O = 1 W		0.035%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 2 Ω, P_O = 1 W		0.04%		
		V_{PVDD} = 24 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, P_O = 1 W		0.027%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 4 Ω, P_O = 1 W		0.029%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 2 Ω, P_O = 1 W		0.047%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 4 Ω, P_O = 1 W		0.025%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 2 Ω, P_O = 1 W		0.047%		
		V_{PVDD} = 15 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, P_O = 1 W		0.015%		
		V_{PVDD} = 12 V, SPK_GAIN = 20 dBV, R_{SPK} = 2 Ω, P_O = 1 W		0.037%		
		V_{PVDD} = 19 V, SPK_GAIN = 26 dBV, R_{SPK} = 8 Ω, P_O = 1 W		0.020%		

7.6 MCLK Timing

		MIN	NOM	MAX	UNIT
t_{MCLK}	MCLK period	20		1000	ns
t_{MCLKH}	MCLK pulse width, high	9			ns
t_{MCLKL}	MCLK pulse width, low	9			ns

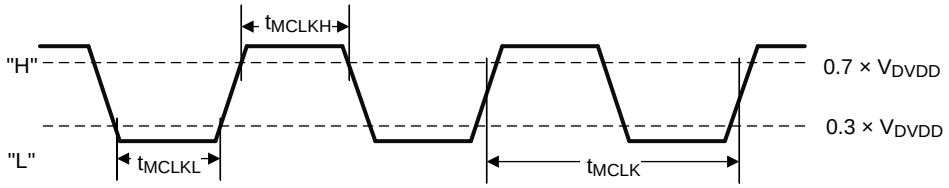


Figure 20. Timing Requirements for MCLK Input

7.7 Serial Audio Port Timing – Slave Mode

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{SL}	SCLK rising to LRCK/FS edge	8			ns
t_{LS}	LRCK/FS Edge to SCLK rising edge	8			ns
t_{SU}	Data set-up time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns

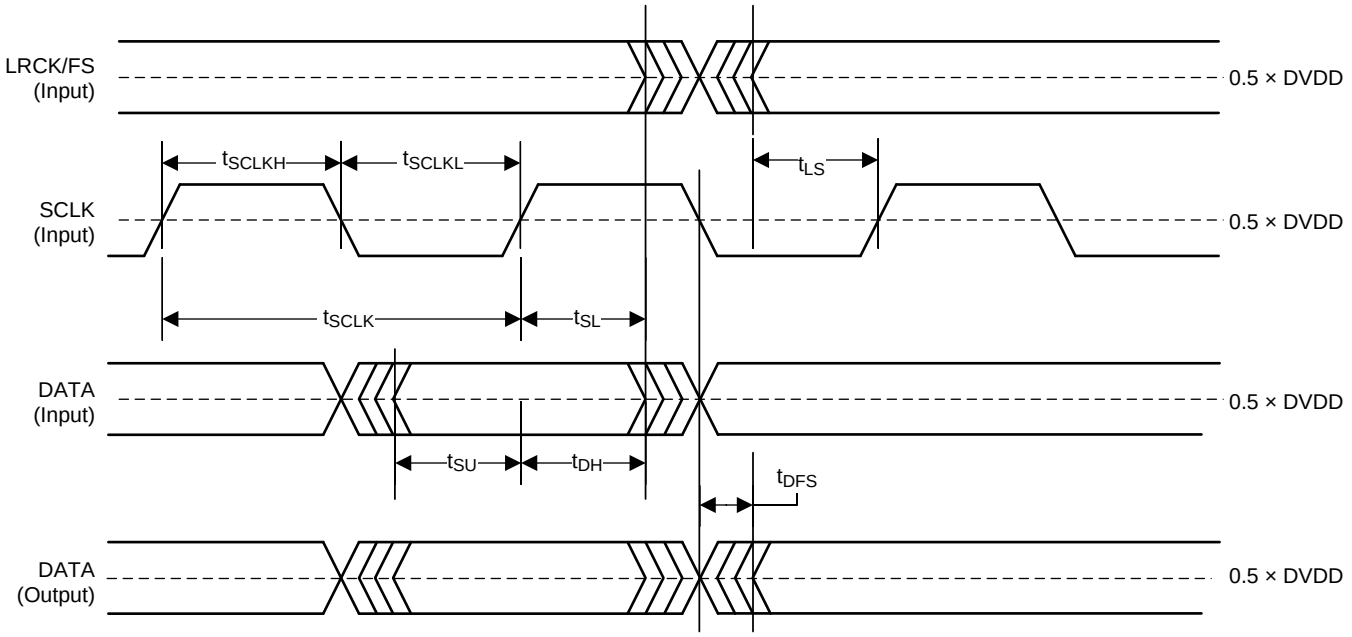


Figure 21. MCLK Timing Diagram in Slave Mode

7.8 Serial Audio Port Timing – Master Mode

		MIN	NOM	MAX	UNIT
t_{SCLK}	SCLK period	40			ns
t_{SCLKL}	SCLK pulse width, low	16			ns
t_{SCLKH}	SCLK pulse width, high	16			ns
t_{LRD}	LRCK/FS delay time from to SCLK falling edge	–10		20	ns
t_{SU}	Data set-up time, before SCLK rising edge	8			ns
t_{DH}	Data hold time, after SCLK rising edge	8			ns
t_{DFS}	Data delay time from SCLK falling edge			15	ns

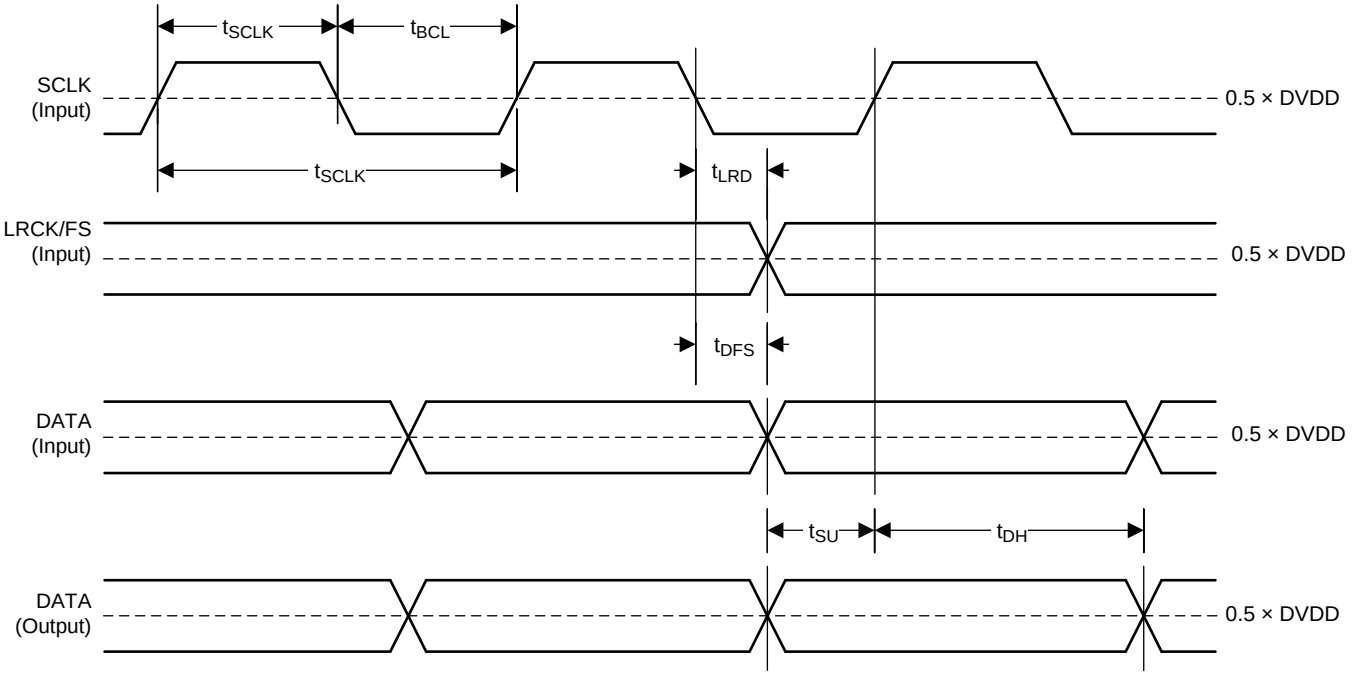


Figure 22. MCLK Timing Diagram in Master Mode

7.9 I²C Bus Timing – Standard

		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		100	kHz
t_{BUF}	Bus free time between a STOP and START condition	4.7		µs
t_{LOW}	Low period of the SCL clock	4.7		µs
t_{HI}	High period of the SCL clock	4.0		µs
t_{RS-SU}	Setup time for (repeated)START condition	4.7		µs
t_{S-HD}	Hold time for (repeated)START condition	4.0		µs
t_{D-SU}	Data setup time	250		ns
t_{D-HD}	Data hold time	0	900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$	1000	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$	1000	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$	1000	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$	1000	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$	1000	ns
t_{P-SU}	Setup time for STOP condition	4.0		µs

7.10 I²C Bus Timing – Fast

		MIN	MAX	UNIT
f_{SCL}	SCL clock frequency		400	kHz
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
t_{LOW}	Low period of the SCL clock	1.3		µs
t_{HI}	High period of the SCL clock	600		ns
t_{RS-SU}	Setup time for (repeated)START condition	600		ns
t_{RS-HD}	Hold time for (repeated)START condition	600		ns
t_{D-SU}	Data setup time	100		ns
t_{D-HD}	Data hold time	0	900	ns
t_{SCL-R}	Rise time of SCL signal	$20 + 0.1C_B$	300	ns
t_{SCL-R1}	Rise time of SCL signal after a repeated START condition and after an acknowledge bit	$20 + 0.1C_B$	300	ns
t_{SCL-F}	Fall time of SCL signal	$20 + 0.1C_B$	300	ns
t_{SDA-R}	Rise time of SDA signal	$20 + 0.1C_B$	300	ns
t_{SDA-F}	Fall time of SDA signal	$20 + 0.1C_B$	300	ns
t_{P-SU}	Setup time for STOP condition	600		ns
t_{SP}	Pulse width of spike suppressed		50	ns

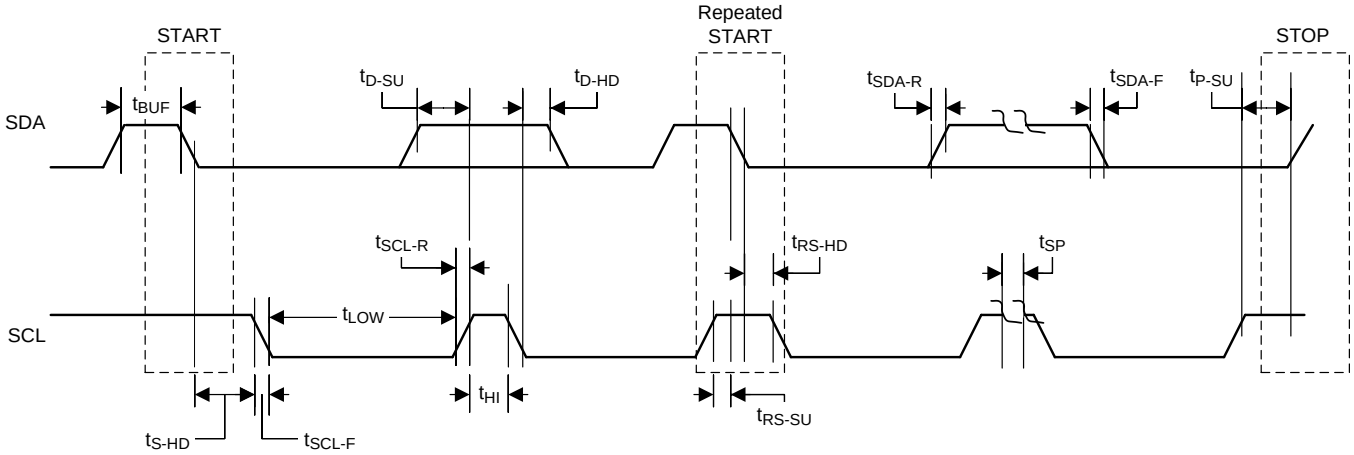


Figure 23. I²C Communication Port Timing Diagram

7.11 $\overline{\text{SPK\_MUTE}}$ Timing

		MIN	MAX	UNIT
t_r	Rise time		20	ns
t_f	Fall time		20	ns

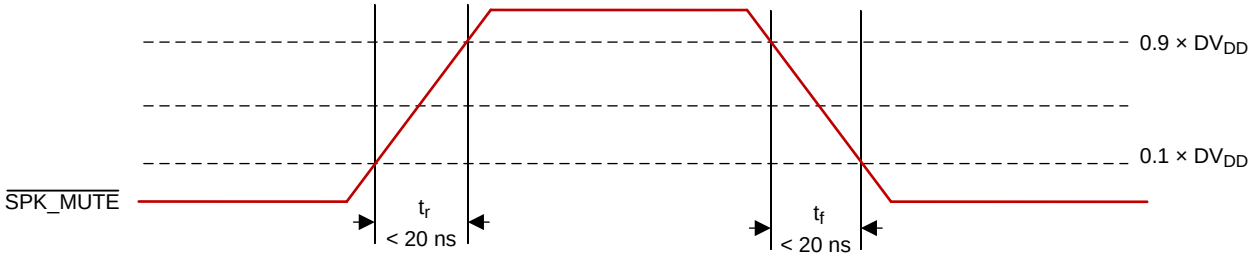


Figure 24. $\overline{\text{SPK\_MUTE}}$ Timing Diagram for Soft Mute Operation via Hardware Pin

7.12 Power Dissipation

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
7.4	20	384	Idle	4	21.3	35	0.273
				6	21.33	35	0.273
				8	21.3	35	0.273
			Mute	4	21.33	35	0.273
				6	21.34	35	0.273
				8	21.36	35	0.274
			Standby	4	2.08	17	0.071
				6	2.11	17	0.072
				8	2.17	17	0.072
			Powerdown	4	2.03	1	0.018
				6	2.04	1	0.018
				8	2.06	1	0.019
		768	Idle	4	27.48	35	0.319
				6	27.49	35	0.319
				8	24.46	35	0.297
			Mute	4	27.5	35	0.319
				6	27.51	35	0.319
				8	27.52	35	0.319
			Standby	4	2.04	17	0.071
				6	2.08	17	0.071
				8	2.11	17	0.072
			Powerdown	4	2.06	1	0.019
				6	2.07	1	0.019
				8	2.08	1	0.019

(1) Mute: P0-R3-B0,B5 = 1
(2) Standby: P0-R2-B5 = 1
(3) P0-R2-B0 = 1
(4) I_{PVDD} refers to all current that flows through the PVDD supply for the DUT. Any other current sinks not directly related to the DUT current draw were removed.
(5) I_{DVDD} refers to all current that flows through the DVDD (3.3-V) supply for the DUT. Any other current sinks not directly related to the DUT current draw were removed.

Power Dissipation (continued)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
11.1	20	384	Idle	4	24.33	35	0.386
				6	24.32	35	0.385
				8	24.36	35	0.386
			Mute	4	24.36	35	0.386
				6	24.32	35	0.385
				8	24.37	35	0.386
			Standby	4	3.58	17	0.096
				6	3.57	17	0.096
				8	3.58	17	0.096
			Powerdown	4	3.52	1	0.042
				6	3.52	1	0.042
				8	3.54	1	0.043
		768	Idle	4	30.7	35	0.456
				6	30.65	35	0.456
				8	30.67	35	0.456
			Mute	4	3.072	35	0.150
				6	30.69	35	0.456
				8	30.69	35	0.456
			Standby	4	3.54	17	0.095
				6	3.54	17	0.095
				8	3.58	17	0.096
			Powerdown	4	3.53	1	0.042
				6	3.53	1	0.042
				8	3.55	1	0.043

Power Dissipation (continued)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
12	20	384	Idle	4	25.07	35	0.416
				6	25.08	35	0.416
				8	25.1	35	0.417
			Mute	4	25.12	35	0.417
				6	25.08	35	0.416
				8	25.11	35	0.417
			Standby	4	3.92	17	0.103
				6	3.93	17	0.103
				8	3.94	17	0.103
			Powerdown	4	3.87	1	0.050
				6	3.85	1	0.050
				8	3.87	1	0.050
		768	Idle	4	31.31	35	0.491
				6	31.29	35	0.491
				8	31.31	35	0.491
			Mute	4	31.31	35	0.491
				6	31.33	35	0.491
				8	31.32	35	0.491
			Standby	4	3.88	17	0.103
				6	3.9	17	0.103
				8	3.91	17	0.103
			Powerdown	4	3.89	1	0.050
				6	3.91	1	0.050
				8	3.88	1	0.050

Power Dissipation (continued)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
15	26	384	Idle	4	27.94	35	0.535
				6	27.91	35	0.534
				8	27.75	35	0.532
			Mute	4	27.98	35	0.535
				6	27.94	35	0.535
				8	27.88	35	0.534
			Standby	4	5.09	17	0.132
				6	5.12	17	0.133
				8	5.19	17	0.134
			Powerdown	4	5.02	1	0.079
				6	5.06	1	0.079
				8	5.14	1	0.080
		768	Idle	4	33.05	35	0.611
				6	33.03	35	0.611
				8	33.08	35	0.612
			Mute	4	33.03	35	0.611
				6	33.04	35	0.611
				8	33.05	35	0.611
			Standby	4	5.07	17	0.132
				6	5.09	17	0.132
				8	5.14	17	0.133
			Powerdown	4	5.02	1	0.079
				6	5.04	1	0.079
				8	5.09	1	0.080

Power Dissipation (continued)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
19.6	26	384	Idle	4	32.27	35	0.748
				6	32.19	35	0.746
				8	32.08	35	0.744
			Mute	4	32.27	35	0.748
				6	32.24	35	0.747
				8	32.22	35	0.747
			Standby	4	6.95	17	0.192
				6	6.93	17	0.192
				8	7	17	0.193
			Powerdown	4	6.89	1	0.138
				6	6.9	1	0.139
				8	6.96	1	0.140
		768	Idle	4	34.99	35	0.801
				6	34.95	35	0.801
				8	34.97	35	0.801
			Mute	4	34.96	35	0.801
				6	34.98	35	0.801
				8	34.96	35	0.801
			Standby	4	6.93	17	0.192
				6	6.93	17	0.192
				8	6.98	17	0.193
			Powerdown	4	6.84	1	0.137
				6	6.89	1	0.138
				8	6.9	1	0.139

Power Dissipation (continued)

V_{PVDD} (V)	SPK_GAIN (1)(2)(3) (dBV)	f_{SPK_AMP} (kHz)	STATE OF OPERATION	R_{SPK} (Ω)	I_{PVDD} (4) (mA)	I_{DVDD} (5) (mA)	P_{DISS} (W)
24	26	384	Idle	4	36.93	35	1.002
				6	36.87	35	1.000
				8	36.77	35	0.998
			Mute	4	36.94	35	1.002
				6	36.89	35	1.001
				8	36.85	35	1.000
			Standby	4	8.73	17	0.266
				6	8.72	17	0.265
				8	8.71	17	0.265
			Powerdown	4	8.64	1	0.211
				6	8.66	1	0.211
				8	8.69	1	0.212
		768	Idle	4	36.84	35	1.000
				6	36.86	35	1.000
				8	36.83	35	0.999
			Mute	4	36.85	35	1.000
				6	36.84	35	1.000
				8	36.82	35	0.999
			Standby	4	8.66	17	0.264
				6	8.68	17	0.264
				8	8.71	17	0.265
			Powerdown	4	8.63	1	0.210
				6	8.64	1	0.211
				8	8.65	1	0.211

7.13 Typical Performance Plots for the TAS5754M

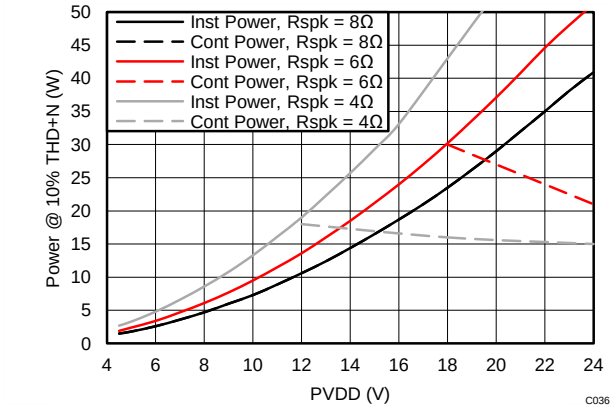
All performance plots were taken using the TAS5754M-56MEVM at room temperature, unless otherwise noted. The term "Traditional LC filter" refers to the output filter that is present by default on the EVM. For "Filterless" measurements, the on-board LC filter was removed and an Audio Precision AUX-025 measurement filter was used to take the measurements.

Table 1. Quick Reference Table

OUTPUT CONFIG	PLOT TITLE	PLOT NUMBER
BTL	Figure 25. Output Power vs PVDD	C036
	Figure 26. THD+N vs Frequency, V_{PVDD} = 12 V	C034
	Figure 27. THD+N vs Frequency, V_{PVDD} = 15 V	C002
	Figure 28. THD+N vs Frequency, V_{PVDD} = 18 V	C037
	Figure 29. THD+N vs Frequency, V_{PVDD} = 24 V	C003
	Figure 30. THD+N vs Power, V_{PVDD} = 12 V	C035
	Figure 31. THD+N vs Power, V_{PVDD} = 15 V	C004
	Figure 32. THD+N vs Power, V_{PVDD} = 18 V	C038
	Figure 33. THD+N vs Power, V_{PVDD} = 24 V	C005
	Figure 34. Idle Channel Noise vs PVDD	C006
	Figure 35. Efficiency vs Output Power	C007
	Figure 36. Idle Current Draw (Filterless) vs PVDD	C013
	Figure 37. Idle Current Draw (Traditional LC Filter) vs PVDD	C015
	Figure 38. Crosstalk vs. Frequency	C008
	Figure 39. PVDD PSRR vs Frequency	C009
	Figure 40. DVDD PSRR vs Frequency	C010
	Figure 41. AVDD PSRR vs Frequency	C011
	Figure 42. CPVDD PSRR vs Frequency	C012
	Figure 43. Powerdown Current Draw vs PVDD	C014
PBTL	Figure 44. Output Power vs PVDD	C039
	Figure 45. THD+N vs Frequency, V_{PVDD} = 12 V	C017
	Figure 46. THD+N vs Frequency, V_{PVDD} = 15 V	C018
	Figure 47. THD+N vs Frequency, V_{PVDD} = 18 V	C019
	Figure 48. THD+N vs Frequency, V_{PVDD} = 24 V	C020
	Figure 49. THD+N vs Power, V_{PVDD} = 12 V	C021
	Figure 50. THD+N vs Power, V_{PVDD} = 15 V	C022
	Figure 51. THD+N vs Power, V_{PVDD} = 18 V	C023
	Figure 52. THD+N vs Power, V_{PVDD} = 24 V	C024
	Figure 53. Idle Channel Noise vs PVDD	C025
	Figure 54. Efficiency vs Output Power	C026
	Figure 55. Idle Current Draw (filterless) vs PVDD	C031
	Figure 56. Idle Current Draw (traditional LC filter) vs PVDD	C033
	Figure 57. PVDD PSRR vs Frequency	C027
	Figure 58. DVDD PSRR vs Frequency	C028
	Figure 59. AVDD PSRR vs Frequency	C029
	Figure 60. CPVDD PSRR vs Frequency	C030
	Figure 61. Powerdown Current Draw vs PVDD	C032

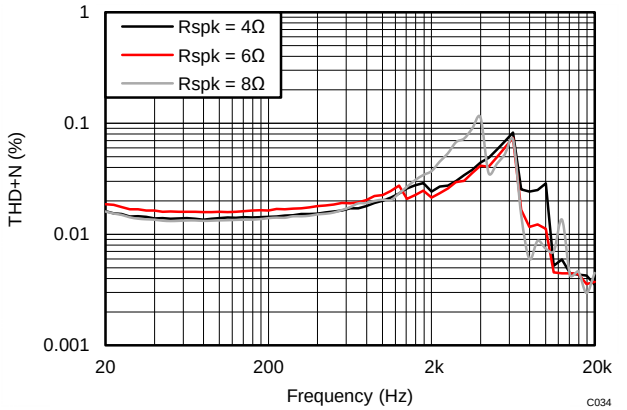
7.13.1 Bridge Tied Load (BTL) Configuration Curves

Return to Quick Reference Table.



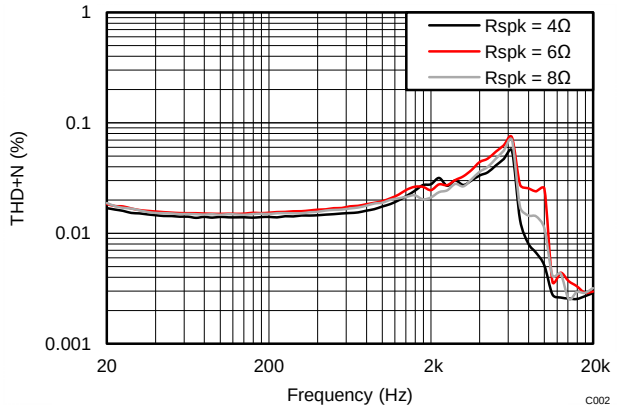
$A_{V(SPK\_AMP)}$ = 26dBV

Figure 25. Output Power vs PVDD – BTL



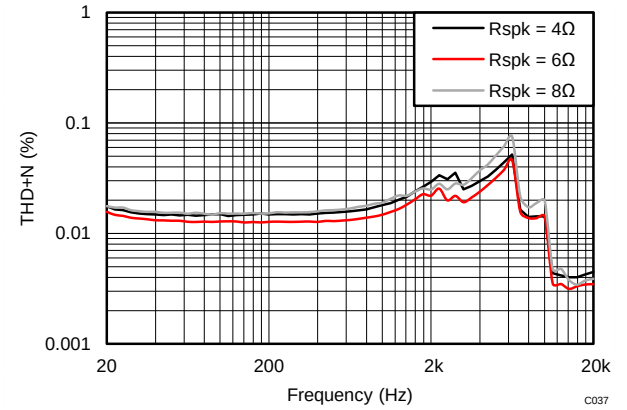
$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 12V

Figure 26. THD+N vs Frequency – BTL



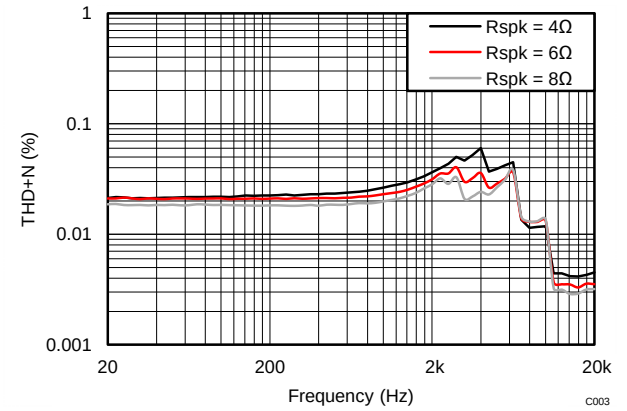
$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 15V

Figure 27. THD+N vs Frequency – BTL



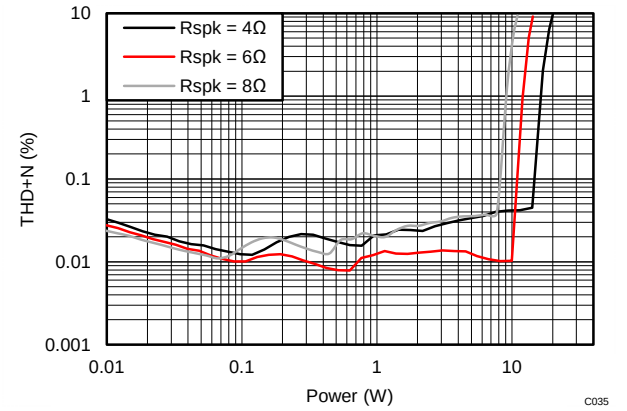
$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 18V

Figure 28. THD+N vs Frequency – BTL



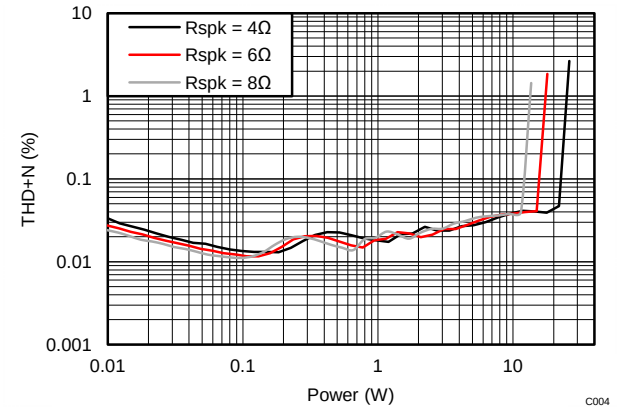
$A_{V(SPK\_AMP)}$ = 26dBV P_O = 1W V_{PVDD} = 24V

Figure 29. THD+N vs Frequency – BTL



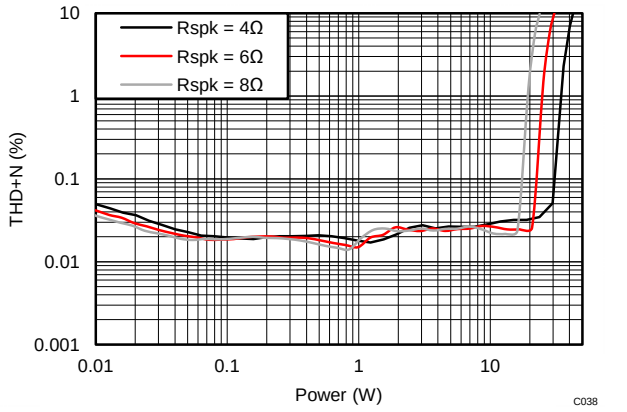
$A_{V(SPK\_AMP)}$ = 20dBV Input Signal = 1kHz Sine V_{PVDD} = 12V

Figure 30. THD + N vs Power – BTL



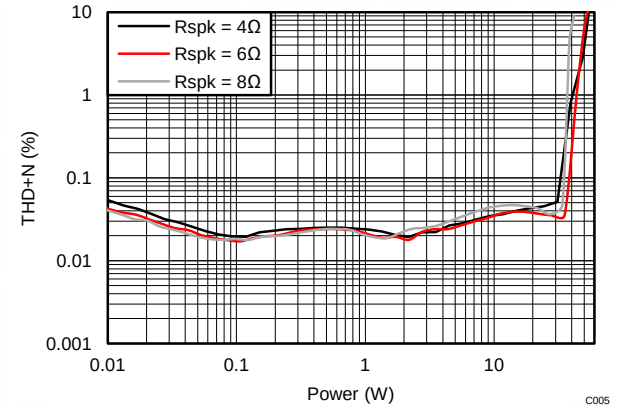
$A_{V(SPK\_AMP)}$ = 20dBV | Input Signal = 1kHz Sine | V_{PVDD} = 15V

Figure 31. THD + N vs Power – BTL



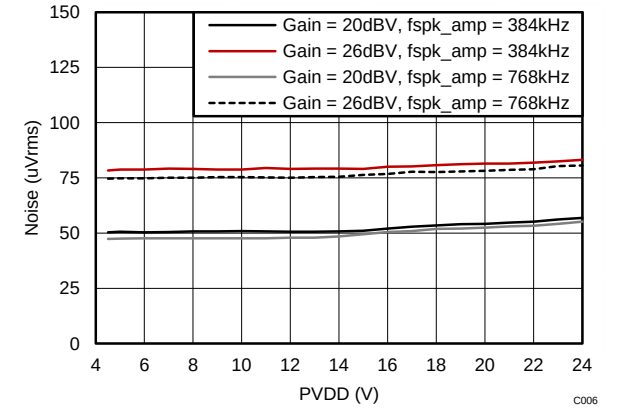
$A_{V(SPK\_AMP)}$ = 26dBV | Input Signal = 1kHz Sine | V_{PVDD} = 18V

Figure 32. THD + N vs Power – BTL



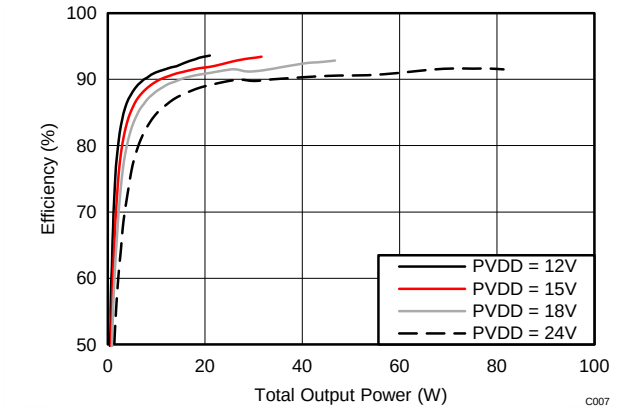
$A_{V(SPK\_AMP)}$ = 26dBV | P_O = 1W | V_{PVDD} = 24V

Figure 33. THD + N vs Power – BTL



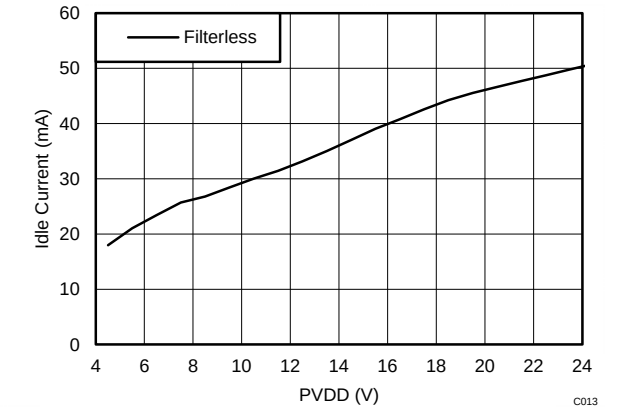
$A_{V(SPK\_AMP)}$ = 20dBV | f_{SPK_AMP} = 384kHz | R_{SPK} = 8Ω

Figure 34. Idle Channel Noise vs PVDD – BTL



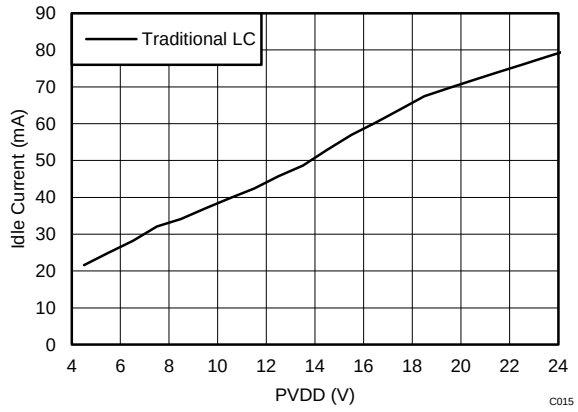
R_{SPK} = 8 Ω

Figure 35. Efficiency vs Output Power – BTL



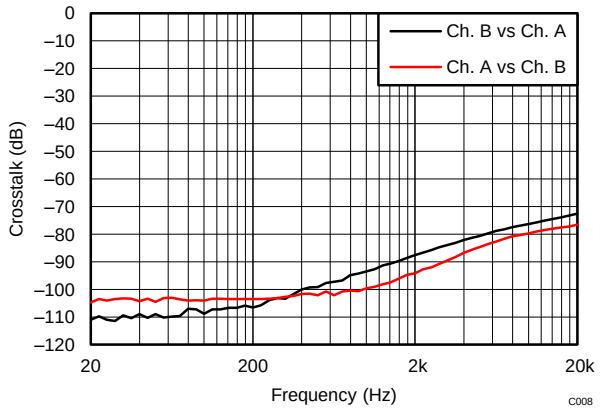
f_{SPK_AMP} = 768kHz | R_{SPK} = 8Ω

Figure 36. Idle Current Draw (Filterless) vs V_{PVDD}– BTL



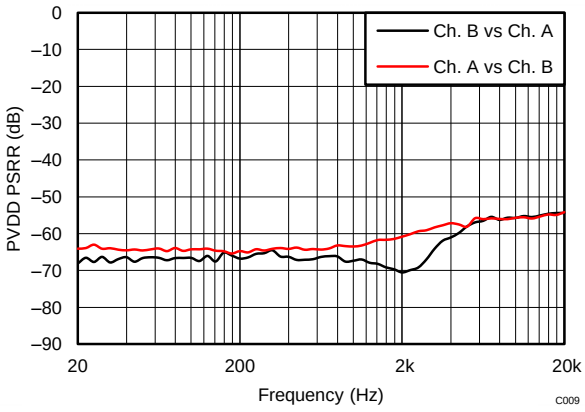
f_{SPK_AMP} = 768kHz R_{SPK} = 8Ω

Figure 37. Idle Current Draw (Traditional LC Filter) vs PVDD – BTL



$A_{V(SPK\_AMP)}$ = 26dBV Sine Input V_{PVDD} = 24V

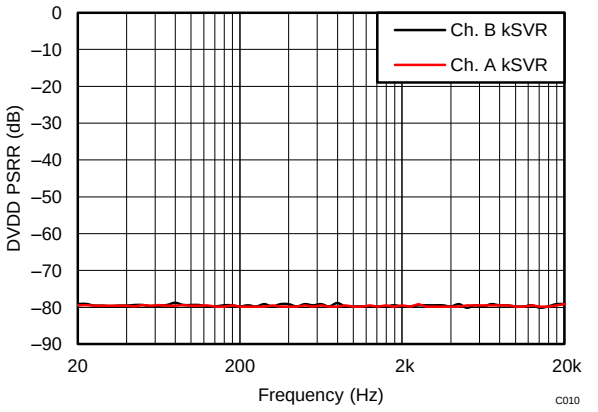
Figure 38. Crosstalk vs Frequency – BTL



$A_{V(SPK\_AMP)}$ = 26dBV Sine Input Supply Noise = 250mV

V_{PVDD} = 24V

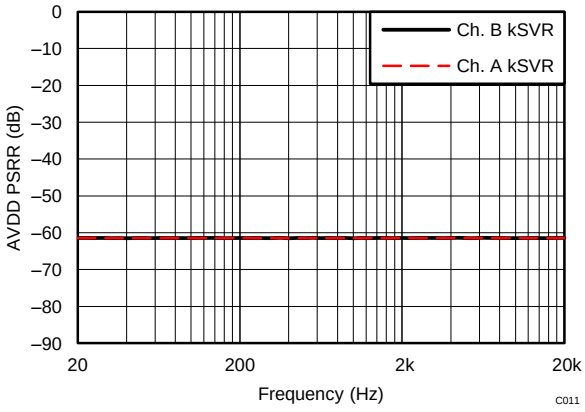
Figure 39. PVDD PSRR vs Frequency – BTL



$A_{V(SPK\_AMP)}$ = 26dBV R_{SPK} = 8Ω Supply Noise = 250mV

V_{PVDD} = 24V

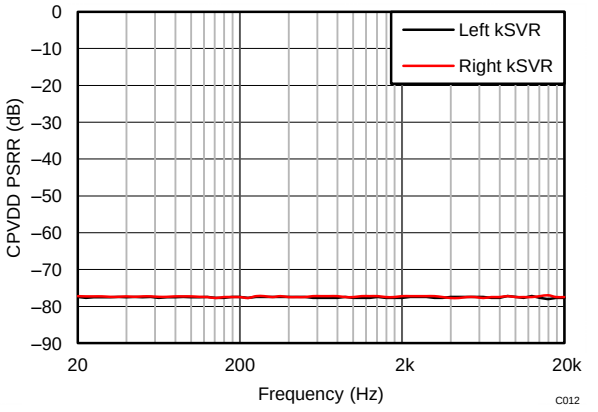
Figure 40. DVDD PSRR vs Frequency – BTL



$A_{V(SPK\_AMP)}$ = 26dBV R_{SPK} = 8Ω Supply Noise = 250mV

V_{PVDD} = 24V

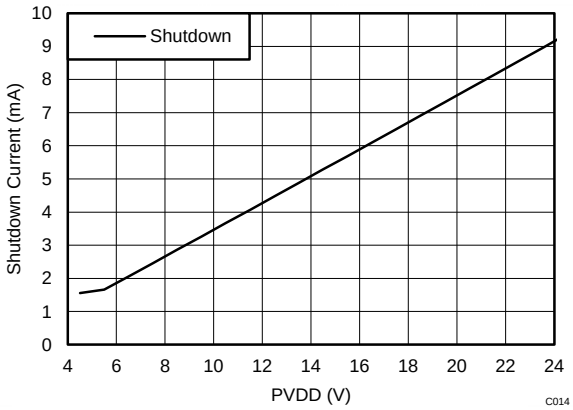
Figure 41. AVDD PSRR vs Frequency – BTL



$A_{V(SPK\_AMP)}$ = 26dBV Sine Input Supply Noise = 250mV

V_{PVDD} = 24V

Figure 42. CPVDD PSRR vs Frequency – BTL



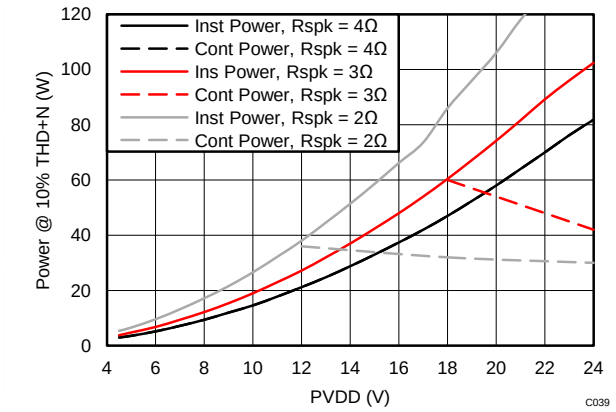
$A_{V(SPK\_AMP)}$ = 26dBV

f_{SPK_AMP} = 786kHz

Figure 43. Powerdown Current Draw vs PVDD – BTL

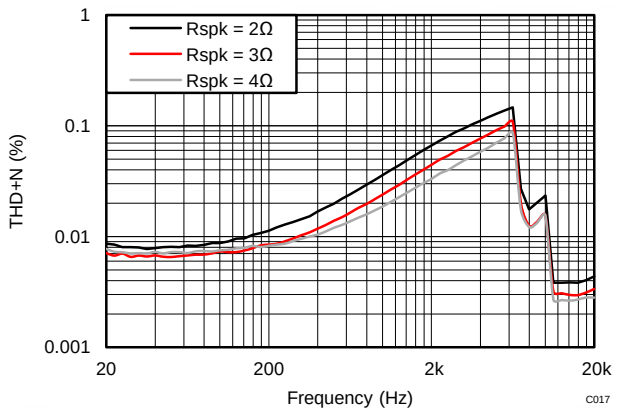
7.13.2 Parallel Bridge Tied Load (PBTL) Configuration

Return to Quick Reference Table.



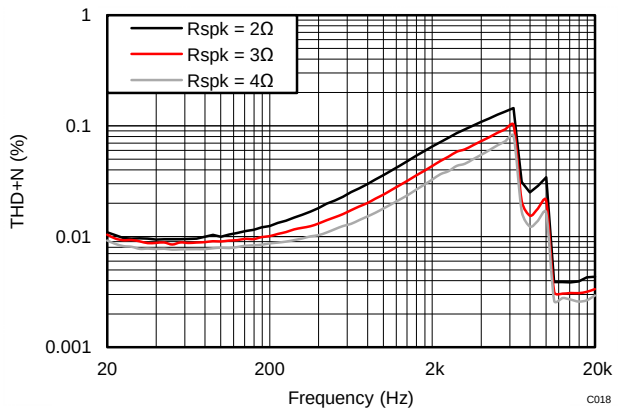
$A_{V(SPK\_AMP)}$ = 26dBV Measured on TAS5754/6 EVM

Figure 44. Output Power vs PVDD – PBTL



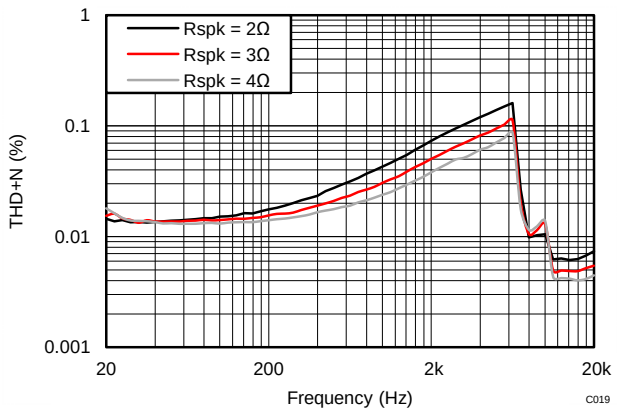
$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 12V

Figure 45. THD+N vs Frequency – PBTL



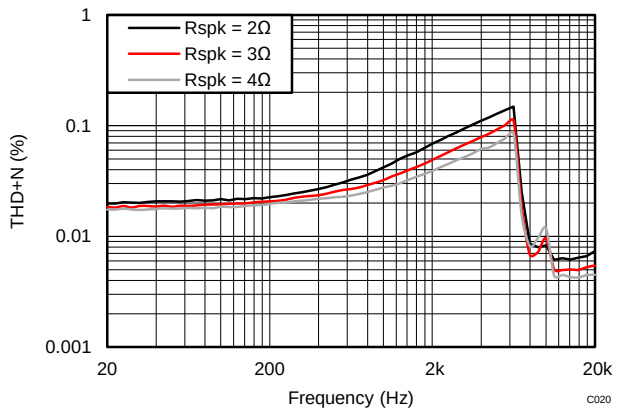
$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 15V

Figure 46. THD+N vs Frequency – PBTL



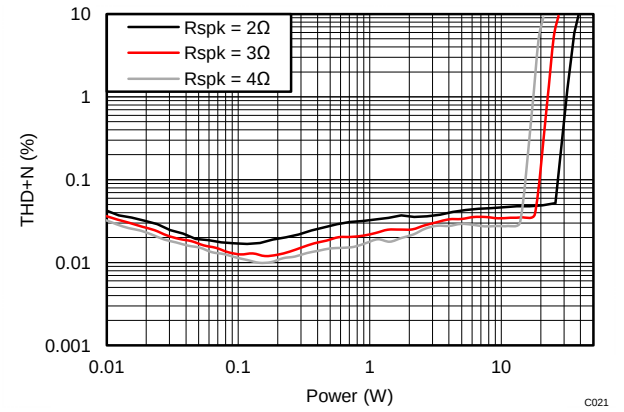
$A_{V(SPK\_AMP)}$ = 26dBV P_O = 1W V_{PVDD} = 18V

Figure 47. THD+N vs Frequency – PBTL



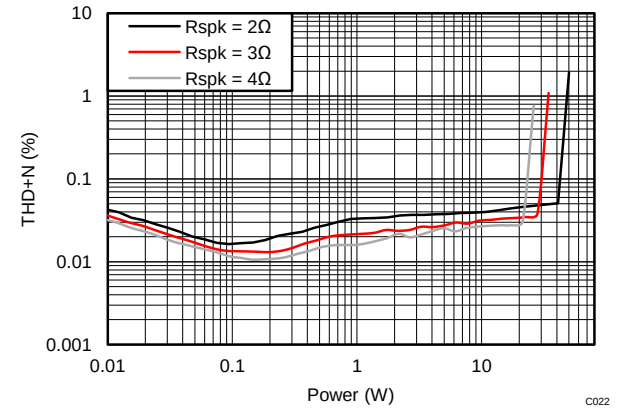
$A_{V(SPK\_AMP)}$ = 26dBV P_O = 1W V_{PVDD} = 24V

Figure 48. THD+N vs Frequency – PBTL



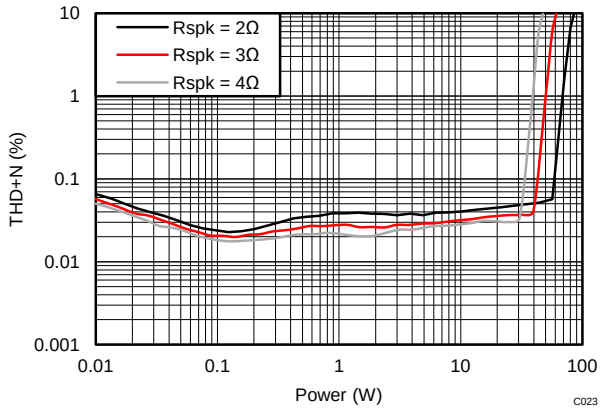
$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 12V

Figure 49. THD+N vs Power – PBTL



$A_{V(SPK\_AMP)}$ = 20dBV P_O = 1W V_{PVDD} = 15V

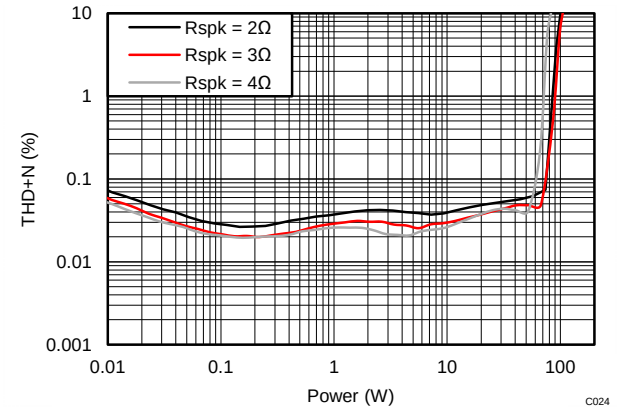
Figure 50. THD+N vs Power – PBTL



$A_{V(SPK\_AMP)}$ = 20dBV Input Signal = 1kHz Sine P_O = 1W

V_{PVDD} = 18V

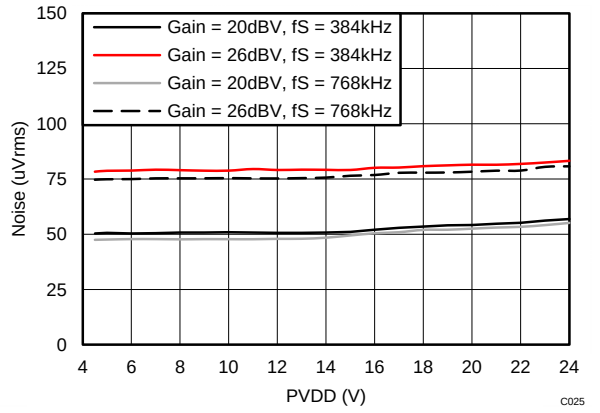
Figure 51. THD+N vs Power – PBTL



$A_{V(SPK\_AMP)}$ = 20dBV Input Signal = 1kHz Sine P_O = 1W

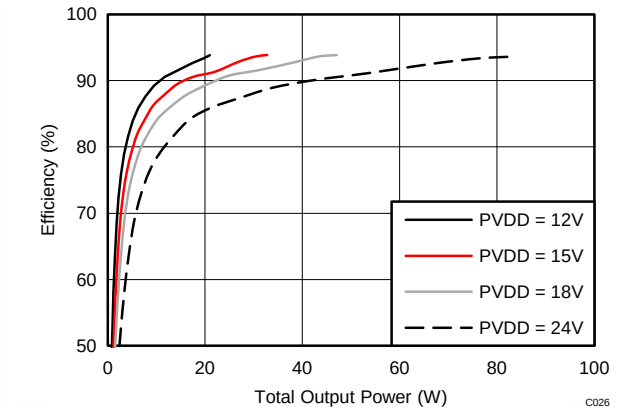
V_{PVDD} = 24V

Figure 52. THD+N vs Power – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV I_{LOAD} = xA V_{PVDD} = 18V

Figure 53. Idle Channel Noise vs PVDD – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV I_{LOAD} = xA V_{PVDD} = 24V

Figure 54. Efficiency vs Output Power – PBTL

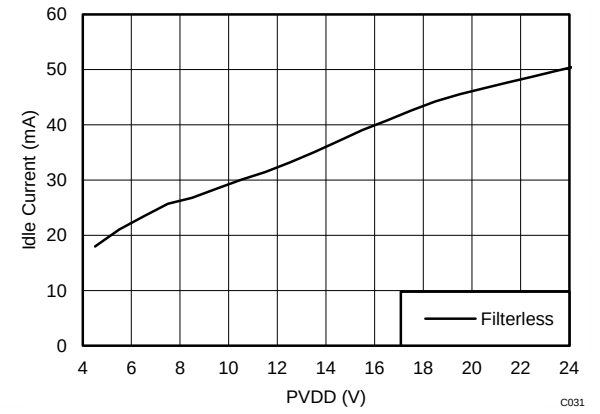


Figure 55. Idle Current Draw (Filterless) vs PVDD – PBTL

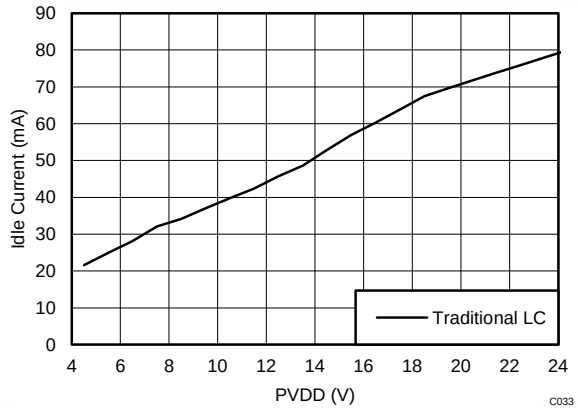
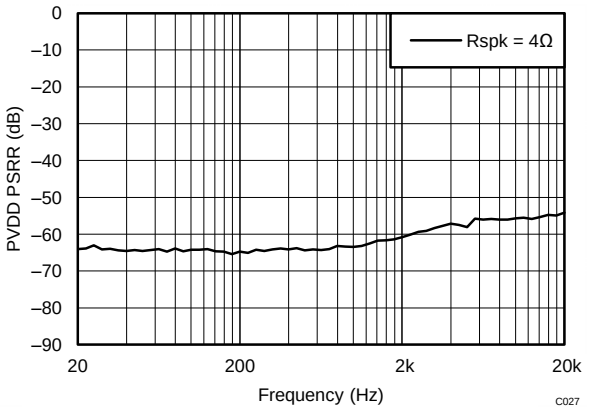
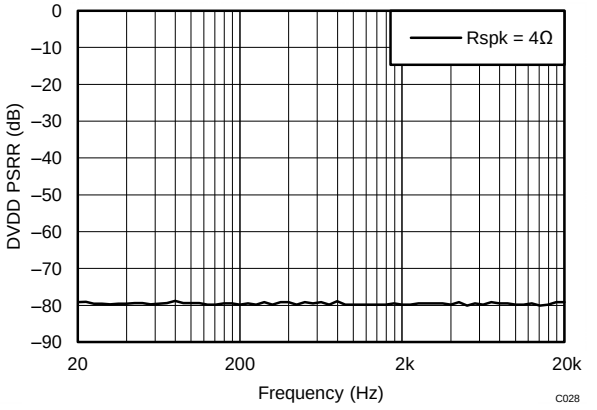


Figure 56. Idle Current Draw (Traditional LC filter) vs PVDD – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV Sine Input V_{PVDD} = 24V

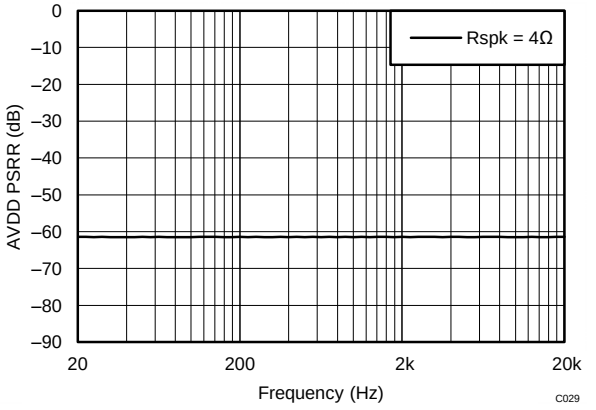
Figure 57. PVDD PSRR vs Frequency – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV R_{SPK} = 8Ω Supply Noise = 250mV

V_{PVDD} = 24V

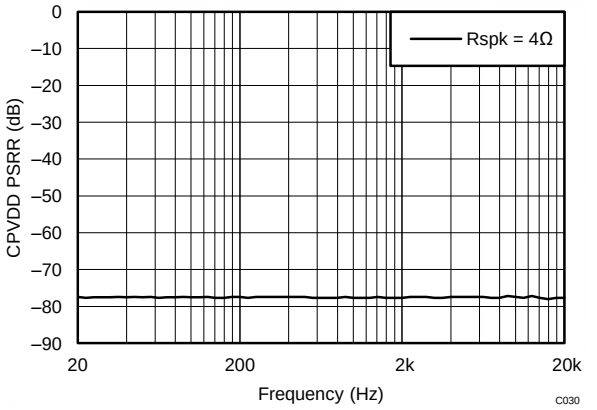
Figure 58. DVDD PSRR vs Frequency – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV R_{SPK} = 8Ω Supply Noise = 250mV

V_{PVDD} = 24V

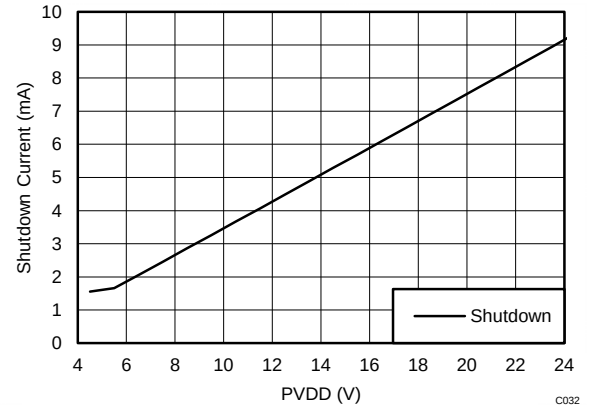
Figure 59. AVDD PSRR vs Frequency – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV Sine Input Supply Noise = 250mV

V_{PVDD} = 24V

Figure 60. CPVDD PSRR vs Frequency – PBTL



$A_{V(SPK\_AMP)}$ = 26dBV f_{SPK_AMP} = 786kHz

Figure 61. Powerdown Current Draw vs PVDD – PBTL

8 Detailed Description

8.1 Overview

The TAS5754M device integrates 4 main building blocks together into a single cohesive device that maximizes sound quality, flexibility, and ease of use. These are shown in the list below:

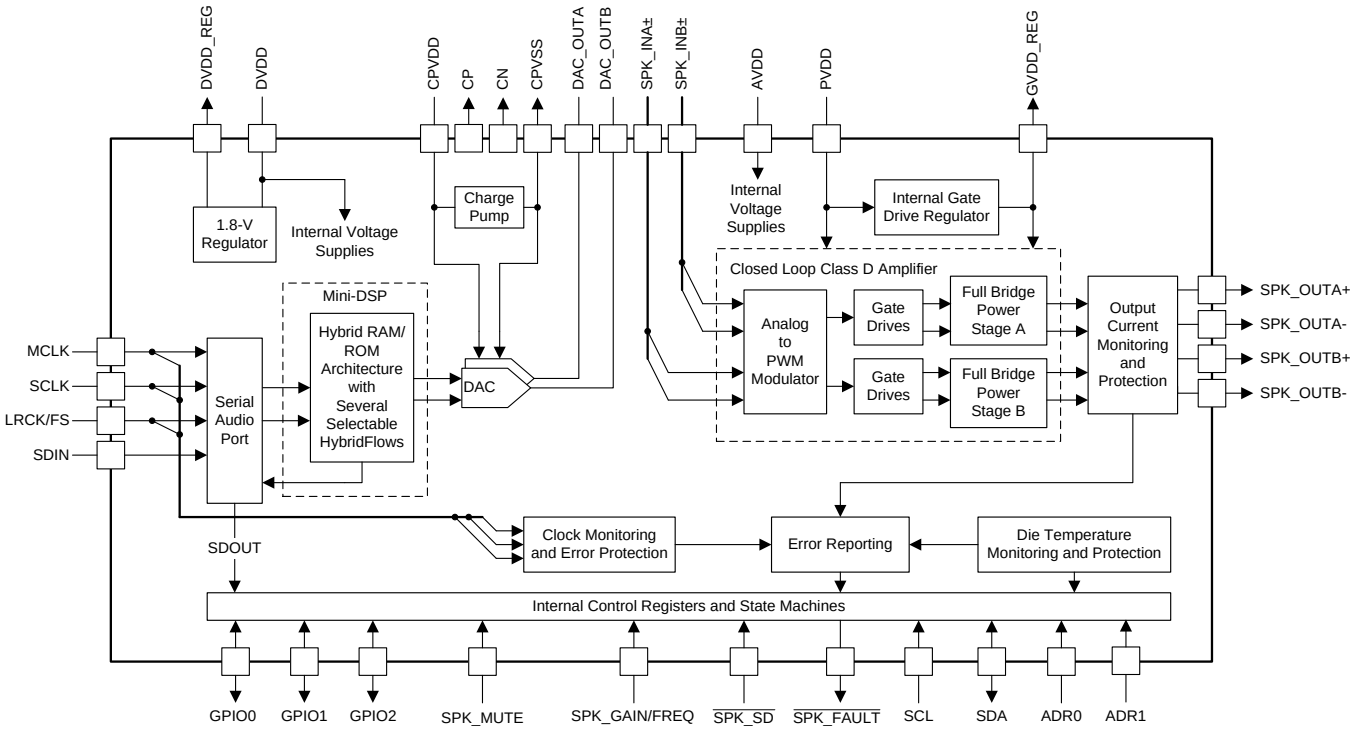
1. A stereo Audio DAC, boasting a strong Burr-Brown heritage with a highly flexible serial audio port.
2. A miniDSP audio processing core with HybridFlow architecture, which provides an increase in flexibility over a fixed-function ROM device with faster download time than a fully programmable device
3. A flexible closed-loop amplifier capable of operating in stereo or mono, at several different switching frequencies, and with a variety of output voltages and loads.
4. An I^2C control port for communication with the device

The device requires only two power supplies for proper operation. A DVDD supply is needed to power the low-voltage digital and analog circuitry. Another supply, called PVDD, is needed to provide power to the output stage of the audio amplifier. The operating range for these supplies is shown in the *Recommended Operating Conditions* table.

Communication with the device is accomplished via the I^2C control port. A speaker amplifier fault line is also provided to notify a system controller of the occurrence of an over-temperature, over-current, over-voltage, under-voltage, or DC error in the speaker amplifier. There are three digital GPIO pins that are available for use by the HybridFlows. One popular use of the GPIO lines is to provide a Serial Audio Output from the device (SDOUT). HybridFlows which provide an SDOUT customarily present that signal on GPIO2, although this configuration can be changed via the I^2C control port. The register space in the control port spans several pages to accommodate some static controls which maintain their functionality across HybridFlows, as well as controls that are determined by the HybridFlow used.

The MiniDSP audio processing core, featuring a HybridFlow architecture, allows the selection of a configurable DSP program called a *HybridFlow* from a list of available HybridFlows. A hybrid flow combines audio processing blocks, many of which that are built in the ROM portion of the device, together in a single payload. The PurePath Console GUI provides a means by which to select the HybridFlow and manipulate the controls associated with that HybridFlow.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-on-Reset (POR) Function

The TAS5754M device has a power-on reset function. This feature resets all of the registers to their default configuration as the device is powering up. When the low-voltage power supply used to power DVDD, AVDD, and CPVDD exceeds the POR threshold, the device holds sets all of the internal registers to their default values and holds them there until it receives valid MCLK, SCLK, and LRCK/FS toggling for a period of approximately 4 ms. After the toggling period has passed, the internal reset of the registers is removed and the registers can be programmed via the I^2C Control Port.

8.3.2 Device Clocking

The TAS5754M devices have flexible systems for clocking. Internally, the device requires a number of clocks, mostly at related clock rates to function correctly. All of these clocks can be derived from the Serial Audio Interface in one form or another.

Feature Description (continued)

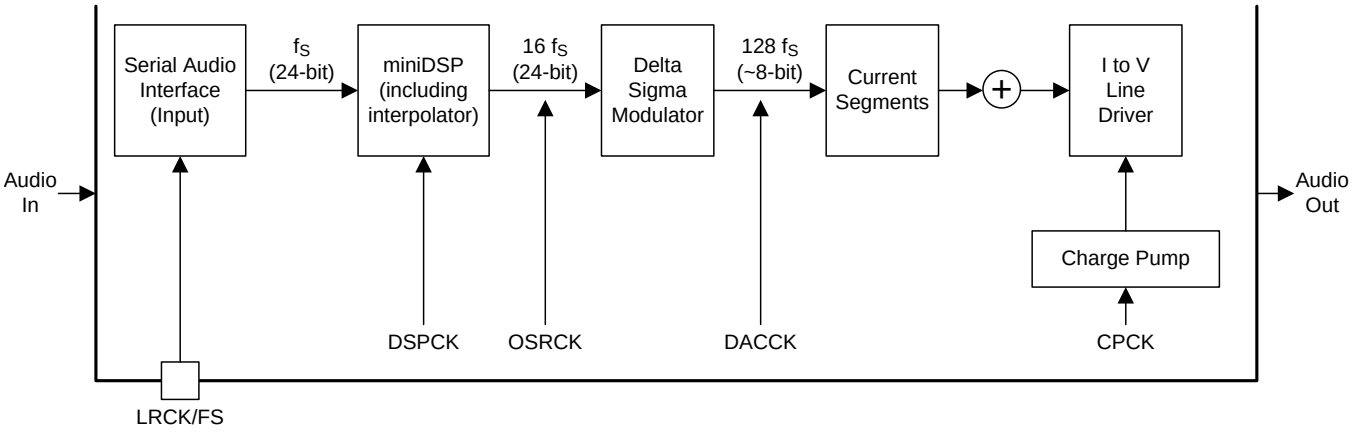


Figure 62. Audio Flow with Respective Clocks

As shown in Figure 62 the basic data flow at basic sample rate (f_S). Once the data is brought into the serial audio interface, it is processed, interpolated and modulated to 128 × f_S before arriving at the current segments for the final digital to analog conversion.

The clock tree is shown in Figure 63.

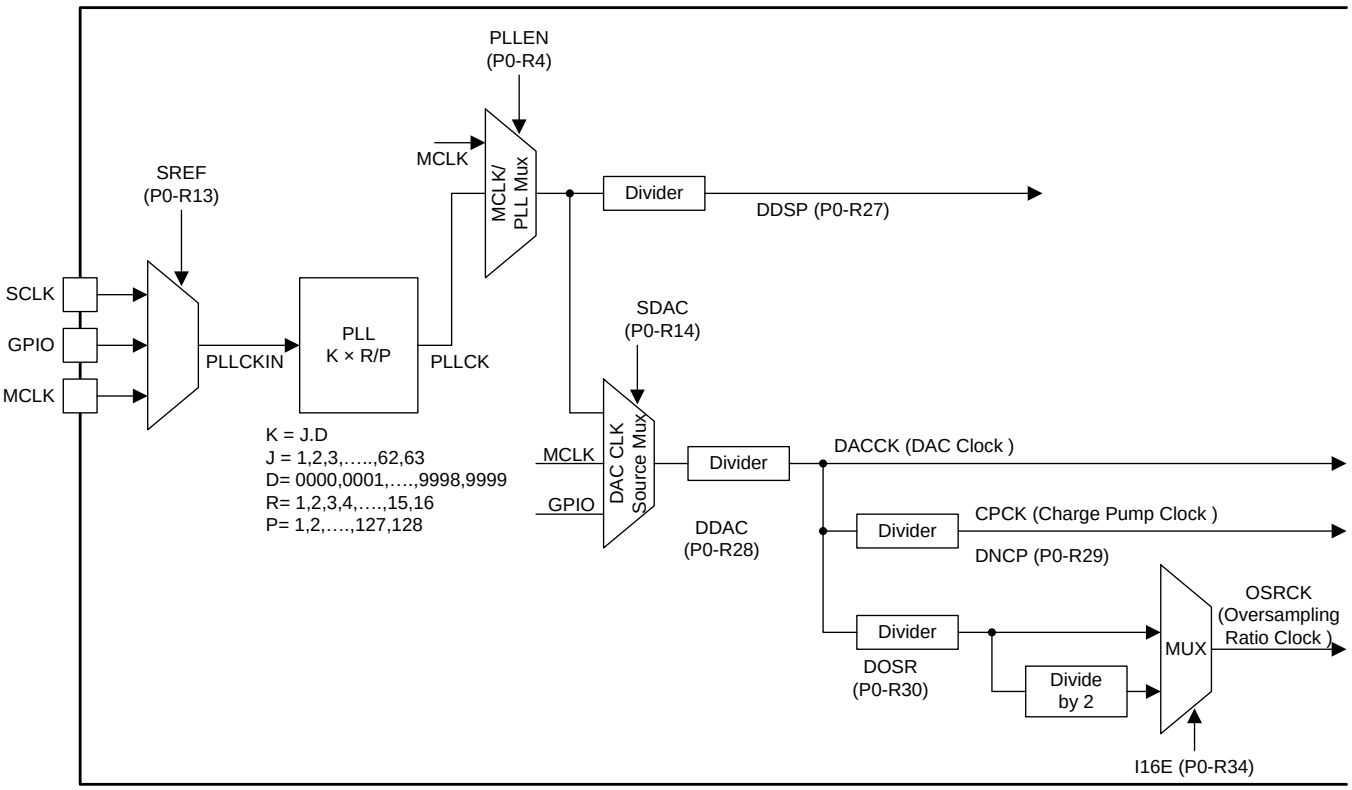


Figure 63. TAS5754M Clock Distribution Tree

The Serial Audio Interface typically has 4 connection pins

1. MLCK (System Master Clock),
2. SLCK (Bit Clock)
3. LRCK/FS (Left Right Word Clock and Frame Sync)

Feature Description (continued)

4. SDIN (note that this is the input data. The output date, SDOUT, is presented on one of the GPIO pins. See Serial Data Output)

The device has an internal PLL that is used to take either MLCK or SLCK and create the higher rate clocks required by the and the DAC clock.

In situations where the highest audio performance is required, it's suggested that the MLCK is brought to the device, along with SLCK and LRCK/FS. The device should be configured so that the PLL is only providing a clock source to the DSP. All other clocks are then be a division of the incoming MLCK. This is done by setting DAC CLK Source Mux (SDAC in the diagram above) to use MLCK as a source, rather than the output of the MLCK/PLL Mux.

8.3.3 Serial Audio Port

8.3.3.1 Clock Master Mode from Audio Rate Master Clock

In Master Mode, the device generates bit clock and left-right and frame sync clock and outputs them on the appropriate pins. To configure the device in this mode, first put the device into reset, then use registers SLCKO and LRKO (P0-R9). Then reset the LRCK/FS and SCLK divider counters using bits RSLCK and RLRK (P0-R12). Finally, exit reset.

Figure 64 shows a simplified serial port clock tree for the device in master mode.

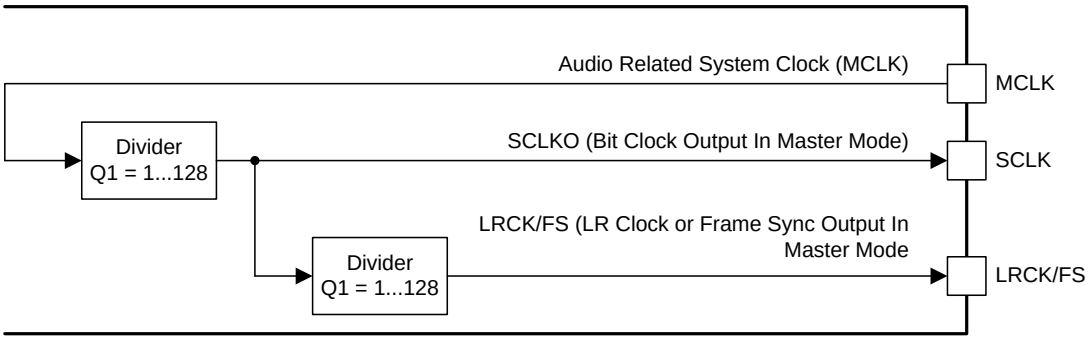


Figure 64. Simplified Clock Tree for MLCK Sourced Master Mode

In master mode, MLCK is an input and SCLK and LRCK/FS are outputs. SCLK and LRCK/FS are integer divisions of MLCK. Master mode with a non-audio rate master clock source will require external GPIO's to use the PLL in standalone mode. The PLL needs to be configured to ensure that the on-chip processor can be driven at its maximum clock rate. This mode of operation is described in the *Clock Master from a Non-Audio Rate Master Clock* section.

When used with Audio Rate Master Clocks, the register changes that need to be done include switching the device into master mode, and setting the divider ratio. An example of this mode of operations is using 24.576 MCLK as a master clock source and driving the SCLK and LRCK/FS with integer dividers to create 48 kHz. In this mode, the DAC section of the device is also running from the PLL output. The TAS5754M device is able to meet the specified audio performance while using the internal PLL. However, using the MCLK CMOS oscillator source will have less jitter than the PLL.

To switch the DAC clocks (SDAC in the Figure 63) the following registers should be modified

- Clock Tree Flex Mode (P253-R63 and P253-R64)
- DAC and OSR Source Clock Register (P0-R14). Set to 0x30 (MLCK input, and OSR is set to whatever the DAC source is)
- The DAC clock divider should be $16f_S$.
  - 16 × 48 kHz = 768 kHz
  - 24.576 MHz (MLCK in) / 768 kHz = 32
  - Therefore, the divide ratio for register DDAC (P0-R28) should be set to 32. The register mapping gives 0x00 = 1, so 32 must be converter to 0x1F (31dec).

Feature Description (continued)

8.3.3.2 Clock Master from a Non-Audio Rate Master Clock

The classic example here is running 12-MHz Master clock for a 48-kHz sampling system. Given the clock tree for the device (shown in Figure 63), a non-audio clock rate cannot be brought into the MLCK to the PLL in master mode. Therefore, the PLL source must be configured to be a GPIO pin, and the output brought back into another GPIO pin.

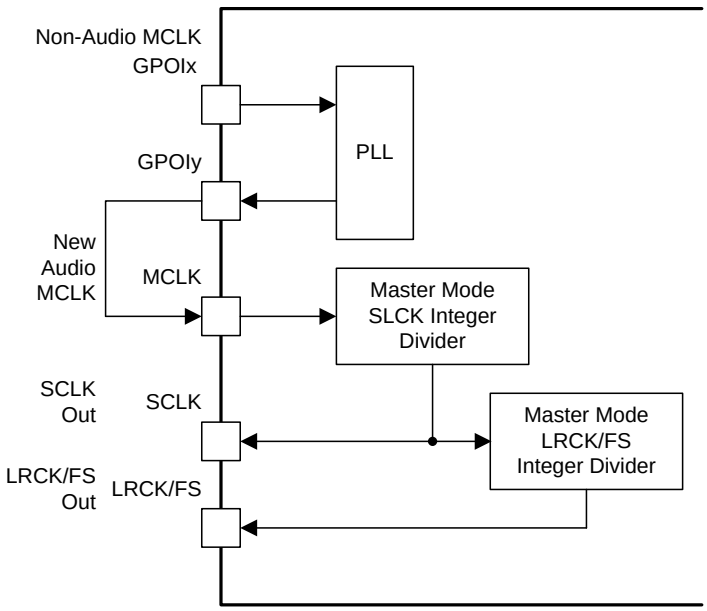


Figure 65. Generating Audio Clocks Using Non-Audio Clock Sources

The clock flow through the system is shown above. The newly generated MLCK must be brought out of the device on a GPIO pin, then brought into the MLCK pin for integer division to create SCLK and LRCK/FS outputs.

NOTE

Pull-up resistors should be used on SCLK and LRCK/FS in this mode to ensure the device remains out of sleep mode.

8.3.3.3 Clock Slave Mode with 4-Wire Operation (SCLK, MCLK, LRCK/FS, SDIN)

The TAS5754M device requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the MLCK input and supports up to 50 MHz. The TAS5754M device system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 8 kHz, 16 kHz, (32 kHz - 44.1 kHz - 48kHz), (88.2 kHz - 96 kHz), and (176.4 kHz - 192 kHz) are supported.

NOTE

Values in the parentheses are grouped when detected, e.g. 88.2 kHz and 96 kHz are detected as *double rate*, 32 kHz, 44.1 kHz and 48 kHz are detected as *single rate*, etc.

In the presence of a valid bit MCLK, SCLK and LRCK/FS, the device automatically configures the clock tree and PLL to drive the miniDSP as required.

The sampling frequency detector sets the clock for the digital filter, Delta Sigma Modulator (DSM) and the Negative Charge Pump (NCP) automatically. Table 2 shows examples of system clock frequencies for common audio sampling rates.

Feature Description (continued)

MLCK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are supported by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCK/FS and SLCK, from a non-audio related clock (for example, using a setting of 12 MHz to generate 44.1 kHz (LRCK/FS) and 2.8224 MHz (SLCK)).

shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise. For MCLK timing requirements, refer to the Serial Audio Port Timing – Master Mode section.

Table 2. System Master Clock Inputs for Audio Related Clocks

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{MLCK}) (MHz)					
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S
8 kHz	See note(1)	1.0240(2)	1.5360(2)	2.0480	3.0720	4.0960
16 kHz		2.0480(2)	3.0720(2)	4.0960	6.1440	8.1920
32 kHz		4.0960(2)	6.1440(2)	8.1920	12.2880	16.3840
44.1 kHz		5.6488(2)	8.4672(2)	11.2896	16.9344	22.5792
48 kHz		6.1440(2)	9.2160(2)	12.2880	18.4320	24.5760
88.2 kHz		11.2896(2)	16.9344	22.5792	33.8688	45.1584
96 kHz		12.2880(2)	18.4320	24.5760	36.8640	49.1520
176.4 kHz		22.5792	33.8688	45.1584	See note(1)	See note(1)
192 kHz		24.5760	36.8640	49.1520		

(1) This system clock rate is not supported for the given sampling frequency.
(2) This system clock rate is supported by PLL mode.

8.3.3.4 Clock Slave Mode with SLCK PLL to Generate Internal Clocks (3-Wire PCM)

8.3.3.4.1 Clock Generation using the PLL

The TAS5754M device supports a wide range of options to generate the required clocks as shown in Figure 63.

The clocks for the PLL require a source reference clock. This clock is sourced as the incoming SLCK or MLCK, a GPIO can also be used.

The source reference clock for the PLL reference clock is selected by programming the SRCREF value on P0-R13, B[6:4]. The TAS5754M device provides several programmable clock dividers to achieve a variety of sampling rates. See Figure 63.

If PLL functionality is not required, set the PLLEN value on P0-R4, B[0] to 0. In this situation, an external master clock is required.

Table 3. PLL Configuration Registers

CLOCK MULTIPLEXER	FUNCTION	BITS
SREF	PLL Reference	P0-R13, B[6:4]
DIVIDER	**FUNCTION**	**BITS**
DDSP	clock divider	P0-R27, B[6:0]
DSLCK	External SLCK Div	P0-R32, B[6:0]
DLRK	External LRCK/FS Div	P0-R33, B[7:0]

8.3.3.4.2 PLL Calculation

The TAS5754M device has an on-chip PLL with fractional multiplication to generate the clock frequency needed by the Digital Signal Processing blocks. The programmability of the PLL allows operation from a wide variety of clocks that may be available in the system. The PLL input (PLLCKIN) supports clock frequencies from 1 MHz to 50 MHz and is register programmable to enable generation of required sampling rates with fine precision.

The PLL is enabled by default. The PLL can be enabled by writing to P0-R4, B[0]. When the PLL is enabled, the PLL output clock PLLCK is given by Equation 1:

$$PLLCK = \frac{PLLCKIN \times R \times J.D}{P} \quad \text{or} \quad PLLCK = \frac{PLLCKIN \times R \times K}{P}$$

where

- R = 1, 2, 3,4, ... , 15, 16
- J = 4,5,6, . . . 63, and D = 0000, 0001, 0002, . . . 9999
- K = [J value].[D value]
- P = 1, 2, 3, ... 15 (1)

R, J, D, and P are programmable. J is the integer portion of K (the numbers to the left of the decimal point), while D is the fractional portion of K (the numbers to the right of the decimal point, assuming four digits of precision).

8.3.3.4.2.1 Examples:

- If K = 8.5, then J = 8, D = 5000
- If K = 7.12, then J = 7, D = 1200
- If K = 14.03, then J = 14, D = 0300
- If K = 6.0004, then J = 6, D = 0004

When the PLL is enabled and D = 0000, **the following conditions must be satisfied:**

- 1 MHz ≤ (PLLCKIN / P) ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 1 ≤ J ≤ 63

When the PLL is enabled and D ≠ 0000, **the following conditions must be satisfied:**

- 6.667 MHz ≤ PLLCLKIN / P ≤ 20 MHz
- 64 MHz ≤ (PLLCKIN x K x R / P) ≤ 100 MHz
- 4 ≤ J ≤ 11
- R = 1

When the PLL is enabled,

- f_S = (PLLCLKIN × K × R) / (2048 × P)
- The value of N is selected so that f_S × N = PLLCLKIN x K x R / P is in the allowable range.

Example: MCLK = 12 MHz and f_S = 44.1 kHz, (N=2048)
Select P = 1, R = 1, K = 7.5264, which results in J = 7, D = 5264

Example: MCLK = 12 MHz and f_S = 48.0 kHz, (N=2048)
Select P = 1, R = 1, K = 8.192, which results in J = 8, D = 1920

Values are written to the registers in Table 4.

Table 4. PLL Registers

DIVIDER	FUNCTION	BITS
PLLE	PLL enable	P0-R4, B[0]
PPDV	PLL P	P0-R20, B[3:0]
PJDV	PLL J	P0-R21, B[5:0]
PDDV	PLL D	P0-R22, B[5:0]
		P0-R23, B[7:0]
PRDV	PLL R	P0-R24, B[3:0]

Table 5. PLL Configuration Recommendations

COLUMN	DESCRIPTION
f_S (kHz)	Sampling frequency
R_{MLCK}	Ratio between sampling frequency and MLCK frequency (MLCK frequency = RMLCK x sampling frequency)
MLCK (MHz)	System master clock frequency at MLCK input (pin 20)
PLL VCO (MHz)	PLL VCO frequency as PLLCK in Figure 63
P	One of the PLL coefficients in Equation 1
PLL REF (MHz)	Internal reference clock frequency which is produced by MLCK / P
M = K × R	The final PLL multiplication factor computed from K and R as described in Equation 1
K = J.D	One of the PLL coefficients in Equation 1
R	One of the PLL coefficients in Equation 1
PLL f_S	Ratio between f_S and PLL VCO frequency (PLL VCO / f_S)
DSP f_S	Ratio between operating clock rate and f_S (PLL f_S / NMAC)
NMAC	The clock divider value in Table 3
DSP CLK (MHz)	The operating frequency as DSPCK in Figure 63
MOD f_S	Ratio between DAC operating clock frequency and f_S (PLL f_S / NDAC)
MOD f (kHz)	DAC operating frequency as DACCK in
NDAC	DAC clock divider value in Table 3
DOSR	OSR clock divider value in Table 3 for generating OSRCK in Figure 63. DOSR must be chosen so that MOD f_S / DOSR = 16 for correct operation.
NCP	NCP (negative charge pump) clock divider value in Table 3
CP f	Negative charge pump clock frequency (f_S * MOD f_S / NCP)
% Error	Percentage of error between PLL VCO / PLL f_S and f_S (mismatch error). • This value is typically zero but can be non-zero especially when K is not an integer (D is not zero). • This value may be non-zero only when the TAS5754M device acts as a master.

The equations above explain how to calculate all necessary coefficients and controls to configure the PLL. Table 6 provides for easy reference to the recommended clock divider settings for the PLL as a Master Clock.

Table 6. Recommended Clock Divider Settings for PLL as Master Clock

f_S (kHz)	R_{MLCK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
8	128	1.024	98.304	1	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	192	1.536	98.304	1	1.536	64	32	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	256	2.048	98.304	1	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	384	3.072	98.304	3	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	512	4.096	98.304	3	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	768	6.144	98.304	3	2.048	48	48	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	1024	8.192	98.304	3	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	1152	9.216	98.304	9	1.024	96	48	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	1536	12.288	98.304	9	1.365	72	36	2	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	2048	16.384	98.304	9	1.82	54	54	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
8	3072	24.576	98.304	9	2.731	36	36	1	12288	1024	12	8.192	768	6144	16	48	0	4	1536
11.025	128	1.4112	90.3168	1	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	192	2.1168	90.3168	3	0.706	128	32	4	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	256	2.8224	90.3168	1	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	384	4.2336	90.3168	3	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	512	5.6448	90.3168	3	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	768	8.4672	90.3168	3	2.822	32	32	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	1024	11.2896	90.3168	3	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	1152	12.7008	90.3168	9	1.411	64	32	2	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	1536	16.9344	90.3168	9	1.882	48	48	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	2048	22.5792	90.3168	9	2.509	36	36	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
11.025	3072	33.8688	90.3168	9	3.763	24	24	1	8192	1024	8	11.2896	512	5644.8	16	32	0	4	1411.2
16	64	1.024	98.304	1	1.024	96	48	2	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	128	2.048	98.304	1	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	192	3.072	98.304	1	3.072	32	32	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	256	4.096	98.304	1	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	384	6.144	98.304	3	2.048	48	48	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	512	8.192	98.304	3	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	768	12.288	98.304	3	4.096	24	24	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	1024	16.384	98.304	3	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	1152	18.432	98.304	3	6.144	16	16	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	1536	24.576	98.304	9	2.731	36	36	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	2048	32.768	98.304	9	3.641	27	27	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536
16	3072	49.152	98.304	9	5.461	18	18	1	6144	1024	6	16.384	384	6144	16	24	0	4	1536

Table 6. Recommended Clock Divider Settings for PLL as Master Clock (continued)

f_S (kHz)	R_{MLCK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
22.05	64	1.4112	90.3168	1	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	128	2.8224	90.3168	1	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	192	4.2336	90.3168	3	1.411	64	32	2	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	256	5.6448	90.3168	1	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	384	8.4672	90.3168	3	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	512	11.2896	90.3168	3	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	768	16.9344	90.3168	3	5.645	16	16	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	1024	22.5792	90.3168	3	7.526	12	12	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	1152	25.4016	90.3168	9	2.822	32	32	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	1536	33.8688	90.3168	9	3.763	24	24	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
22.05	2048	45.1584	90.3168	9	5.018	18	18	1	4096	1024	4	22.5792	256	5644.8	16	16	0	4	1411.2
32	32	1.024	98.304	1	1.024	96	48	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	48	1.536	98.304	1	1.536	64	16	4	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	64	2.048	98.304	1	2.048	48	24	2	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	128	4.096	98.304	1	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	192	6.144	98.304	3	2.048	48	48	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	256	8.192	98.304	2	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	384	12.288	98.304	3	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	512	16.384	98.304	3	5.461	18	18	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	768	24.576	98.304	3	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	1024	32.768	98.304	3	10.923	9	9	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	1152	36.864	98.304	9	4.096	24	24	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
32	1536	49.152	98.304	6	8.192	12	12	1	3072	1024	3	32.768	192	6144	16	12	0	4	1536
44.1	32	1.4112	90.3168	1	1.411	64	32	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	64	2.8224	90.3168	1	2.822	32	16	2	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	128	5.6448	90.3168	1	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	192	8.4672	90.3168	3	2.822	32	32	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	256	11.2896	90.3168	2	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	384	16.9344	90.3168	3	5.645	16	16	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	512	22.5792	90.3168	3	7.526	12	12	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	768	33.8688	90.3168	3	11.29	8	8	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2
44.1	1024	45.1584	90.3168	3	15.053	6	6	1	2048	1024	2	45.1584	128	5644.8	16	8	0	4	1411.2

Table 6. Recommended Clock Divider Settings for PLL as Master Clock (continued)

f_S (kHz)	R_{MLCK}	MCLK (MHz)	PLL VCO (MHz)	P	PLL REF (MHz)	M = K×R	K = J×D	R	PLL f_S	DSP f_S	NMAC	DSP CLK (MHz)	MOD f_S	MOD f (kHz)	NDAC	DOSR	% ERROR	NCP	CP f (kHz)
48	32	1.536	98.304	1	1.536	64	32	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	64	3.072	98.304	1	3.072	32	16	2	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	128	6.144	98.304	1	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	192	9.216	98.304	3	3.072	32	32	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	256	12.288	98.304	2	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	384	18.432	98.304	3	6.144	16	16	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	512	24.576	98.304	3	8.192	12	12	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	768	36.864	98.304	3	12.288	8	8	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
48	1024	49.152	98.304	3	16.384	6	6	1	2048	1024	2	49.152	128	6144	16	8	0	4	1536
96	32	3.072	98.304	1	3.072	32	16	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	48	4.608	98.304	3	1.536	64	32	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	64	6.144	98.304	1	6.144	16	8	2	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	128	12.288	98.304	2	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	192	18.432	98.304	3	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	256	24.576	98.304	4	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	384	36.864	98.304	6	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
96	512	49.152	98.304	8	6.144	16	16	1	1024	512	2	49.152	64	6144	16	4	0	4	1536
192	32	6.144	98.304	1	6.144	16	8	2	512	256	2	49.152	32	6144	16	2	0	4	1536
192	48	9.216	98.304	3	3.072	32	16	2	512	256	2	49.152	32	6144	16	2	0	4	1536
192	64	12.288	98.304	1	12.288	8	4	2	512	256	2	49.152	32	6144	16	2	0	4	1536
192	128	24.576	98.304	2	12.288	8	8	1	512	256	2	49.152	32	6144	16	2	0	4	1536
192	192	36.864	98.304	3	12.288	8	8	1	512	256	2	49.152	32	6144	16	2	0	4	1536
192	256	49.152	98.304	4	12.288	8	8	1	512	256	2	49.152	32	6144	16	2	0	4	1536

8.3.3.5 Serial Audio Port – Data Formats and Bit Depths

The serial audio interface port is a 3-wire serial port with the signals LRCK/FS (pin 25), SCLK (pin 23), and SDIN (pin 24). SCLK is the serial audio bit clock, used to clock the serial data present on SDIN into the serial shift register of the audio interface. Serial data is clocked into the TAS5754M device on the rising edge of SCLK.The LRCK/FS pin is the serial audio left/right word clock or frame sync when the device is operated in TDM Mode.

Table 7. TAS5754M device Audio Data Formats, Bit Depths and Clock Rates

FORMAT	DATA BITS	MAXIMUM LRCK/FS FREQUENCY (kHz)	MCLK RATE (f_S)	SCLK RATE (f_S)
I^2S/LJ/RJ	32, 24, 20, 16	Up to 192	128 to 3072 (≤ 50 MHz)	64, 48, 32
TDM/DSP	32, 24, 20, 16	Up to 48	128 to 3072	125, 256
		96	128 to 512	125, 256
		192	128, 192, 256	128

The TAS5754M device requires the synchronization of LRCK/FS and system clock, but does not need a specific phase relation between LRCK/FS and system clock.

If the relationship between LRCK/FS and system clock changes more than ±5 MCLK, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until re-synchronization between LRCK/FS and system clock is completed.

If the relationship between LRCK/FS and SCLK are invalid more than 4 LRCK/FS periods, internal operation is initialized within one sample period and analog outputs are forced to the bipolar zero level until re-synchronization between LRCK/FS and SCLK is completed.

8.3.3.5.1 Data Formats and Master/Slave Modes of Operation

The TAS5754M device supports industry-standard audio data formats, including standard I^2S and left-justified. Data formats are selected via Register (P0-R40). All formats require binary two's complement, MSB-first audio data; up to 32-bit audio data is accepted. The data formats are detailed in Figure 66 through Figure 71.

The TAS5754M device also supports right-justified and TDM/DSP data. I^2S, LJ, RJ, and TDM/DSP are selected using Register (P0-R40). All formats require binary 2s complement, MSB-first audio data. Up to 32 bits are accepted. Default setting is I^2S and 24 bit word length. The I^2S slave timing is shown in .

shows a detailed timing diagram for the serial audio interface.

In addition to acting as a I^2S slave, the TAS5754M device can act as an I^2S master, by generating SCLK and LRCK/FS as outputs from the MCLK input. Table 8 lists the registers used to place the device into Master or Slave mode. Please refer to the *Serial Audio Port Timing – Master Mode* section for serial audio Interface timing requirements in Master Mode. For Slave Mode timing, please refer to to the *Serial Audio Port Timing – Slave Mode* section.

Table 8. I^2S Master Mode Registers

REGISTER	FUNCTION
P0-R9-B0, B4, and B5	I^2S Master mode select
P0-R32-B[6:0]	SCLK divider and LRCK/FS divider
P0-R33-B[7:0]	

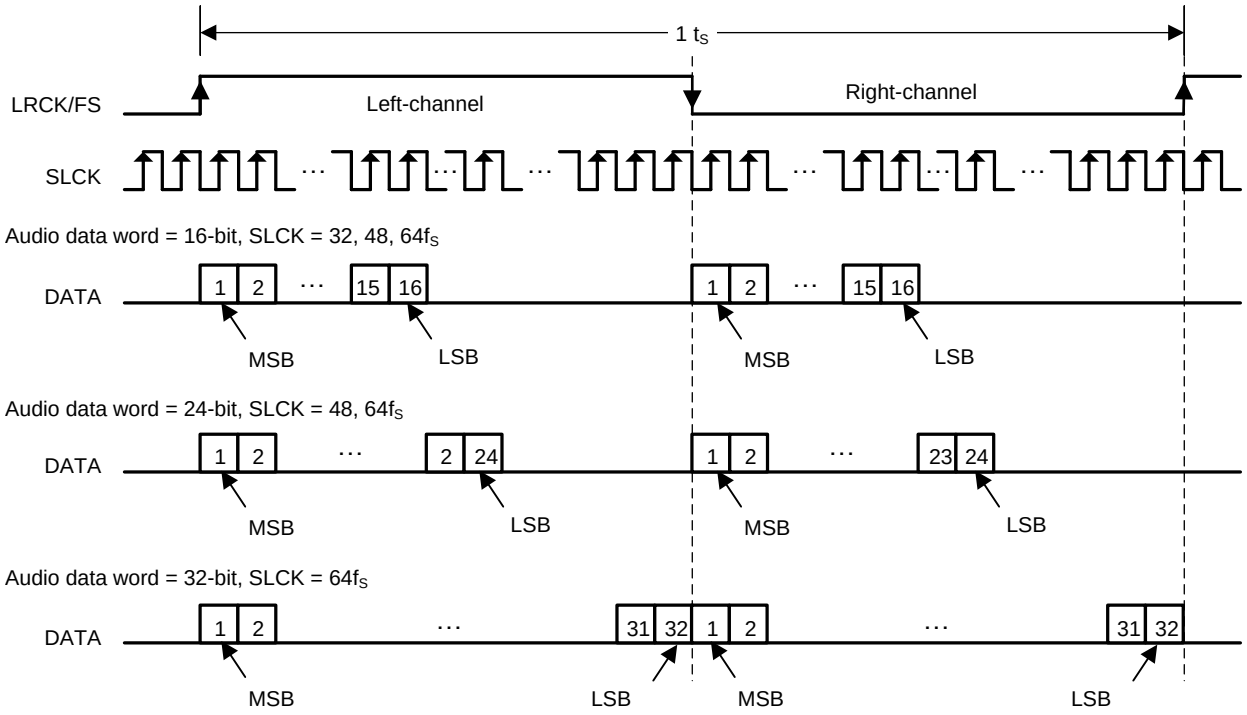
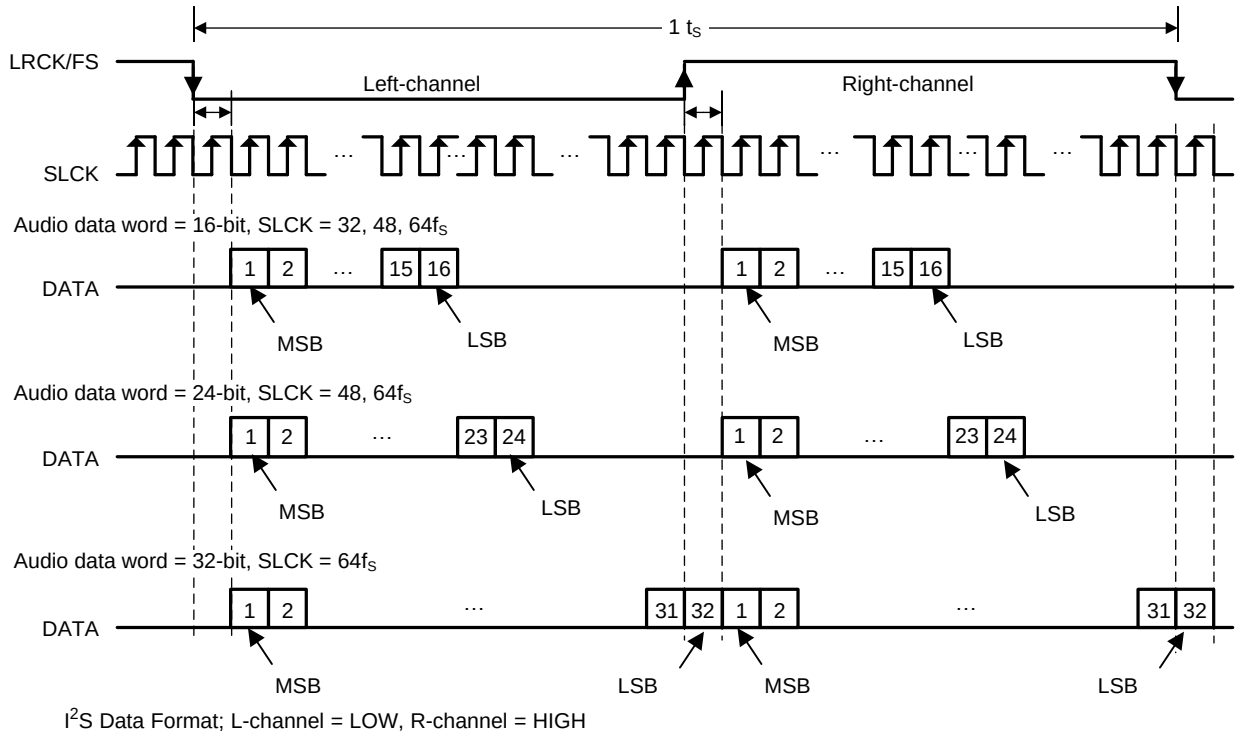
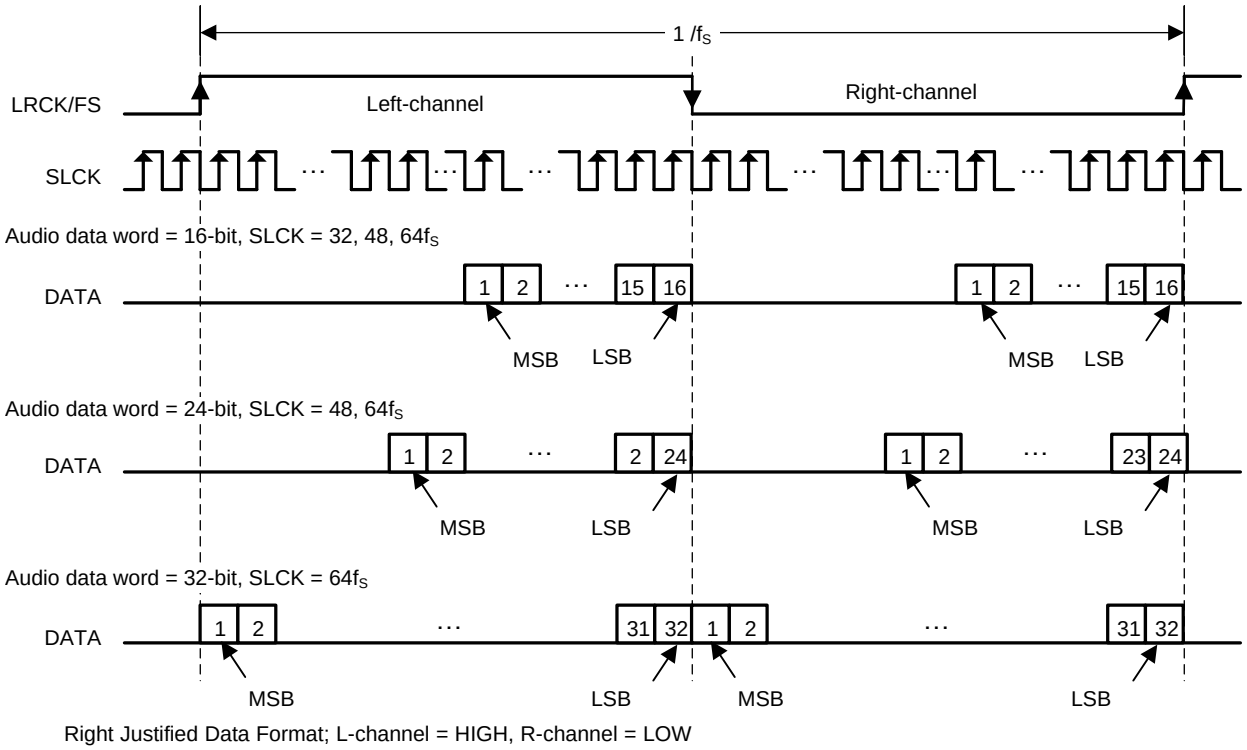


Figure 66. Left Justified Audio Data Format



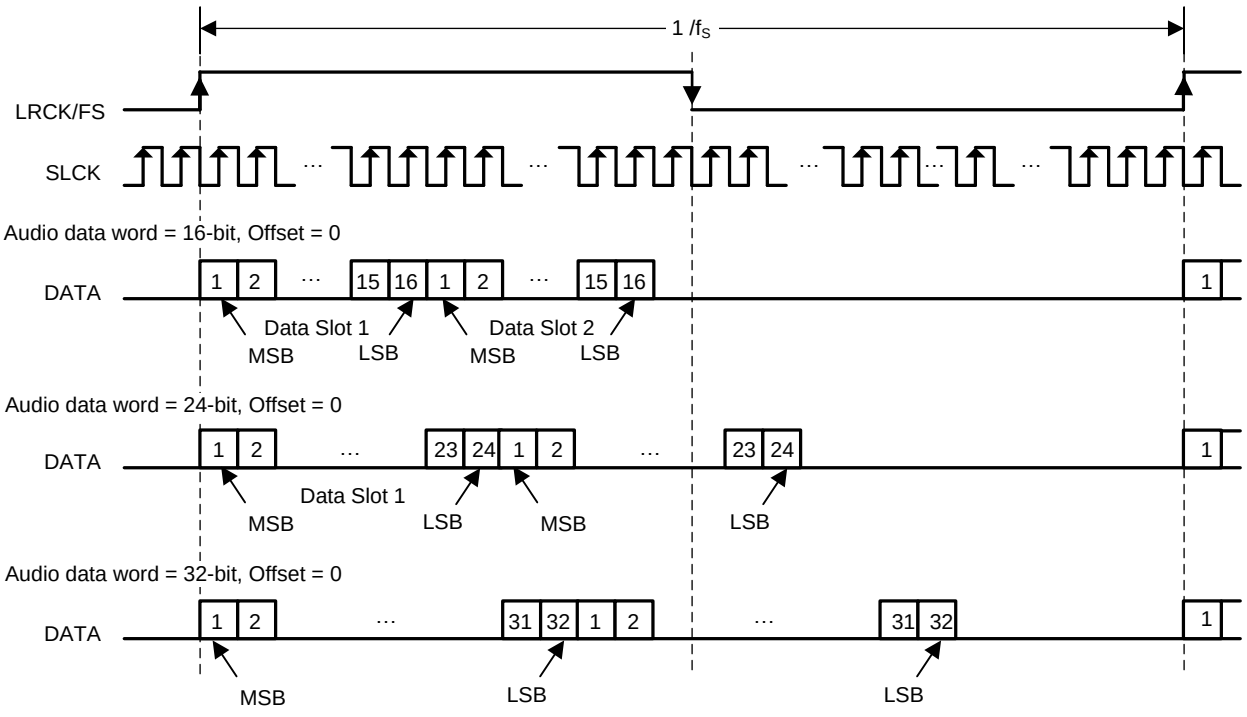
I^2S Data Format; L-channel = LOW, R-channel = HIGH

Figure 67. I^2S Audio Data Format



Right Justified Data Format; L-channel = HIGH, R-channel = LOW

Figure 68. Right Justified Audio Data Format



TDM/DSP Data Format with OFFSET = 0

Figure 69. TDM/DSP 1 Audio Data Format

NOTE

In TDM Modes, Duty Cycle of LRCK/FS should be 1x SCLK at minimum. Rising edge is considered frame start.

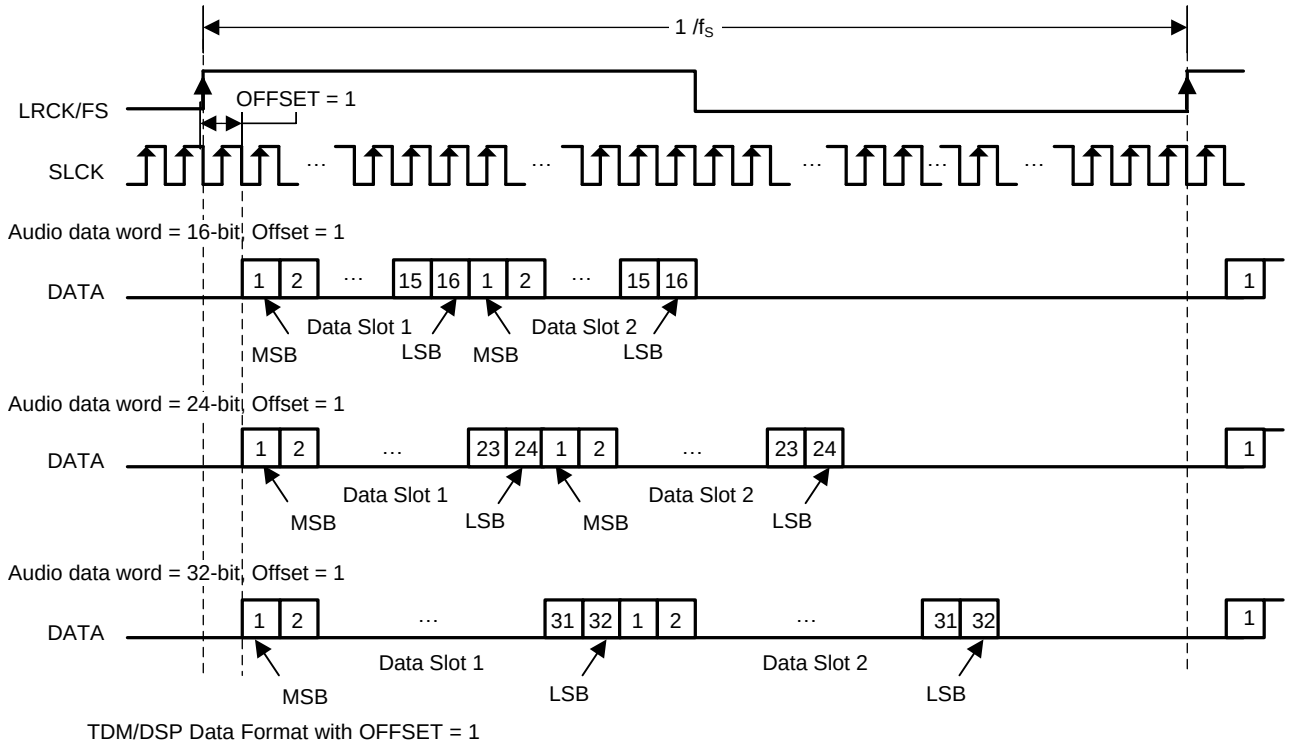


Figure 70. TDM/DSP 2 Audio Data Format

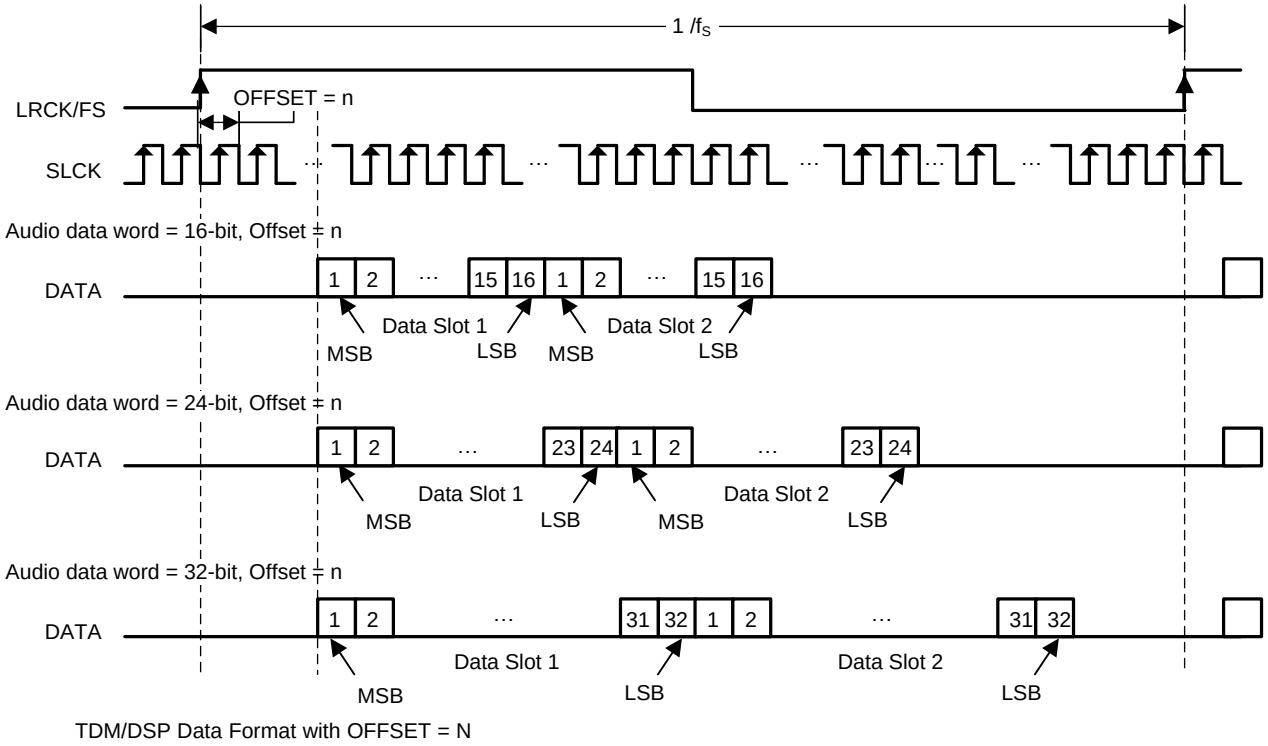


Figure 71. TDM/DSP 3 Audio Data Format

8.3.3.6 Input Signal Sensing (Power-Save Mode)

The TAS5754M device has a zero-detect function. This function can be applied to both channels of data as an AND function or an OR function, via controls provided in the control port in P0-R65-B[2:1].Continuous Zero data cycles are counted by LRCK/FS, and the threshold of decision for analog mute can be set by P0-R59, B[6:4] for the data which is clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal and P0-R59, B[2:0] for the data which is clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal as shown in Table 10. Default values are 0 for both channels.

Table 9. Zero Detection Mode

ATMUTECTL	VALUE	FUNCTION
Bit : 2	0	Zero data triggers for the two channels for zero detection are OR'ed together.
	1 (Default)	Zero data triggers for the two channels for zero detection are AND'ed together.
Bit : 1	0	Zero detection and analog mute are disabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the right frame of an I^2S signal or Slot 2 of a TDM signal.
Bit : 0	0	Zero detection analog mute are disabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.
	1 (Default)	Zero detection analog mute are enabled for the data clocked in on the left frame of an I^2S signal or Slot 1 of a TDM signal.

Table 10. Zero Data Detection Time

ATMUTETIML OR ATMA	NUMBER OF LRCK/FS CYCLES	TIME @ 48kHz
0 0 0	1024	21 ms
0 0 1	5120	106 ms
0 1 0	10240	213 ms
0 1 1	25600	533 ms
1 0 0	51200	1.066 sec
1 0 1	102400	2.133 sec
1 1 0	256000	5.333 sec
1 1 1	512000	10.66 sec

8.3.3.7 Serial Data Output

If it is supported by the HybridFlow in use, the TAS5754M device can present serial data on one of the three available hardware pins, GPIO0, GPIO1, or GPIO2. In a HybridFlow which supports serial data out, the serial data out origin can always be configured to come before the mini-DSP, by clearing the SDSL bit in P0-R7. This feature is used as a *loop-back* to check the integrity of the data transmission from the source to the TAS5754M device . In addition to the default loop-back mode, HybridFlows allows the SDOUT signal to originate from either a point after the processing or from some intermediary point within the HybridFlow. This option is accomplished by setting the SDSL bit in P0-R7. Figure 72 shows how to configure the origin of the serial data output signal.

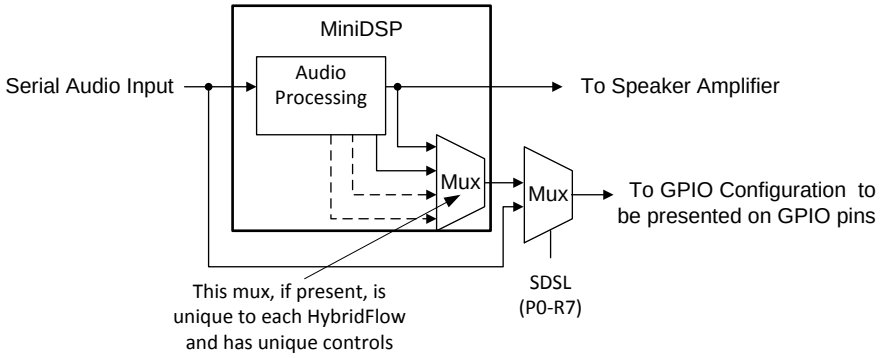


Figure 72. Serial Data Output Signal

Choosing the origin to be after all processing has been applied to the signal (i.e. before it is sent to the amplifier) is popular for sending a monitor signal back to a voice processing or echo-cancelling device elsewhere in the system. Other origins may configure the signal to originate after a subwoofer generation block, which sums in the inputs and applies a low-pass filter to create a mono, low-frequency signal. Please refer to the target HybridFlows for details regarding the options for the serial data output.

8.3.4 miniDSP Audio Processing Engine

The TAS5754M device integrates a highly efficient processing engine called a miniDSP. The miniDSP in the TAS5754M device uses a Hybrid architecture in which some processing blocks are built in ROM and other processing blocks are created in RAM via the PurePath™ Control Console GUI. This approach allows the flexibility of a fully-programmable device to be combined with the ease of use and rapid download time of a hard-coded ROM device.

8.3.4.1 HybridFlow Architecture

The Hybrid RAM and ROM Architecture allows the device to be highly flexible, but also easy to use. Unlike a device where all digital processing blocks are hard-coded in ROM, the hybrid RAM and ROM architecture allows a variety of processing blocks to be used in various combinations with various connectivity. These combinations of processing blocks are called *HybridFlows*.

HybridFlows are generated by combining a collection of processing blocks together in a targeted manner so that the device is well suited for a particular application or use case. Some HybridFlows are targeted for stereo applications, while others are targeted for mono, 1.1 (Bi-Amped), or 2.1 configurations.

It is important to note that the amount of processing which can be combined together into a given process flow is highly dependent on the sample rate of the audio signal which is being processed. For instance, an audio signal at 48 kHz can have much more processing applied than the same signal presented to the TAS5754M device at 192 kHz sample rate. For this reason, a HybridFlow which supports only up to 48 kHz sample rate cannot be used with a 192 kHz input signal.

8.3.4.2 Volume Control

8.3.4.2.1 Digital Volume Control

A basic digital volume control with range between 24 dB and 103 dB and mute is available on each channels by P0-R61-B[7:0] for SPK_OUTB± and P0-R62-B[7:0] for SPK_OUTA±. These volume controls all have 0.5 dB step programmability over most gain and attenuation ranges. Table 11 lists the detailed gain versus programmed setting for this basic volume control. Volume can be changed for both SPK_OUTB± and SPK_OUTA± at the same time or independently by P0-R61-B[1:0] . When B[1:0] set 00 (default), independent control is selected. When B[1:0] set 01, SPK_OUTA± accords with SPK_OUTB± volume. When B[1:0] set 10, SPK_OUTA± volume controls the volume for both channels. To set B[1:0] to 11 is prohibited.

Table 11. Digital Volume Control Settings

GAIN SETTING	BINARY DATA	GAIN (dB)	COMMENTS
0	0000-0000	24.0	Positive maximum
1	0000-0001	23.5	
. . .	. . .	. . .	
46	0010-1110	1.0	
47	0010-1111	0.5	
48	0011-0000	0.0	No attenuation (default)
49	0011-0001	–0.5	
50	0011-0010	–1.0	
51	0011-0011	–1.5	
. . .	. . .	. . .	
253	1111-1101	–102.5	
254	1111-1110	–103	Negative maximum
255	1111-1111	– ∞	Negative infinite (Mute)

Ramp-up frequency and ramp-down frequency can be controlled by P0-R63, B[7:6] and B[3:2] as shown in Table 12. Also ramp-up step and ramp-down step can be controlled by P0-R63, B[5:4] and B[1:0] as shown in Table 13.

Table 12. Ramp Up or Down Frequency

RAMP UP SPEED	EVERY N f_S	COMMENTS	RAMP DOWN FREQUENCY	EVERY N f_S	COMMENTS
00	1	Default	00	1	Default
01	2		01	2	
10	4		10	4	
11	Direct change		11	Direct change	

Table 13. Ramp Up or Down Step

RAMP UP STEP	STEP dB	COMMENTS	RAMP DOWN STEP	STEP dB	COMMENTS
00	4.0		00	–4.0	
01	2.0		01	–2.0	
10	1.0	Default	10	–1.0	Default
11	0.5		11	–0.5	

8.3.4.2.1.1 Emergency Volume Ramp Down

Emergency ramp down of the volume by is provided for situations such as I^2S clock error and power supply failure. Ramp-down speed is controlled by P0-R64-B[7:6]. Ramp-down step can be controlled by P0-R64-B[5:4]. Default is ramp-down by every f_S cycle with –4dB step.

8.3.5 Adjustable Amplifier Gain and Switching Frequency Selection

The voltage divider between the GVDD_REG pin a the SPK_GAIN/FREQ pin is used to set the gain and switching frequency of the amplifier. The voltage presented on the SPK_GAIN/FREQ pin is digitized and then decoded into a 3 bit word which is interpreted inside the TAS5754M device to correspond to a given gain and switching frequency.

Because the amplifier adds gain to both the signal and the noise present in the audio signal, the lowest gain setting that can meet voltage-limited output power targets should be used. This ensures that the power target can be reached while minimizing the idle channel noise of the system. The switching frequency selection affects three important operating characteristics of the device. These are the power dissipation in the device, the power dissipation in the inductor, and the target output filter for the application.

Higher switching frequencies typically result in slightly higher power dissipation in the TAS5754M device and lower dissipation in the inductor in the system, due to decreased ripple current through the inductor and increased charging and discharging current in device and parasitic capacitances. Switching at the higher of the two available switching frequencies will result in lower overall dissipation in the system and lower operating temperature of the inductors. However, the thermally limited power output of the device may be decreased in this situation, because some of the TAS5754M device thermal headroom will be absorbed by the higher switching frequency. Conversely inductor heating can be reduced by using the higher switching frequency in order to reduce the ripple current.

Another advantage of increasing the switching frequency is that the higher frequency carrier signal can be filtered by an L-C filter with a higher corner frequency, leading to physically smaller components. Use the highest switching frequency that continues to meet the thermally limited power targets for the application. If thermal constraints require heat reduction in the TAS5754M device, use a lower switching rate.

The switching frequency of the speaker amplifier is dependent on an internal synchronizing signal, (f_{SYNC}), which is synchronous with the sample rate. The rate of the synchronizing signal is also dependent on the sample rate. Refer to Table 14 below for details regarding how the sample rates correlate to the synchronizing signal.

Table 14. Sample Rates vs Synchronization Signal

SAMPLE RATE [kHz]	f_{SYNC} [kHz]
8	96
16	
32	
48	
96	
192	
11.025	88.2
22.05	
44.1	
88.2	

Table 15 summarizes the de-code of the voltage presented to the SPK_GAIN/FREQ pin.

Table 15. Amplifier Switching Mode vs. SPK_GAIN/FREQ Voltage

$V_{SPK\_GAIN/FREQ}$ (V)		GAIN MODE	AMPLIFIER SWITCHING FREQUENCY MODE
MIN	MAX		
6.61	7	Reserved	Reserved
5.44	6.6	26dBV	8 × f_{SYNC}
4.67	5.43		6 × f_{SYNC}
3.89	4.66		4 × f_{SYNC}
3.11	3.88		2 × f_{SYNC}
2.33	3.1	20dBV	8 × f_{SYNC}
1.56	2.32		6 × f_{SYNC}
0.78	1.55		4 × f_{SYNC}
0	0.77		2 × f_{SYNC}

8.3.6 Error Handling and Protection Suite

8.3.6.1 Device Over-Temperature Protection

The TAS5754M device continuously monitors die temperature to ensure it does to exceed the OTE_{THRES} level specified in the Recommended Operating Conditions table. If an OTE event occurs, the $\overline{SPK\_FAULT}$ line is pulled low and out the SPK_OUTxx outputs transition to high impedance, signifying a fault. This latched error requires the $\overline{SPK\_MUTE}$ line to toggle in order to reset the error. Alternatively, pulling the MCLK, SCLK, or LRCK/FS pin low causes a clock error, which also resets the device. Normal operation resumes by re-starting the stopped clock.

8.3.6.2 SPK_OUTxx Over-Current Protection

The TAS5754M device continuously monitors the output current of each amplifier output to ensure it does to exceed the OCE_{THRES} level specified in the Recommended Operating Conditions table. If an OCE event occurs, the $\overline{SPK\_FAULT}$ line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This latched error requires the $\overline{SPK\_MUTE}$ line to toggle in order to reset the error. Alternatively, pulling the MCLK, SCLK, or LRCK/FS pin low causes a clock error, which also resets the device. Normal operation resumes by re-starting the stopped clock.

8.3.6.3 DC Offset Protection

If the TAS5754M device measures a DC offset in the output voltage, the $\overline{SPK\_FAULT}$ line is pulled low and the SPK_OUTxx outputs transition to high impedance, signifying a fault. This latched error require the $\overline{SPK\_MUTE}$ line to toggle in order to reset the error. Alternatively, pulling the MCLK, SCLK, or LRCK low causes a clock error, which also resets the device. Normal operation resumes by re-starting the stopped clock.

8.3.6.4 Internal V_{AVDD} Undervoltage-Error Protection

The TAS5754M device internally monitors the AVDD net to protect against the AVDD supply dropping unexpectedly. To enable this feature, P1-R5-B0 is used.

8.3.6.5 Internal V_{PVDD} Undervoltage-Error Protection

If the voltage presented on the PVDD supply drops below the $UVE_{THRES(PVDD)}$ value listed in the Recommended Operating Conditions table, the SPK_OUTxx outputs transition to high impedance. This is a self-clearing error, which means that once the PVDD level drops below the level listed in the Recommended Operating Conditions table, the device resumes normal operation.

8.3.6.6 Internal V_{PVDD} Overvoltage-Error Protection

If the voltage presented on the PVDD supply exceeds the $OVE_{THRES(PVDD)}$ value listed in the Recommended Operating Conditions table, the SPK_OUTxx outputs will transition to high impedance. This is a self-clearing error, which means that once the PVDD level drops below the level listed in the Recommended Operating Conditions table, the device will resume normal operation. It is important to note that this voltage only protects up to the level described in the Recommended Operating Conditions table for the PVDD voltage. Exceeding this absolute maximum rating causes damage and possible device failure, because the levels exceed that which can be protected against by the OVE protection circuit.

8.3.6.7 External Undervoltage-Error Protection

The $\overline{SPK\_MUTE}$ pin can also be used to monitor a system voltage, such as a LCD TV backlight, a battery pack in portable device, by using a voltage divider created with two resistors. (See Figure 73)

- If the $\overline{SPK\_MUTE}$ pin makes a transition from “1” to “0” over 6 ms or more, the device switches into external under-voltage protection mode. This mode uses two trigger levels.
- When the $\overline{SPK\_MUTE}$ pin level reaches 2 V, soft mute process begins.
- When the $\overline{SPK\_MUTE}$ pin level reaches 1.2 V, analog output mute engages, regardless of digital audio level, and analog output shutdown begins.

A timing diagram to show this is shown in Figure 74.

NOTE

The $\overline{\text{SPK\_MUTE}}$ input pin voltage range is provided in the Recommended Operating Conditions table. The ratio of external resistors must produce a voltage within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the $\overline{\text{SPK\_MUTE}}$ pin higher than that the level specified in the Recommended Operating Conditions table, potentially causing damage to or failure of the device. Therefore, it is imperative that any monitored voltage (including all ripple, power supply variation, resistor divider variation, transient spikes, etc.) is scaled by the resistor divider network to never drive the voltage on the SPK_MUTE pin higher than the maximum level specified in the Recommended Operating Conditions table.

When the divider is set correctly, any DC voltage can be monitored. shows a 12-V example of how the $\overline{\text{SPK\_MUTE}}$ is used for external undervoltage error protection.

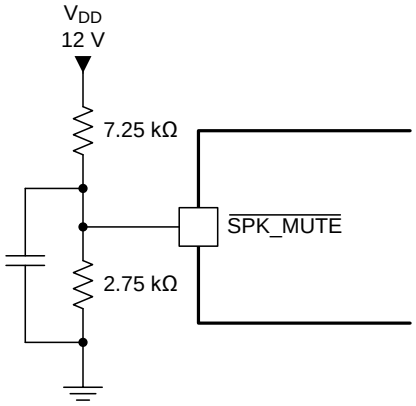


Figure 73. $\overline{\text{SPK\_MUTE}}$ Used in External Undervoltage Error Protection

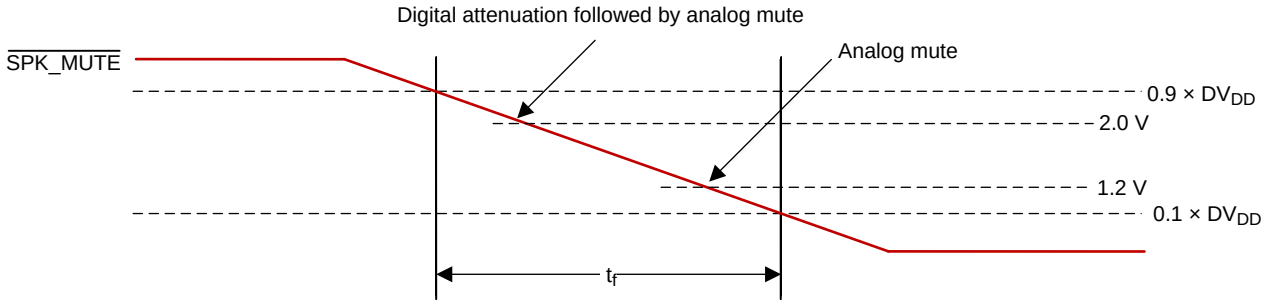


Figure 74. $\overline{\text{SPK\_MUTE}}$ Timing for External Undervoltage Error Protection

8.3.6.8 Internal Clock Error Notification (CLKE)

8.3.7 GPIO Port and Hardware Control Pins

The TAS5754M device includes a versatile GPIO port, allowing signals to be passed from the system to the device or sent out of the device to the system. There are three GPIO pins available for use. These pins can be used for advanced clocking features, to pass internal signals to the system or accept signals from the system for use inside the device by a HybridFlow, or simply to monitor the status of an external signal via I^2C. The GPIO port requires some configuration in the control port. This configuration is detailed in Figure 75.

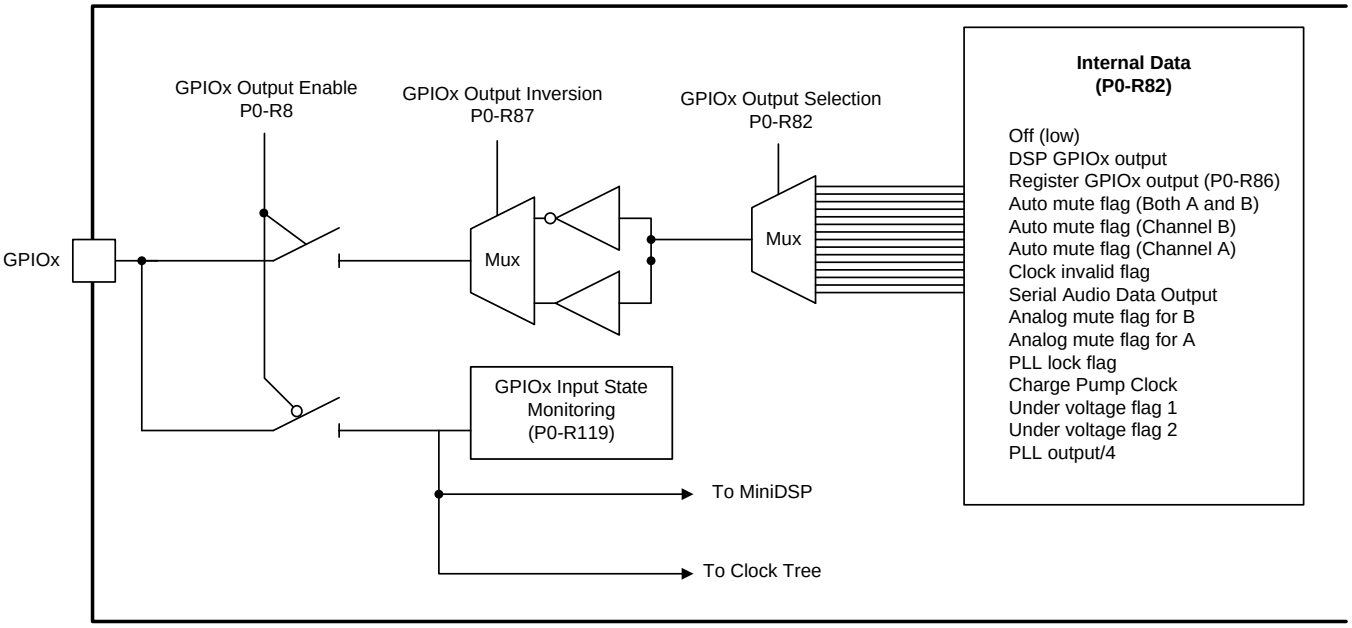


Figure 75. GPIO Port

In addition to the dynamic controls which can be implemented with the GPIO port, each HybridFlow uses the GPIO port as required. In some HybridFlows, a GPIO is used to present an internal serial audio data signal to a system controller. In others, the status of a GPIO pin is monitored and the status of that pin is used to adjust the audio processing applied to the signal. Refer to each HybridFlow for specifics regarding how the GPIO port is used. GPIOs which have been allocated to a function in a HybridFlow can be reassigned using the same controls as those listed in Figure 75. However, they no longer serve the purpose intended by the design of the HybridFlow.

8.3.8 I^2C Communication Port

The TAS5754M device supports the I^2C serial bus and the data transmission protocol for standard and fast mode as a slave device.

8.3.8.1 Slave Address

Table 16. I^2C Slave Address

MSB							LSB
1	0	0	1	1	ADR2	ADR1	R/ $\overline{W}$

The TAS5754M device has 7 bits for its own slave address. The first five bits (MSBs) of the slave address are factory preset to 10011 (0x9x). The next two bits of the address byte are the device select bits which can be user-defined by the ADR1 and ADR0 terminals. A maximum of four devices can be connected on the same bus at one time. This gives a range of 0x98, 0x9A, 0x9C and 0x9E, as detailed below. Each TAS5754M device responds when it receives its own slave address.

Table 17. I^2C Address Configuration via ADR0 and ADR1 Pins

ADR1	ADR0	I^2C SLAVE ADDRESS [R/$\overline{W}$]
0	0	0x99/0x98
0	1	0x9B/0x9A
1	0	0x9D/0x9C
1	1	0x9F/0x9E

8.3.8.2 Register Address Auto-Increment Mode

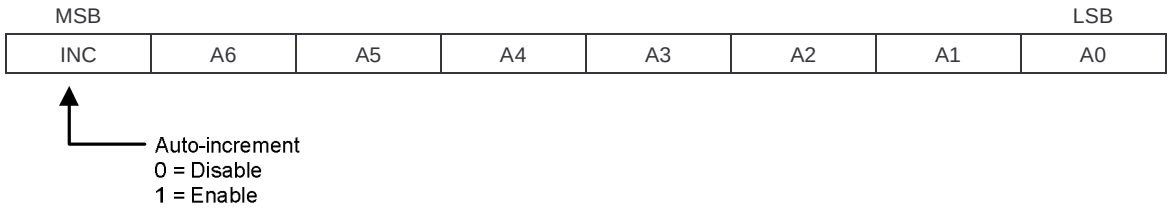


Figure 76. Auto Increment Mode

Auto-increment mode allows multiple sequential register locations to be written to or read back in a single operation, and is especially useful for block write and read operations.

8.3.8.3 Packet Protocol

A master device must control packet protocol, which consists of start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The TAS5754M device supports only slave receivers and slave transmitters.

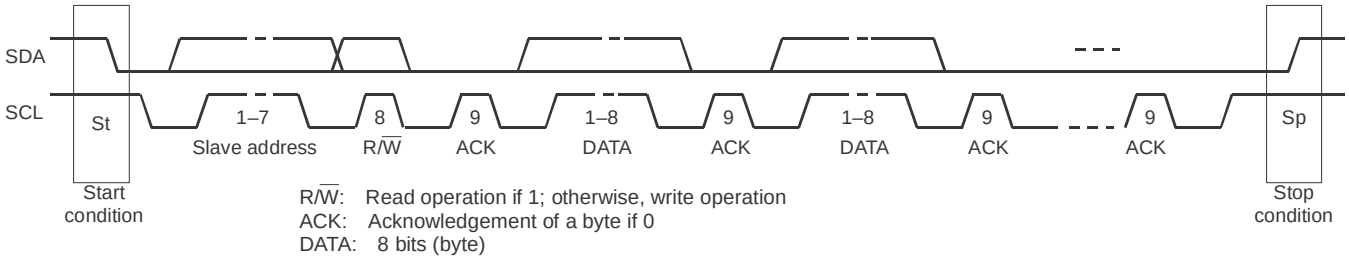


Figure 77. Packet Protocol

Table 18. Write Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		ACK	Sp

Table 19. Read Operation - Basic I²C Framework

Transmitter	*M*	*M*	*M*	*S*	*S*	*M*	*S*	*M*		*M*	*M*
Data Type	St	slave address	R/	ACK	DATA	ACK	DATA	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition

8.3.8.4 Write Register

A master can write to any TAS5754M device registers using single or multiple accesses. The master sends a TAS5754M device slave address with a write bit, a register address with auto-increment bit, and the data. If auto-increment is enabled, the address is that of the starting register, followed by the data to be transferred. When the data is received properly, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 20 shows the write operation.

Table 20. Write Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*S*	*M*	*S*		*S*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	write data 1	ACK	write data 2	ACK		ACK	Sp

M = Master Device; S = Slave Device; St = Start Condition Sp = Stop Condition; W = Write; ACK = Acknowledge

8.3.8.5 Read Register

A master can read the TAS5754M device register. The value of the register address is stored in an indirect index register in advance. The master sends a TAS5754M device slave address with a read bit after storing the register address. Then the TAS5754M device transfers the data which the index register points to. When auto-increment is enabled, the index register is incremented by 1 automatically. When the index register reaches 0x7F, the next value is 0x0. Table 21 shows the read operation.

Table 21. Read Operation

Transmitter	*M*	*M*	*M*	*S*	*M*		*S*	*M*	*M*	*M*	*S*	*S*	*M*		*M*	*M*
Data Type	St	slave addr	W	ACK	inc	reg addr	ACK	Sr	slave addr	R	ACK	data	ACK		NACK	Sp

M = Master Device; S = Slave Device; St = Start Condition; Sr = Repeated start condition; Sp = Stop Condition; W = Write; R = Read; NACK = Not acknowledge

8.3.9 Device Functional Modes

Because the TAS5754M device is a highly configurable device, numerous modes of operation can exist for the device. For the sake of succinct documentation, these modes are divided into two modes:

- Fundamental operating modes
- Secondary usage modes

Fundamental operating modes are the primary modes of operation that affect the major operational characteristics of the device. These are the most basic configurations that are chosen to ensure compatibility with the intended application or the other components that interact with the device in the final system. Some examples of these are the communication protocol used by the control port, the output configuration of the amplifier, or the Master/Slave clocking configuration.

The fundamental operating modes are described starting in the *Serial Audio Port Operating Modes* section.

Secondary usage modes are best described as modes of operation that are used after the fundamental operating modes are chosen to fine tune how the device operates within a given system. These secondary usage modes may include selecting between left justified and right justified Serial Audio Port data formats, or enabling some slight gain/attenuation within the DAC path. Secondary usage modes are accomplished through manipulation of the registers and controls in the I^2C control port. Those modes of operation are described in their respective register/bit descriptions and, to avoid redundancy, are not included in this section.

8.3.9.1 Serial Audio Port Operating Modes

The serial audio port in the TAS5754M device supports industry-standard audio data formats, including I^2S, Time Division Multiplexing (TDM), Left-Justified (LJ), and Right-Justified (RJ) formats. To select the data format that will be used with the device, controls are provided on P0-R40. The timing diagrams for the serial audio port are shown in the *Serial Audio Port Timing – Slave Mode* section, and the data formats are shown in the *Serial Audio Port – Data Formats and Bit Depths* section.

8.3.9.2 Communication Port Operating Modes

The TAS5754M device is configured via an I^2C communication port. The device does not support a hardware only mode of operation, nor Serial Peripheral Interface (SPI) communication. The I^2C Communication Protocol is detailed in the *I^2C Communication Port* section. The I^2C timing requirements are described in the *I^2C Bus Timing – Standard* and I^2C Bus Timing – Fast sections.

8.3.9.3 Audio Processing Modes via HybridFlow Audio Processing

The TAS5754M device can be configured to include several different audio processing features through the use of pre-defined DSP loads called HybridFlows. These HybridFlows have been created and tested to be application focused. This approach results in a device which offers the flexibility of a programmable device with the ease-of-use and fast download time of a fixed function device. The HybridFlows are selected and downloaded using the PurePath™ ControlConsole software. .

8.3.9.4 Speaker Amplifier Operating Modes

The TAS5754M device can be used in three different amplifier configurations:

- Stereo Mode
- Mono Mode
- Bi-Amp Mode

8.3.9.4.1 Stereo Mode

The familiar stereo mode of operation uses the TAS5754M device to amplify two independent signals, which represent the left and right portions of a stereo signal. These amplified left and right audio signals are presented on differential output pairs shown as SPK_OUTA± and SPK_OUTB±. The routing of the audio data which is presented on the SPK_OUTxx outputs can be changed according to the HybridFlow which is used and the configuration of registers P0-R42-B[5:4] and P0-R42-B[1:0]. This mode of operation is shown in Figure 80.

By default, the TAS5754M device is configured to output the Right frame of a I^2S input on the Channel A output and the left frame on the Channel B output.

8.3.9.4.2 Mono Mode

This mode of operation is used to describe operation in which the two outputs of the device are placed in parallel with one another to increase the power sourcing capabilities of the device.

On the output side of the TAS5754M device, the summation of the devices can be done before the filter in a configuration called *Pre-Filter Parallel Bridge Tied Load* (PBTL). However, it is sometimes preferable to merge the two outputs together after the inductor portion of the output filter. Doing so does require two additional inductors, but allows smaller, less expensive inductors to be used because the current is divided between the two inductors. This is called *Post-Filter PBTL*. Both variants of mono operation are shown in Figure 78 and Figure 79.

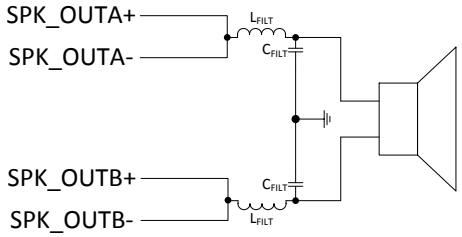


Figure 78. Pre-Filter PBTL

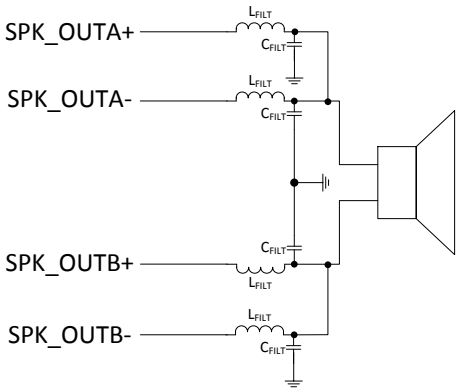


Figure 79. Post-Filter PBTL

On the input side of the TAS5754M device, the input signal to the mono amplifier can be selected from the any slot in a TDM stream or the left or right frame from an I^2S, LJ, or RJ signal. It can also be configured to amplify some mixture of two signals, as in the case of a subwoofer channel which mixes the left and right channel together and sends it through a low-pass filter in order to create a mono, low-frequency signal.

This mode of operation is shown in the *Mono (PBTL) Systems* section.

8.3.9.4.3 Bi-Amp Mode

Bi-Amp mode, sometimes also referred to as *1.1 Mode* uses a two channel device (such as the TAS5754M device) to amplify two different frequency regions of the same signal for a two-way speaker. This is most often used in a single active speaker, where one channel of the amplifier is use to drive the high frequency transducer and one channel is used to drive the low-frequency transducer. To operate in *Bi-Amped Mode* or *1.1 Mode*, an appropriate HybridFlow must be chosen, because the frequency separation and audio processing must occur in the DSP. This mode of operation is shown in the *1.1 (Dual BTL, Bi-Amped) Systems* section.

8.3.9.4.4 Master and Slave Mode Clocking for Digital Serial Audio Port

The digital audio serial port in the TAS5754M device can be configured to receive its clocks from another device as a serial audio slave device. This mode of operation is described in the Clock Slave Mode with SLCK PLL to Generate Internal Clocks (3-Wire PCM) section. If there no system processor available to provide the audio clocks, the TAS5754M device can be placed into Master Mode. In this mode, the TAS5754M device provides the clocks to the other audio devices in the system. For more details regarding the Master and Slave mode operation within the TAS5754M device, please refer to Serial Audio Port Operating Modes.

8.4 Register Maps

8.4.1 Control Port Registers- Quick Reference

Register Quick Reference ~ Page 0

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
1	1	P0-R1	Reserved	Reserved	Reserved	RSTM	Reserved	Reserved	Reserved	RSTR	0
			0	0	0	0	0	0	0	0	
2	2	P0-R2	Reserved	Reserved	Reserved	RQST	Reserved	Reserved	Reserved	RQPD	0
			0	0	0	0	0	0	0	0	
3	3	P0-R3	Reserved	Reserved	Reserved	RQMB	Reserved	Reserved	Reserved	RQMA	0
			0	0	0	0	0	0	0	0	
4	4	P0-R4	Reserved	Reserved	Reserved	PLCK	Reserved	Reserved	Reserved	PLLE	1
			0	0	0	0	0	0	0	1	
5	5	P0-R5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
6	6	P0-R6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
7	7	P0-R7	Reserved	Reserved	Reserved	DEMP	Reserved	Reserved	Reserved	SDSL	0
			0	0	0	0	0	0	0	0	
8	8	P0-R8	Reserved	Reserved	G2OE	INTMUTE	G0OE	G1OE	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
9	9	P0-R9	Reserved	Reserved	SCLKP	SCLKO	Reserved	Reserved	Reserved	LRCKFSO	0
			0	0	0	0	0	0	0	0	
10	A	P0-R10	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
11	B	P0-R11	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
12	C	P0-R12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RSCLK	RLRCKFS	7C
			0	1	1	1	1	1	0	0	
13	D	P0-R13	Reserved	SREF			Reserved	Reserved	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
14	E	P0-R14	Reserved	SDAC			Reserved	Reserved	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
15	F	P0-R15	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...		...	...								...
17	H	P0-R17	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
18	12	P0-R18	Reserved	Reserved	Reserved	Reserved	Reserved	GREF			0
			0	0	0	0	0	0	0	0	
19	13	P0-R19	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RQSY	10
			0	0	0	0	1	0	0	0	
20	14	P0-R20	Reserved	Reserved	Reserved	Reserved	PPDV				0
			0	0	0	0	0	0	0	0	
21	15	P0-R21	Reserved	Reserved	Reserved	PJDV					0
			0	0	0	0	0	0	0	0	
22	16	P0-R22	Reserved	Reserved	PDDV (MSB)						0
			0	0	0	0	0	0	0	0	
23	17	P0-R23	PDDV (LSB)								0
			0	0	0	0	0	0	0	0	
24	18	P0-R24	–	–	–	–	PRDV				0
			Reserved	Reserved	Reserved	Reserved	0	0	0	0	
25	19	P0-R25	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
26	1A	P0-R26	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Register Maps (continued)

Register Quick Reference ~ Page 0 (continued)

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
27	1B	P0-R27	Reserved	DDSP							0
			0	0	0	0	0	0	0	0	
28	1C	P0-R28	Reserved	DDAC							0
			0	0	0	0	0	0	0	0	
29	1D	P0-R29	Reserved	DNCP							0
			0	0	0	0	0	0	0	0	
30	1E	P0-R30	Reserved	DOSR							0
			0	0	0	0	0	0	0	0	
31	1F	P0-R31	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
32	20	P0-R32	DSCLK								0
			0	0	0	0	0	0	0	0	
33	21	P0-R33	DLRCKFS								0
			0	0	0	0	0	0	0	0	
34	22	P0-R34	FSSP		Reserved	I16E	Reserved	Reserved	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
35	23	P0-R35	IDAC (MSB)								1
			0	0	0	0	0	0	0	1	
36	24	P0-R36	IDAC (LSB)								0
			0	0	0	0	0	0	0	0	
37	25	P0-R37	IPLK	DCAS	IDCM	IDCH	IDSK	IDBK	IDFS	Reserved	0
			0	0	0	0	0	0	0	–	
38	26	P0-R38	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
39	27	P0-R39	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
40	28	P0-R40	Reserved	Reserved	AFMT		Reserved	Reserved	ALEN		2
			0	0	0	0	0	0	1	0	
41	29	P0-R41	AOFS								0
			0	0	0	0	0	0	0	0	
42	2A	P0-R42	Reserved	Reserved	Reserved	AUPB		Reserved	AUPA		11
			0	0	0	1	0	0	0	1	
43	2B	P0-R43	Reserved	Reserved	Reserved	Reserved	PSEL				1
			0	0	0	0	0	0	0	1	
44	2C	P0-R44	Reserved	Reserved	Reserved	Reserved	Reserved	CMDP			0
			0	0	0	0	0	0	0	0	
45	2D	P0-R45	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
58	3A	P0-R58	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
59	3B	P0-R59	Reserved	AMTB			Reserved	AMTA			0
			0	0	0	0	0	0	0	0	
60	3C	P0-R60	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PCTL		0
			0	0	0	0	0	0	0	0	
61	3D	P0-R61	VOLB								30
			0	0	1	1	0	0	0	0	
62	3E	P0-R62	VOLA								30
			0	0	1	1	0	0	0	0	

Register Maps (continued)

Register Quick Reference ~ Page 0 (continued)

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
63	3F	P0-R63	VNDF		VNDS		VNUF		VNUS		22
			0	0	1	0	0	0	1	0	
64	40	P0-R64	VEDF		VEDS		Reserved	Reserved	Reserved	Reserved	2
			0	0	0	0	0	0	1	0	
65	41	P0-R65	Reserved	Reserved	Reserved	Reserved	Reserved	ACTL	AMLE	AMRE	4
			0	0	0	0	0	1	0	0	
66	42	P0-R66	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
81	51	P0-R81	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
82	52	P0-R82	Reserved	Reserved	Reserved	G1SL					0
			0	0	0	0	0	0	0	0	
83	53	P0-R83	Reserved	Reserved	Reserved	G0SL					0
			0	0	0	0	0	0	0	0	
84	54	P0-R84	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
85	55	P0-R85	Reserved	Reserved	Reserved	G2SL					0
			0	0	0	0	0	0	0	0	
86	56	P0-R86	Reserved	Reserved	GOUT2	Reserved	GOUT0	GOUT1	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
87	57	P0-R87	Reserved	Reserved	GINV2	Reserved	GINV0	GINV1	Reserved	Reserved	0
			0	0	0	0	0	0	0	0	
88	58	P0-R88	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
89	59	P0-R89	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
90	5A	P0-R90	Reserved	Reserved	Reserved	B1OV	A1OV	B2OV	A2OV	SFOV	0
			0	0	0	0	0	0	0	0	
91	5B	P0-R91	Reserved	DTFS			DTSR				38
			0	0	1	1	1	0	0	0	
92	5C	P0-R92	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DTBR		0
			0	0	0	0	0	0	0	0	
93	5D	P0-R93	DTBR	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	40
			0	1	0	0	0	0	0	0	
94	5E	P0-R94	Reserved	CDST6	CDST5	CDST4	CDST3	CDST2	CDST1	CDST0	0
			0	0	0	0	0	0	0	0	
95	5F	P0-R95	Reserved	Reserved	Reserved	LTSH	Reserved	CKMF	CSRF	CERF	0
			0	0	0	0	0	0	0	0	
96	60	P0-R96	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
107	6B	PO-R107	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
108	6C	P0-R108	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AMBM	AMAM	33
			0	0	1	1	0	0	1	1	
109	6D	P0-R109	Reserved	Reserved	Reserved	SDTM	Reserved	Reserved	Reserved	SHTM	0
			0	0	0	0	0	0	0	0	
110	6E	PO-R110	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
...	...	...	...								...
113	71	PO-R113	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Register Maps (continued)

Register Quick Reference ~ Page 0 (continued)

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
114	72	P0-R114	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	MTST		3
			0	0	0	0	0	0	1	1	
115	73	P0-R115	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FSMM		0
			0	0	0	0	0	0	0	0	
116	74	P0-R116	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
117	75	P0-R117	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
118	76	P0-R118	BOTM	Reserved	Reserved	Reserved	PSTM				85
			1	0	0	0	0	1	0	1	
119	77	P0-R119	Reserved	Reserved	GPIN						2D
			0	0	1	0	1	1	0	1	
120	78	P0-R120	Reserved	Reserved	Reserved	AMFB	Reserved	Reserved	Reserved	AMFA	0
			0	0	0	0	0	0	0	0	
121	79	P0-R121	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	DAMD	0
			0	0	0	0	0	0	0	0	
122	7A	P0-R122	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	EIFM	0
			0	0	0	0	0	0	0	0	

Register Quick Reference ~ Page 1

Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
1	1	P1-R1	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	OSEL	0
			0	0	0	0	0	0	0	0	
2	2	P1-R2	Reserved	Reserved	Reserved	BAGN	Reserved	Reserved	Reserved	AAGN	0
			0	0	0	0	0	0	0	0	
3	3	P1-R3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
4	4	P1-R4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
5	5	P1-R5	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	UEPD	UIPD	11
			0	0	0	1	0	0	0	1	
6	6	P1-R6	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	AMCT	0
			0	0	0	0	0	0	0	0	
7	7	P1-R7	Reserved	Reserved	Reserved	AGBB	Reserved	Reserved	Reserved	AGBA	0
			0	0	0	0	0	0	0	0	
8	8	P1-R8	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RCMF	0
			0	0	0	0	0	0	0	0	
9	9	P1-R9	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	VCPD	0
			0	0	0	0	0	0	0	0	

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Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
1	1	P44-R1	Reserved	Reserved	Reserved	Reserved	ACRM	AMDC	ACRS	ASCW	0
			0	0	0	0	0	0	0	0	

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Adr. (Dec)	Adr. (Hex)	Register Name	Default (Binary)								Default (Hex)
			B7	B6	B5	B4	B3	B2	B1	B0	
63	3F	P253-63	PLLFLEX1								0
			0	0	0	0	0	0	0	0	
64	40	P253-64	PLLFLEX2								0
			0	0	0	0	0	0	0	0	

8.4.2 Control Port Registers- Detailed Description

8.4.2.1 P0-R1

Reset Modules [4] (R/W)	00000000
This bit resets the interpolation filter and the DAC modules. Since the DSP is also reset, the coefficient RAM content will also be cleared by the DSP. This bit is auto cleared and can be set only in standby mode.	
Normal	- - - 0 - - - -
Reset modules	- - - 1 - - - -

Reset Register [0] (R/W)	0000000 0
This bit resets the mode registers back to their initial values. The RAM content is not cleared, but the execution source will be back to ROM. This bit is auto cleared and must be set only when the DAC is in standby mode (resetting registers when the DAC is running is prohibited and not supported).	
Normal	- - - - - - - 0
Reset mode registers	- - - - - - - 1

8.4.2.2 P0-R2

Standby Request [4] (R/W)	00000000
When this bit is set, the DAC will be forced into a system standby mode, which is also the mode the system enters in the case of clock errors. In this mode, most subsystems will be powered down but the charge pump and digital power supply.	
Normal operation	- - - 0 - - - -
Standby mode	- - - 1 - - - -
Powerdown Request [0] (R/W)	**0000000 0**
When this bit is set, the DAC will be forced into powerdown mode, in which the power consumption would be minimum as the charge pump is also powered down. However, it will take longer to restart from this mode. This mode has higher precedence than the standby mode, i.e. setting this bit along with bit 4 for standby mode will result in the DAC going into powerdown mode.	
Normal operation	- - - - - - - 0
Powerdown mode	- - - - - - - 1

8.4.2.3 P0-R3

Mute Channel B [4] (R/W)	00000000
This bit issues soft mute request for the Channel B. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - 0 - - - -
Mute	- - - 1 - - - -

Mute Channel A [0] (R/W)	0000000**0**
This bit issues soft mute request for the Channel A. The volume will be smoothly ramped down/up to avoid pop/click noise.	
Normal volume	- - - - - - - 0
Mute	- - - - - - - 1

8.4.2.4 P0-R4

PLL Lock Flag [4] (Read Only)	000**0**0001
This bit indicates whether the PLL is locked or not. When the PLL is disabled this bit always shows that the PLL is not locked.	
The PLL is locked	- - - 0 - - - -
The PLL is not locked	- - - 1 - - - -
PLL Enable [0] (R/W)	**0000000**1
This bit enables or disables the internal PLL. When PLL is disabled, the master clock is switched to the MCLK.	
Disable PLL	- - - - - - - 0
Enable PLL	- - - - - - - 1

8.4.2.5 P0-R7

De-Emphasis Enable [4] (R/W)	000**0**0000
This bit enables or disables the de-emphasis filter. The default coefficients are for 44.1 kHz sampling rate, but can be changed by reprogramming the appropriate coeffients via the coefficient spaces provided in each HybridFlow.	
De-emphasis filter is disabled	- - - 0 - - - -
De-emphasis filter is enabled	- - - 1 - - - -
SDOUT Select [0] (R/W)	**0000000**0
This bit selects what is being output as SDOUT via GPIO pins.	
SDOUT is the DSP output (post-processing)(1)	- - - - - - - 0
SDOUT is the DSP input (pre-processing)	- - - - - - - 1

(1) Some HybridFlows offer several paths from which to take the SDOUT signal. In this case, this bit should be cleared, and the appropirate mixer/mux function in the HybridFlow should be used to determine which processed signal should be presented as the SDOUT signal.

8.4.2.6 P0-R8

GPIO2 Output Enable [5] (R/W)	00**0**00000
This bit sets the direction of the GPIO2 pin	
GPIO2 is input	- - - 0 - - - - -
GPIO2 is output	- - - 1 - - - - -
GPIO0 Output Enable [3] (R/W)	**0000**0**000**
This bit sets the direction of the GPIO0 pin	
GPIO0 is input	- - - - - 0 - - -
GPIO0 is output	- - - - - 1 - - -
GPIO1 Output Enable [2] (R/W)	**00000**0**00**
This bit sets the direction of the GPIO1 pin	
GPIO1 is input	- - - - - 0 - -
GPIO1 is output	- - - - - 1 - -

8.4.2.7 P0-R9

SCLK Polarity [5] (R/W)	00**0**00000
This bit sets the inverted SCLK mode. In inverted SCLK mode, the DAC assumes that the LRCK/FS and SDIN edges are aligned to the rising edge of the SCLK. Normally they are assumed to be aligned to the falling edge of the SCLK.	
Normal SCLK mode	- - - 0 - - - - -
Inverted SCLK mode	- - - 1 - - - - -

SCLK Output Enable [4] (R/W)	00000000
This bit sets the SCLK pin direction to output for I2S master mode operation. In I^2S master mode the TAS5754M outputs the reference SCLK and LRCK/FS, and the external source device provides the SDIN according to these clocks. Use P0-R32 to program the division factor of the MCLK to yield the desired SCLK rate (normally $64F_S$)	
SCLK is input (I^2S slave mode)	- - - 0 - - - -
SCLK is output (I^2S master mode)	- - - 1 - - - -
LRCK/FS Output Enable [0] (R/W)	**0000000 0**
This bit sets the LRCK/FS pin direction to output for I2S master mode operation. In I2S master mode the PCM51xx outputs the reference SCLK and LRCK/FS, and the external source device provides the SDIN according to these clocks. Use P0/R33 to program the division factor of the SCLK to yield $1F_S$ for LRCK/FS.	
LRCK/FS is input (I^2S slave mode)	- - - - - - - 0
LRCK/FS is output (I^2S master mode)	- - - - - - - 1

8.4.2.8 P0-R12

Master Mode SCLK Divider Reset [1] (R/W)	0111110 0
This bit, when set to 0, will reset the MCLK divider to generate SCLK clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly.	
Master mode SCLK clock divider is reset	- - - - - - - 0 -
Master mode SCLK clock divider is functional	- - - - - - - 1 -
Master Mode LRCK/FS Divider Reset [0] (R/W)	**0111110 0**
This bit, when set to 0, will reset the SCLK divider to generate LRCK/FS clock for I2S master mode. To use I2S master mode, the divider must be enabled and programmed properly.	
Master mode LRCK/FS clock divider is reset	- - - - - - - 0
Master mode LRCK/FS clock divider is functional	- - - - - - - 1

8.4.2.9 P0-R13

PLL Reference [6:4] (R/W)	0000 0000
This bit select the source clock for internal PLL. This bit is ignored and overriden in clock auto set mode.	
The PLL reference clock is MCLK	- 0 0 0 - - - -
The PLL reference clock is MCLK	- 0 0 1 - - - -
Reserved	- 1 0 0 - - - -
The PLL reference clock is GPIO (selected using P0-R18)	- 1 1 1 - - - -

8.4.2.10 P0-R14

DAC Clock Source [6:4] (R/W)	0000 0000
These bits select the source clock for DAC clock divider.	
Master clock (PLL/MCLK and OSC auto-select)	- 0 0 0 - - - -
PLL clock	- 0 0 1 - - - -
Reserved	- 0 1 0 - - - -
MCLK clock	- 0 1 1 - - - -
SCLK clock others:	- 1 0 0 - - - -
Others: reserved (muted)	

8.4.2.11 P0-R18

GPIO Source for PLL Reference clock [2:0] (R/W)	00000 000
These bits select the GPIO pins as clock input source when GPIO is selected as the PLL reference clock source.	
Reserved	- - - - - 0 0 0
Reserved	- - - - - 0 0 1
GPIO1 functions as clock input source	- - - - - 0 1 0

GPIO Source for PLL Reference clock [2:0] (R/W)	00000000
GPIO0 functions as clock input source	- - - - - 0 1 1
Reserved	- - - - - 1 0 0
GPIO2 functions as clock input source	- - - - - 1 0 1
Others: reserved (muted)	

8.4.2.12 P0-R19

Synchronization Request [0] (R/W)	00010000
This bit, when set to 1 will issue the clock resynchronization by synchronously resets the DAC, CP and OSR clocks. The actual clock resynchronization takes place when this bit is set back to 0, where the DAC, CP and OSR clocks are resumed at the beginning of the audio frame.	
Resume DAC, CP and OSR clocks synchronized to the beginning of audio frame	- - - - - - - 0
Halt DAC, CP and OSR clocks as the beginning of re-synchronization process	- - - - - - - 1

8.4.2.13 P0-R20

PLL Divider P-Factor [3:0] (R/W)	00000000
These bits set the PLL divider P factor. These bits are ignored in clock auto set mode.	
Sets the PLL divider P factor to P=1	- - - - 0 0 0 0
Sets the PLL divider P factor to P=2	- - - - 0 0 0 1
Sets the PLL divider P factor to P=3	- - - - 0 0 1 0
...	...
Sets the PLL divider P factor to P=13	- - - - 1 1 0 0
Sets the PLL divider P factor to P=14	- - - - 1 1 0 1
Sets the PLL divider P factor to P=15	- - - - 1 1 1 0
Prohibited (do not set this value)	- - - - 1 1 1 1

8.4.2.14 P0-R21

PLL Divider J-Factor [4:0] (R/W)	00000000
These bits set the J part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.	
Prohibited (do not set this value)	- - - 0 0 0 0 0
Sets the J part if the overall PLL multiplication factor J.D * R to J = 1	- - - 0 0 0 0 1
Sets the J part if the overall PLL multiplication factor J.D * R to J = 2	- - - 0 0 0 1 0
Sets the J part if the overall PLL multiplication factor J.D * R to J = 3	- - - 0 0 0 1 1
...	...
Sets the J part if the overall PLL multiplication factor J.D * R to J = 61	- - - 1 1 1 0 1
Sets the J part if the overall PLL multiplication factor J.D * R to J = 62	- - - 1 1 1 1 0
Sets the J part if the overall PLL multiplication factor J.D * R to J = 63	- - - 1 1 1 1 1

8.4.2.15 P0-R22

PLL Divider D-Factor (Most Significant Bit) [5:0] (Least Significant Bit) [7:0] (R/W)	Decimal
These bits set the D part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.	
Sets the D part if the overall PLL multiplication factor J.D * R to D = 0000	0
Sets the D part if the overall PLL multiplication factor J.D * R to D = 0001	1
Sets the D part if the overall PLL multiplication factor J.D * R to D = 0010	2
...	...
Sets the D part if the overall PLL multiplication factor J.D * R to D = 9997	9997
Sets the D part if the overall PLL multiplication factor J.D * R to D = 9998	9998
Sets the D part if the overall PLL multiplication factor J.D * R to D = 9999	9999

8.4.2.16 P0-R24

PLL Divider R-Factor [3:0] (R/W)	00000000
These bits set the R part of the overall PLL multiplication factor J.D * R. These bits are ignored in clock auto set mode.	
Sets the R part if the overall PLL multiplication factor J.D * R to R = 1	- - - - 0 0 0 0
Sets the R part if the overall PLL multiplication factor J.D * R to R = 2	- - - - 0 0 0 1
Sets the R part if the overall PLL multiplication factor J.D * R to R = 3	- - - - 0 0 1 0
...	...
Sets the R part if the overall PLL multiplication factor J.D * R to R = 14	- - - - 1 1 0 1
Sets the R part if the overall PLL multiplication factor J.D * R to R = 15	- - - - 1 1 1 0
Sets the R part if the overall PLL multiplication factor J.D * R to R = 16	- - - - 1 1 1 1

8.4.2.17 P0-R27

DSP Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the DSP clock. These bits are ignored in clock auto set mode.	
These bits set the source clock divider value for the DSP clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the DSP clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the DSP clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the DSP clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the DSP clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the DSP clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.18 P0-R28

DAC Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the DAC clock. These bits are ignored in clock auto set mode.	
These bits set the source clock divider value for the DAC clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the DAC clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the DAC clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the DAC clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the DAC clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the DAC clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.19 P0-R29

NCP Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the CP clock. These bits are ignored in clock auto set mode.	
These bits set the source clock divider value for the NCP clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the NCP clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the NCP clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the NCP clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the NCP clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the NCP clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.20 P0-R30

OSR Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the OSR clock. These bits are ignored in clock auto set mode.	

OSR Clock Divider [6:0] (R/W)	00000000
These bits set the source clock divider value for the OSR clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the OSR clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the OSR clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the OSR clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the OSR clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the OSR clock. Divide by 128	- 1 1 1 1 1 1 1

8.4.2.21 P0-R32

Master Mode SCLK Divider [6:0] (R/W)	00000000
These bits set the MCLK divider value to generate I2S master SCLK clock.	
These bits set the source clock divider value for the SCLK clock. Divide by 1	- 0 0 0 0 0 0 0
These bits set the source clock divider value for the SCLK clock. Divide by 2	- 0 0 0 0 0 0 1
These bits set the source clock divider value for the SCLK clock. Divide by 3	- 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the SCLK clock. Divide by 126	- 1 1 1 1 1 0 1
These bits set the source clock divider value for the SCLK clock. Divide by 127	- 1 1 1 1 1 1 0
These bits set the source clock divider value for the SCLK clock Divide by 128	- 1 1 1 1 1 1 1

8.4.2.22 P0-R33

Master Mode LRCK/FS Divider [7:0] (R/W)	00000000
These bits set the I2S master SCLK clock divider value to generate I2S master LRCK/FS clock.	
These bits set the source clock divider value for the LRCK/FS clock. Divide by 1	0 0 0 0 0 0 0 0
These bits set the source clock divider value for the LRCK/FS clock. Divide by 2	0 0 0 0 0 0 0 1
These bits set the source clock divider value for the LRCK/FS clock. Divide by 3	0 0 0 0 0 0 1 0
...	...
These bits set the source clock divider value for the LRCK/FS clock. Divide by 254	1 1 1 1 1 1 0 1
These bits set the source clock divider value for the LRCK/FS clock. Divide by 255	1 1 1 1 1 1 1 0
These bits set the source clock divider value for the LRCK/FS clock. Divide by 256	1 1 1 1 1 1 1 1

8.4.2.23 P0-R34

16x Interpolation [4] (R/W)	00000000
This bit enables or disables the 16x interpolation mode	
8x interpolation	- - - 0 - - - -
16x interpolation	- - - 1 - - - -
Switching Frequency Speed Mode [1:0] (R/W)	**000000000**
These bits select the F_S operation mode, which must be set according to the current audio sampling rate. These bits are ignored in clock auto set mode.	
Single speed (f_{SW} ≤ 48 kHz)	- - - - - - 0 0
Double speed (48 kHz ≤ f_{SW} ≤ 96 kHz)	- - - - - - 0 1
Quad speed (96 kHz ≤ f_{SW} ≤ 192 kHz)	- - - - - - 1 0

8.4.2.24 P0-R35

Available DSP Clock Cycles (MSB) [7:0] (R/W)	00000001
These bits specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock F_S ratio. These bits are ignored in clock auto set mode.	
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 0

Available DSP Clock Cycles (MSB) [7:0] (R/W)	00000001
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 1
DSP clock:F_S ratio = x	0 0 0 0 0 0 1 0
...	...
DSP clock:F_S ratio = x	1 1 1 1 1 1 0 1
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 0
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 1

8.4.2.25 P0-R36

Available DSP Clock Cycles (LSB) [7:0] (R/W)	00000000
These bits specify the number of DSP clock cycles available in one audio frame. The value should match the DSP clock F_S ratio. These bits are ignored in clock auto set mode.	
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 0
DSP clock:F_S ratio = x	0 0 0 0 0 0 0 1
DSP clock:F_S ratio = x	0 0 0 0 0 0 1 0
...	...
DSP clock:F_S ratio = x	1 1 1 1 1 1 0 1
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 0
DSP clock:F_S ratio = x	1 1 1 1 1 1 1 1

8.4.2.26 P0-R37

Ignore F_S Detection [6] (R/W)	00000000
This bit controls whether to ignore the F_S detection. When ignored, F_S error will not cause a clock error.	
Regard F_S detection	- 0 - - - - - -
Ignore F_S detection	- 1 - - - - - -
Ignore SCLK Detection [5] (R/W)	**00000000**
This bit controls whether to ignore the SCLK detection against LRCK/FS. The SCLK must be stable between $32F_S$ and $256F_S$ inclusive or an error will be reported. When ignored, a SCLK error will not cause a clock error.	
Regard SCLK detection	- - 1 - - - - -
Ignore SCLK detection	- - 0 - - - - -
Ignore MCLK Detection [4] (R/W)	**00000000**
This bit controls whether to ignore the MCLK detection against LRCK/FS. Only some certain MCLK ratios within some error margin are allowed. When ignored, an MCLK error will not cause a clock error.	
Regard MCLK detection	- - - 0 - - - -
Ignore MCLK detection	- - - 1 - - - -
Ignore Clock Halt Detection [3] (R/W)	**00000000**
This bit controls whether to ignore the MCLK halt (static or frequency is lower than acceptable) detection. When ignored an MCLK halt will not cause a clock error.	
Regard MCLK halt detection	- - - - - - 0 -
Ignore MCLK halt detection	- - - - - - 1 -
Ignore LRCK/FS and SCLK Missing Detection [2] (R/W)	**00000000**
This bit controls whether to ignore the LRCK/FS and SCLK missing detection. The LRCK/FS and SCLK need to be in low state (not only static) to be deemed missing. When ignored an LRCK/FS and SCLK missing will not cause the DAC go into powerdown mode.	
Regard LRCK/FS and SCLK missing detection	- - - - - 0 - -
Ignore LRCK/FS and SCLK missing detection	- - - - - 1 - -
Disable Clock Divider Autoset [1] (R/W)	**00000000**
This bit enables or disables the clock auto set mode. When dealing with uncommon audio clock configuration, the auto set mode must be disabled and all clock dividers must be set manually. Addtionally, some clock detectors might also need to be disabled. The clock autoset feature will not work with PLL enabled in VCOM mode. In this case this feature has to be disabled and the clock dividers must be set manually.	
Enable clock auto set	- - - - - - 0 -

Disable Clock Divider Autoset [1] (R/W)	0000000**0**
Disable clock auto set	- - - - - - 1 -
Ignore PLL Lock Detection [0] (R/W)	**0000000**0
This bit controls whether to ignore the PLL lock detection. When ignored, PLL unlocks will not cause a clock error. The PLL lock flag at P0-R4, bit 4 is always correct regardless of this bit.	
PLL unlocks raise clock error	- - - - - - - 0
PLL unlocks are ignored	- - - - - - - 1

8.4.2.27 P0-R40

I^2S Data Format [5:4] (R/W)	00**00**0010
These bits control both input and output audio interface formats for DAC operation.	
Input and output audio interface formats for DAC operation is I^2S	- - 0 0 - - - -
Input and output audio interface formats for DAC operation is TDM/DSP	- - 0 1 - - - -
Input and output audio interface formats for DAC operation is RTJ	- - 1 0 - - - -
Input and output audio interface formats for DAC operation is LTJ	- - 1 1 - - - -
I^2S Word Length [1:0] (R/W)	**000000010**
These bits control both input and output audio interface sample word lengths for DAC operation.	
Input and output audio interface sample word length for DAC operation is 16 bits	- - - - - - 0 0
Input and output audio interface sample word length for DAC operation is 20 bits	- - - - - - 0 1
Input and output audio interface sample word length for DAC operation is 24 bits	- - - - - - 1 0
Input and output audio interface sample word length for DAC operation is 32 bits	- - - - - - 1 1

8.4.2.28 P0-R41

I^2S Shift [7:0] (R/W)	00000000
These bits control the offset of audio data in the audio frame for both input and output. The offset is defined as the number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample.	
Offset (number of SCLK from the starting (MSB) of audio frame to the starting of the desired audio sample) is 0 SCLK (no offset)	0 0 0 0 0 0 0 0
Offset is 1 SCLK	0 0 0 0 0 0 0 1
Offset is 2 SCLKs	0 0 0 0 0 0 1 0
...	...
Offset is 254 SCLKs	1 1 1 1 1 1 0 1
Offset is 255 SCLKs	1 1 1 1 1 1 1 0
Offset is 256 SCLKs	1 1 1 1 1 1 1 1

8.4.2.29 P0-R42

Channel B DAC Data Path [5:4] (R/W)	00**00**0001
These bits control the Channel B audio data path connection.	
Zero data (mute)	- - 0 0 - - - -
Channel B data	- - 0 1 - - - -
Channel A data	- - 1 0 - - - -
Reserved (do not set)	- - 1 1 - - - -
Channel A DAC Data Path [1:0] (R/W)	**000000001**
These bits control the Channel A audio data path connection.	
Zero data (mute)	- - - - - - 0 0
Channel A data	- - - - - - 0 1
Channel B data	- - - - - - 1 0
Reserved (do not set)	- - - - - - 1 1

8.4.2.30 P0-R43

DSP Program Selection [4:0] (R/W)	00000001
These bits select the DSP program to use for audio processing.	
Reserved (do not set)	- - - 0 0 0 0 0
8x, 4x, or 2x FIR interpolation filter with de-emphasis	- - - 0 0 0 0 1
8x, 4x, or 2x Low latency IIR interpolation filter with de-emphasis	- - - 0 0 0 1 0
16x FIR interpolation filter with de-emphasis	- - - 0 0 0 1 1
16x Low latency IIR interpolation filter with de-emphasis	- - - 0 0 1 0 0
Fixed process flow with configurable parameters	- - - 0 0 1 0 1
Reserved (do not set)	- - - 0 0 1 1 0
8× Ringing-less low latency FIR interpolation filter without de-emphasis	- - - 0 0 1 1 1
Others: Reserved (do not set)	...
User program in RAM	- - - 1 1 1 1 1

8.4.2.31 P0-R44

Clock Missing Detection Period [2:0] (R/W)	00000000
These bits set how long both SCLK and LRCK/FS keep low before the audio clocks deemed missing and the DAC transitions to powerdown mode.	
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 1 second	- - - - - 0 0 0
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 2 seconds	- - - - - 0 0 1
...	...
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 7 seconds	- - - - - 1 1 0
Period that SCLK and LRCK/FS are keep low before the audio clock is deemed missing and the DAC transitions to powerdown mode is approximately 8 seconds	- - - - - 1 1 1

8.4.2.32 P0-R59

Auto Mute Time for Channel B [6:4] (R/W)	00000000
These bits specify the length of consecutive zero samples at Channel B before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates.	
Length of consecutive zero samples before the channel can be auto muted is 21 ms	- 0 0 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 106 ms	- 0 0 1- - - -
Length of consecutive zero samples before the channel can be auto muted is 213 ms	- 0 1 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 533 ms	- 0 1 1 - - - -
Length of consecutive zero samples before the channel can be auto muted is 1.07 seconds	- 1 0 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 2.13 seconds	- 1 0 1 - - - -
Length of consecutive zero samples before the channel can be auto muted is 5.33 seconds	- 1 1 0 - - - -
Length of consecutive zero samples before the channel can be auto muted is 10.66 seconds	- 1 1 1 - - - -
Auto Mute Time for Channel A [2:0] (R/W)	**00000000**
These bits specify the length of consecutive zero samples at Channel A before the channel can be auto muted. The times shown are for 48 kHz sampling rate and will scale with other rates.	
Length of consecutive zero samples before the channel can be auto muted is 21 ms	- - - - - 0 0 0
Length of consecutive zero samples before the channel can be auto muted is 106 ms	- - - - - 0 0 1
Length of consecutive zero samples before the channel can be auto muted is 213 ms	- - - - - 0 1 0
Length of consecutive zero samples before the channel can be auto muted is 533 ms	- - - - - 0 1 1
Length of consecutive zero samples before the channel can be auto muted is 1.07 seconds	- - - - - 1 0 0
Length of consecutive zero samples before the channel can be auto muted is 2.13 seconds	- - - - - 1 0 1
Length of consecutive zero samples before the channel can be auto muted is 5.33 seconds	- - - - - 1 1 0

Auto Mute Time for Channel A [2:0] (R/W)	00000000
Length of consecutive zero samples before the channel can be auto muted is 10.66 seconds	- - - - - 1 1 1

8.4.2.33 P0-R60

Digital Volume Control [1:0] (R/W)	0000000 00
These bits control the behavior of the digital volume.	
The volume for Channels A and B are independent	- - - - - - 0 0
Channel A volume follows Channel B setting	- - - - - - 0 1
Channel B volume follows Channel A setting	- - - - - - 1 0
Reserved (The volume for Channels A and B are independent)	- - - - - - 1 1

8.4.2.34 P0-R61

Channel B Digital Volume [7:0] (R/W)	00110000
These bits control the Channel B digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.	
Channel B digital volume is 24 dB	0 0 0 0 0 0 0 0
Channel B digital volume is 23.5 dB	0 0 0 0 0 0 0 1
Channel B digital volume is 23 dB.	0 0 0 0 0 0 1 0
...	...
Channel B digital volume is 0.5 dB	0 0 1 0 0 0 0 0
Channel B digital volume is 0 dB	0 0 1 1 0 0 0 0
Channel B digital volume is –0.5 dB	0 0 1 1 0 0 0 1
...	...
Channel B digital volume is –102.5 dB	1 1 1 1 1 1 0 1
Channel B digital volume is –103 dB	1 1 1 1 1 1 1 0
Reserved	1 1 1 1 1 1 1 1

8.4.2.35 P0-R62

Channel A Digital Volume [7:0] (R/W)	00110000
These bits control the Channel A digital volume. The digital volume is 24 dB to -103 dB in -0.5 dB step.	
Channel A digital volume is 24 dB	0 0 0 0 0 0 0 0
Channel A digital volume is 23.5 dB	0 0 0 0 0 0 0 1
Channel A digital volume is 23 dB.	0 0 0 0 0 0 1 0
...	...
Channel A digital volume is 0.5 dB	0 0 1 0 0 0 0 0
Channel A digital volume is 0 dB	0 0 1 1 0 0 0 0
Channel A digital volume is –0.5 dB	0 0 1 1 0 0 0 1
...	...
Channel A digital volume is –102.5 dB	1 1 1 1 1 1 0 1
Channel A digital volume is –103 dB	1 1 1 1 1 1 1 0
Reserved	1 1 1 1 1 1 1 1

8.4.2.36 P0-R63

Digital Volume Normal Ramp-Down Frequency [7:6] (R/W)	00100010
These bits control the frequency of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by SPK_MUTE pin or P0-R3.	
The frequency of the digital volume updates is every 1 F_S period	0 0 - - - - - -
The frequency of the digital volume updates is every 2 F_S period	0 1 - - - - - -
The frequency of the digital volume updates is every 4 F_S period	1 0 - - - - - -

Digital Volume Normal Ramp-Down Frequency [7:6] (R/W)	00100010
Directly sets the volume to zero (Instant mute)	1 1 - - - - - -
Digital Volume Normal Ramp Down Step [5:4] (R/W)	**00100010**
These bits control the step of the digital volume updates when the volume is ramping down. The setting here is applied to soft mute request, asserted by SPK_MUTE pin or P0-R3.	
Decrement by 4 dB for each update	- - 0 0 - - - -
Decrement by 2 dB for each update	- - 0 1 - - - -
Decrement by 1 dB for each update	- - 1 0 - - - -
Decrement by 0.5 dB for each update	- - 1 1 - - - -
Digital Volume Normal Ramp-Up Frequency [3:2] (R/W)	**00100010**
These bits control the frequency of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by SPK_MUTE pin or P0-R3.	
The frequency of the digital volume updates is every 1 F_S period	- - - - 0 0 - -
The frequency of the digital volume updates is every 2 F_S period	- - - - 0 1 - -
The frequency of the digital volume updates is every 4 F_S period	- - - - 1 0 - -
Directly sets the volume to zero (Instant unmute)	- - - - 1 1 - -
Digital Volume Normal Ramp Up Step [1:0] (R/W)	**00100010**
These bits control the step of the digital volume updates when the volume is ramping up. The setting here is applied to soft unmute request, asserted by SPK_MUTE pin or P0-R3.	
Increment by 4 dB for each update	- - - - - - 0 0
Increment by 2 dB for each update	- - - - - - 0 1
Increment by 1 dB for each update	- - - - - - 1 0
Increment by 0.5 dB for each update	- - - - - - 1 1

8.4.2.37 P0-R64

Digital Volume Emergency Ramp Down Frequency [7:6] (R/W)	00000010
These bits control the frequency of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.	
The frequency of the digital volume updates is every 1 F_S period	0 0 - - - - - -
The frequency of the digital volume updates is every 2 F_S period	0 1 - - - - - -
The frequency of the digital volume updates is every 4 F_S period	1 0 - - - - - -
Directly sets the volume to zero (Instant mute)	1 1 - - - - - -
Digital Volume Emergency Ramp Down Step [5:4] (R/W)	**00000010**
These bits control the step of the digital volume updates when the volume is ramping down due to clock error or power outage, which usually needs faster ramp down compared to normal soft mute.	
Decrement by 4 dB for each update	- - 0 0 - - - -
Decrement by 2 dB for each update	- - 0 1 - - - -
Decrement by 1 dB for each update	- - 1 0 - - - -
Decrement by 0.5 dB for each update	- - 1 1 - - - -

8.4.2.38 P0-R65

Auto Mute Control [2] (R/W)	00000100
This bit controls the behavior of the auto mute upon zero sample detection. The time length for zero detection is set with P0-R59.	
Auto mute Channel B and Channel A independently	- - - - - 0 - -
Auto mute Channels A and Channel B only when both channels are about to be auto muted	- - - - - 1 - -
Auto Mute Channel B [1] (R/W)	**00000100**
This bit enables or disables auto mute on Channel A. Note that when Channel A auto mute is disabled and the P0-R65, bit 2 is set to 1, the Channel B will also never be auto muted.	
Disable Channel A auto mute	- - - - - - - 0 -
Enable Channel A auto mute	- - - - - - - 1 -

Auto Mute Channel A [0] (R/W)	00000100
This bit enables or disables auto mute on Channel B. Note that when Channel B auto mute is disabled and the P0-R65, bit 2 is set to 1, the Channel A will also never be auto muted.	
Disable Channel B auto mute	- - - - - - - 0
Enable Channel B auto mute	- - - - - - - 1

8.4.2.39 P0-R82

GPIO1 Output Selection [4:0] (R/W)	00000000
These bits select the signal to output to GPIO1. To actually output the selected signal, the GPIO1 must be set to output mode at P0-R8.	
Off (low)	- - - 0 0 0 0 0
DSP GPIO1 output	- - - 0 0 0 0 1
Register GPIO1 output (P0-R86, bit 2)	- - - 0 0 0 1 0
Auto mute flag (asserted when both Channel A and Channel B are auto muted)	- - - 0 0 0 1 1
Auto mute flag for Channel B	- - - 0 0 1 0 0
Auto mute flag for Channel A	- - - 0 0 1 0 1
Clock invalid flag (clock error or clock changing or clock missing)	- - - 0 0 1 1 0
Serial audio interface data output (SDOUT)	- - - 0 0 1 1 1
Analog mute flag for Channel B (low active)	- - - 0 1 0 0 0
Analog mute flag for Channel A (low active)	- - - 0 1 0 0 1
PLL lock flag	- - - 0 1 0 1 0
Charge pump clock	- - - 0 1 0 1 1
Reserved	- - - 0 1 1 0 0
Reserved	- - - 0 1 1 0 1
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.7 DVDD	- - - 0 1 1 1 0
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.3 DVDD	- - - 0 1 1 1 1
PLL Output/4 (Requires Clock Flex Register)	- - - 1 0 0 0 0
Others: reserved	

8.4.2.40 P0-R83

GPIO0 Output Selection [4:0] (R/W)	00000000
These bits select the signal to output to GPIO0. To actually output the selected signal, the GPIO0 must be set to output mode at P0-R8.	
Off (low)	- - - 0 0 0 0 0
DSP GPIO0 output	- - - 0 0 0 0 1
Register GPIO0 output (P0-R86, bit 2)	- - - 0 0 0 1 0
Auto mute flag (asserted when both Channel A and Channel B are auto muted)	- - - 0 0 0 1 1
Auto mute flag for Channel B	- - - 0 0 1 0 0
Auto mute flag for Channel A	- - - 0 0 1 0 1
Clock invalid flag (clock error or clock changing or clock missing)	- - - 0 0 1 1 0
Serial audio interface data output (SDOUT)	- - - 0 0 1 1 1
Analog mute flag for Channel B (low active)	- - - 0 1 0 0 0
Analog mute flag for Channel A (low active)	- - - 0 1 0 0 1
PLL lock flag	- - - 0 1 0 1 0
Charge pump clock	- - - 0 1 0 1 1
Reserved	- - - 0 1 1 0 0
Reserved	- - - 0 1 1 0 1
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.7 DVDD	- - - 0 1 1 1 0
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.3 DVDD	- - - 0 1 1 1 1
PLL Output/4 (Requires Clock Flex Register)	- - - 1 0 0 0 0
Others: reserved	

8.4.2.41 P0-R85

GPIO2 Output Selection [4:0] (R/W)	00000000
These bits select the signal to output to GPIO2. To actually output the selected signal, the GPIO2 must be set to output mode at P0-R8.	
Off (low)	- - - 0 0 0 0 0
DSP GPIO2 output	- - - 0 0 0 0 1
Register GPIO2 output (P0-R86, bit 5)	- - - 0 0 0 1 0
Auto mute flag (asserted when both Channels A and B are auto muted)	- - - 0 0 0 1 1
Auto mute flag for Channel B	- - - 0 0 1 0 0
Auto mute flag for Channel A	- - - 0 0 1 0 1
Clock invalid flag (clock error or clock changing or clock missing)	- - - 0 0 1 1 0
Serial audio interface data output (SDOUT)	- - - 0 0 1 1 1
Analog mute flag for Channel B (low active)	- - - 0 1 0 0 0
Analog mute flag for Channel A (low active)	- - - 0 1 0 0 1
PLL lock flag	- - - 0 1 0 1 0
Charge pump clock	- - - 0 1 0 1 1
Reserved	- - - 0 1 1 0 0
Reserved	- - - 0 1 1 0 1
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.7 DVDD	- - - 0 1 1 1 0
Under voltage flag, asserted when SPK_MUTE voltage is higher than 0.3 DVDD	- - - 0 1 1 1 1
PLL Output/4 (Requires Clock Flex Register)	- - - 1 0 0 0 0
Others: reserved	

8.4.2.42 P0-R86

GPIO2 Output Control [5] (R/W)	00000000
This bit controls the GPIO2 output when the selection at P0-R85 is set to 0010 (register output).	
Output low	- - - 0 - - - - -
Output high	- - - 1 - - - - -
GPIO0 Output Control [3] (R/W)	**00000000**
This bit controls the GPIO0 output when the selection at P0-R83 is set to 0010 (register output).	
Output low	- - - - - 0 - - -
Output high	- - - - - 1 - - -
GPIO1 Output Control [2] (R/W)	**00000000**
This bit controls the GPIO1 output when the selection at P0-R82 is set to 0010 (register output).	
Output low	- - - - - 0 - -
Output high	- - - - - 1 - -

8.4.2.43 P0-R87

GPIO2 Output Inversion [5] (R/W)	00000000
This bit controls the polarity of GPIO2 output. When set to 1, the output is inverted for any signal being selected.	
Non-inverted	- - - 0 - - - - -
Inverted	- - - 1 - - - - -
GPIO0 Output Inversion [3] (R/W)	**00000000**
This bit controls the polarity of GPIO0 output. When set to 1, the output is inverted for any signal being selected.	
Non-inverted	- - - - - 0 - - -
Inverted	- - - - - 1 - - -

GPIO1 Output Inversion [2] (R/W)	00000000
This bit controls the polarity of GPIO1 output. When set to 1, the output is inverted for any signal being selected.	
Non-inverted	- - - - - 0 - -
Inverted	- - - - - 1 - -

8.4.2.44 P0-R90

Channel B-1 Overflow [4] (Read Only)	00000000
This bit indicates whether the Channel B of DSP first output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - 0 - - - -
Overflow occurred	- - - 1 - - - -
Channel A-1 Overflow [3] (Read Only)	**00000000**
This bit indicates whether the Channel A of DSP first output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - - - 0 - - -
Overflow occurred	- - - - - 1 - - -
Channel B-2 Overflow [2] (Read Only)	**00000000**
This bit indicates whether the Channel B of DSP second output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - - - 0 - -
Overflow occurred	- - - - - 1 - -
Channel A-2 Overflow [1] (Read Only)	**00000000**
This bit indicates whether the Channel A of DSP second output port has overflow. This bit is sticky and is cleared when read.	
No overflow	- - - - - - - 0 -
Overflow occurred	- - - - - - - 1 -
Shifter Overflow [0] (Read Only)	**00000000**
This bit indicates whether overflow occurred in the DSP shifter (possible sample corruption). This bit is sticky and is cleared when read.	
No overflow	- - - - - - - 0
Overflow occurred	- - - - - - - 1

8.4.2.45 P0-R91

Detected F_S [6:4] (Read Only)	00111000
These bits indicate the currently detected audio sampling rate.	
Error (out-of-valid range)	- 0 0 0 - - - -
8 kHz	- 0 0 1 - - - -
16 kHz	- 0 1 0 - - - -
32 kHz to 48 kHz	- 0 1 1 - - - -
88.2 kHz to 96 kHz	- 1 0 0 - - - -
176.4 kHz to 192 kHz	- 1 0 1 - - - -
Reserved	- 1 1 1 - - - -
Detected MCLK Ratio [3:0] (Read Only)	**00111000**
These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz.	
Ratio error (The MCLK ratio is not allowed)	- - - - 0 0 0 0
MCLK = 32 F_S	- - - - 0 0 0 1
MCLK = 48 F_S	- - - - 0 0 1 0
MCLK = 64 F_S	- - - - 0 0 1 1
MCLK = 128 F_S	- - - - 0 1 0 0
MCLK = 192 F_S	- - - - 0 1 0 1
MCLK = 256 F_S	- - - - 0 1 1 0
MCLK = 384 F_S	- - - - 0 1 1 1

Detected MCLK Ratio [3:0] (Read Only)	00111000
MCLK = 512 F_S	- - - - 1 0 0 0
MCLK = 768 F_S	- - - - 1 0 0 1
MCLK = 1024 F_S	- - - - 1 0 1 0
MCLK = 1152 F_S	- - - - 1 0 1 1
MCLK = 1536 F_S	- - - - 1 1 0 0
MCLK = 2048 F_S	- - - - 1 1 0 1
MCLK = 3072 F_S	- - - - 1 1 1 0

8.4.2.46 P0-R92

Detected SCLK Ratio [0] (Read Only)	00000000
This bit is the MSB of the 9 bit word that describes the currently detected SCLK to LRCK/FS Ratio. Binary to decimal conversion gives ratio.	
Decode with P0-93 to determine value.	- - - - - - - 0
	- - - - - - - 1

8.4.2.47 P0-R93

Detected SCLK Ratio [7:0] (Read Only)	00000000
These bits are bit 1 through bit 8 of the 9 bit word that describes the currently detected SCLK to LRCK/FS Ratio. Binary to decimal conversion gives ratio.	
LSB of 9 bit word	- - - - - - - 0
2nd LSB of 9 bit word	- - - - - - 0 -
...	...
2nd MSB of 9 bit word (MSB is found in P0-R92-B0)	0 - - - - - - -
Detected MCLK Ratio [3:0] (Read Only)	**00111000**
These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz.	
These bits indicate the currently detected MCLK ratio. Note that even if the MCLK ratio is not indicated as error, clock error might still be flagged due to incompatible combination with the sampling rate. Specifically the MCLK ratio must be high enough to allow enough DSP cycles for minimal audio processing when PLL is disabled. The absolute MCLK frequency must also be lower than 50 MHz. Ratio error (The MCLK ratio is not allowed)	- - - - 0 0 0 0
MCLK = 32 F_S	- - - - 0 0 0 1
MCLK = 48 F_S	- - - - 0 0 1 0
MCLK = 64 F_S	- - - - 0 0 1 1
MCLK = 128 F_S	- - - - 0 1 0 0
MCLK = 192 F_S	- - - - 0 1 0 1
MCLK = 256 F_S	- - - - 0 1 1 0
MCLK = 384 F_S	- - - - 0 1 1 1
MCLK = 512 F_S	- - - - 1 0 0 0
MCLK = 768 F_S	- - - - 1 0 0 1
MCLK = 1024 F_S	- - - - 1 0 1 0
MCLK = 1152 F_S	- - - - 1 0 1 1
MCLK = 1536 F_S	- - - - 1 1 0 0
MCLK = 2048 F_S	- - - - 1 1 0 1
MCLK = 3072 F_S	- - - - 1 1 1 0

8.4.2.48 P0-R94

Clock Detector Status [6] (Ready Only)	00000000
This bit indicates whether the MCLK clock is present or not.	
MCLK is present	- 0 - - - - - -

Clock Detector Status [6] (Ready Only)	00000000
MCLK is missing (halted)	- 1 - - - - - -
Clock Detector Status 5 [5] (Ready Only)	**00000000**
This bit indicates whether the PLL is locked or not. The PLL will be reported as unlocked when it is disabled.	
PLL is locked	- - 1 - - - - -
PLL is unlocked	- - 0 - - - - -
Clock Detector Status 4 [4] (Ready Only)	**00000000**
This bit indicates whether the both LRCK/FS and SCLK are missing (tied low) or not.	
LRCK/FS and/or SCLK is present	- - - 0 - - - -
LRCK/FS and SCLK are missing	- - - 1 - - - -
Clock Detector Status 3 [3] (Read Only)	**00000000**
This bit indicates whether the combination of current sampling rate and MCLK ratio is valid for clock auto set.	
The combination of FS:MCLK ratio is valid	- - - - - 0 - - -
Error (clock auto set is not possible)	- - - - - 1 - - -
Clock Detector Status 2 [2] (Read Only)	**00000000**
This bit indicates whether the MCLK is valid or not. The MCLK ratio must be detectable to be valid. There is a limitation with this flag, that is, when the low period of LRCK/FS is less than or equal to 5 SCLKs, this flag will be asserted (MCLK invalid reported).	
MCLK is valid	- - - - - 0 - -
MCLK is invalid	- - - - - 1 - -
Clock Detector Status 1 [1] (Read Only)	**00000000**
This bit indicates whether the SCLK is valid or not. The SCLK ratio must be stable and in the range of 32-256F_S to be valid.	
SCLK is valid	- - - - - - - 0 -
SCLK is invalid	- - - - - - - 1 -
Clock Detector Status 0 [0] (Read Only)	**00000000**
This bit indicated whether the audio sampling rate is valid or not. The sampling rate must be detectable to be valid. There is a limitation with this flag, that is when this flag is asserted and P0-R37 is set to ignore all asserted error flags such that the DAC recovers, this flag will be de-asserted (sampling rate invalid not reported anymore).	
Sampling rate is valid	- - - - - - - 0
Sampling rate is invalid	- - - - - - - 1

8.4.2.49 P0-R95

Latched Clock Halt [4] (Ready Only)	00000000
This bit indicates whether MCLK halt has occurred. The bit is cleared when read.	
MCLK halt has not occurred	- - - 0 - - - -
MCLK halt has occurred since last read	- - - 1 - - - -
Clock Missing [2] (Read Only)	**00000000**
This bit indicates whether the LRCK/FS and SCLK are missing (tied low).	
One or both of LRCK/FS SCLK is present	- - - - - 0 - -
Both LRCK/FS and SCLK are missing	- - - - - 1 - -
Clock Resync Request [1] (Read Only)	**00000000**
This bit indicates whether the clock resynchronization is in progress.	
Not resynchronizing	- - - - - - - 0 -
Clock resynchronization is in progress	- - - - - - - 1 -
Clock Error [0] (Read Only)	**00000000**
This bit indicates whether a clock error is being reported.	
Clock is valid	- - - - - - - 0
Clock is invalid (Error)	- - - - - - - 1

8.4.2.50 P0-R108

Channel B Analog Mute Monitor [1] (Read Only)	00110011
This bit is a monitor for Channel B analog mute status.	
Mute	- - - - - - - 0 -
Unmute	- - - - - - - 1 -
Channel A Analog Mute Monitor [0] (Read Only)	**00110011**
This bit is a monitor for Channel A analog mute status.	
Mute	- - - - - - - 0
Unmute	- - - - - - - 1

8.4.2.51 P0-R109

Short Detect Monitor [4] (Ready Only)	00000000
This bit indicates whether line output short is occurring on the DAC_OUTx line.	
Normal (No short)	- - - 0 - - - -
Line output is being shorted	- - - 1 - - - -
Short Detected Monitor [0] (Read Only)	**00000000**
This bit indicates whether line output short on DAC_OUTx has occurred since last read. This bit is sticky and is cleared when read.	
No short	- - - - - - - 0
Line output short occurred	- - - - - - - 1

8.4.2.52 P0-R114

SPK_MUTE Decoder Status[1:0] (Read Only)	00000000
These bits indicate the output of the SPK_MUTE level decoder for monitoring purpose.	
VDD > SPK_MUTE	- - - - - - 0 0
VDD ≤ SPK_MUTE < 0.7 × VDD	- - - - - - 0 1
Reserved (do not set)	- - - - - - 1 0
0.7 × VDD ≤ SPK_MUTE	- - - - - - 1 1

8.4.2.53 P0-R115

F_S Speed Mode Monitor [1:0] (Read Only)	00000000
These bits indicate the actual F_S operation mode being used. The actual value is the auto set one when clock auto set is active and register set one when clock auto set is disabled.	
Single speed (f_S ≤ 48 kHz)	- - - - - - 0 0
Double speed (48 kHz ≤ f_S ≤ 96 kHz)	- - - - - - 0 1
Quad speed (96 kHz ≤ f_S ≤ 192 kHz)	- - - - - - 1 0

8.4.2.54 P0-R117

DSP Boot Done Flag [7] (R/W)	00000000
This bit indicates whether the DSP boot is completed.	
DSP is booting	0 - - - - - - -
DSP boot completed	1 - - - - - - -
Power State [3:0] (Read Only)	**00000000**
These bits indicate the current power state of the DAC	
Powerdown	- - - - 0 0 0 0
Wait for CP voltage valid	- - - - 0 0 0 1
Calibration	- - - - 0 0 1 0
Calibration	- - - - 0 0 1 1

Power State [3:0] (Read Only)	00000000
Volume ramp up	- - - - 0 1 0 0
Run (Playing)	- - - - 0 1 0 1
Line output short or low impedance	- - - - 0 1 1 0
Volume ramp down	- - - - 0 1 1 1
Standby	- - - - 1 0 0 0

8.4.2.55 P0-R119

GPIO2 Input State [5] (Read Only)	00101101
This bit indicates the logic level at GPIO2 pin.	
GPIO2 logic level low	- - - 0 - - - - -
GPIO2 logic level high	- - - 1 - - - - -
GPIO0 Input State [3] (Read Only)	**00101101**
This bit indicates the logic level at GPIO0 pin.	
GPIO0 logic level low	- - - - - 0 - - -
GPIO0 logic level high	- - - - - 1 - - -
GPIO1 Input State [2] (Read Only)	**00101101**
This bit indicates the logic level at GPIO1 pin.	
GPIO1 logic level low	- - - - - 0 - -
GPIO1 logic level high	- - - - - 1 - -

8.4.2.56 P0-R120

Auto Mute Flag for Channel B [4] (Read Only)	00000000
This bit indicates the auto mute status for Channel B.	
Not auto muted	- - - 0 - - - -
Auto muted	- - - 1 - - - -
Auto Mute Flag for Channel A [0] (Read Only)	**00000000**
This bit indicates the auto mute status for Channel A.	
Not auto muted	- - - - - - - 0
Auto muted	- - - - - - - 1

8.4.2.57 P0-R121

DAC Mode [0] (R/W)	00000000
This bit controls the DAC mode.	
Mode1	- - - - - - - 0
Mode2	- - - - - - - 1

8.4.2.58 P1-R2

Analog Gain Control for Channel B [4] (R/W)	00000000
This bit controls the Channel B analog gain.	
0 dB	- - - 0 - - - -
–6 dB	- - - 1 - - - -
Analog Gain Control for Channel A [0] (R/W)	**00000000**
This bit controls the Channel A analog gain.	
0 dB	- - - - - - - 0
–6 dB	- - - - - - - 1

8.4.2.59 P1-R5

External UVP Control [1] (R/W)	00010001
This bit enables or disables detection of power supply drop via SPK_MUTE pin (external UVLO protection).	
Enabled	- - - - - - - 0 -
Disabled	- - - - - - - 1 -
Internal UVP Control [0] (R/W)	**00010001**
This bit enables or disables internal detection of AVDD voltage drop (internal UVLO protection).	
Enabled	- - - - - - - 0
Disabled	- - - - - - - 1

8.4.2.60 P1-R6

Analog Mute Control [0] (R/W)	00000000
This bit enables or disables analog mute following digital mute.	
Enabled	- - - - - - - 0
Disabled	- - - - - - - 1

8.4.2.61 P1-R7

Analog +10% Gain for Channel B [4] (R/W)	00000000
This bit enables or disables amplitude boost mode for Channel B.	
Normal amplitude	- - - 0 - - - -
+10% (+0.8 dB) boosted amplitude	- - - 1 - - - -
Analog +10% Gain for Channel A [0] (R/W)	**00000000**
This bit enables or disables amplitude boost mode for Channel A.	
Normal amplitude	- - - - - - - 0
+10% (+0.8 dB) boosted amplitude	- - - - - - - 1

8.4.2.62 P1-R8

VCOM Reference Ramp-Up [0] (R/W)	00000000
This bit controls the VCOM voltage ramp up speed.	
Normal ramp-up time is approximately 600 ms with external capacitance = 1 µF	- - - - - - - 0
Fast ramp-up time is approximately 3 ms with external capacitance = 1 µF	- - - - - - - 1

8.4.2.63 P1-R9

VCOM Power-Down Control [0] (R/W)	00000000
This bit controls VCOM powerdown switch.	
VCOM is powered on	- - - - - - - 0
VCOM is powered down	- - - - - - - 1

8.4.2.64 P44-R1

Active CRAM Monitor [3] (Read Only)	00000000
This bit indicates which CRAM is being accessed by the DSP when adaptive mode is disabled. When adaptive mode is enabled, this bit has no meaning.	
CRAM A is being used by the DSP	- - - - - 0 - - -
CRAM B is being used by the DSP	- - - - - 1 - - -

Adaptive Mode Control [2] (R/W)	00000000
This bit controls the DSP adaptive mode. When in adaptive mode, only CRAM A is accessible via serial interface when the DSP is disabled (DAC in standby state), while when the DSP is enabled (DAC is run state) the CRAM A can only be accessed by the DSP and the CRAM B can only be accessed by the serial interface, or vice versa depending on the value of CRAMSTAT. When not in adaptive mode, both CRAM A and B can be accessed by the serial interface when the DSP is disabled, but when the DSP is enabled, no CRAM can be accessed by serial interface. The DSP can access either CRAM, which can be monitored at SWPMON.	
Adaptive mode disabled	- - - - - 0 - -
Adaptive mode enabled	- - - - - 1 - -
Active CRAM Selection [1] (Read Only)	**00000000**
This bit indicates which CRAM currently serves as the active one. The other CRAM serves as an update buffer, and can accessed by serial interface (SPI/I^{2}C)	
CRAM A is active and being used by the DSP	- - - - - - - 0 -
CRAM B is active and being used by the DSP	- - - - - - - 1 -
Switch Active CRAM [0] (R/W)	**00000000**
This bit is used to request switching roles of the two buffers, (switching the active buffer role between CRAM A and CRAM B). This bit is cleared automatically when the switching process completed.	
No switching requested or switching completed	- - - - - - - 0
Switching is being requested	- - - - - - - 1

8.4.2.65 P253-R63

Clock Flex Register No. 1 [7:0] (R/W)	00000000
Using this register allows the PLL I/O to be set to GPIOs.	
Set to 0x11	0 0 0 0 0 0 0 0
	0 0 0 0 0 0 0 1
	0 0 0 0 0 0 1 0
...	...
	0 0 1 0 0 0 0 0
	0 0 1 1 0 0 0 0
	0 0 1 1 0 0 0 1
	...
	1 1 1 1 1 1 0 1
	1 1 1 1 1 1 1 0
	1 1 1 1 1 1 1 1

8.4.2.66 P253-R64

Clock Flex Register No. 2 [7:0] (R/W)	00000000
Using this register allows the PLL I/O to be set to GPIOs.	
Set to 0x11	0 0 0 0 0 0 0 0
	0 0 0 0 0 0 0 1
	0 0 0 0 0 0 1 0
...	...
	0 0 1 0 0 0 0 0
	0 0 1 1 0 0 0 0
	0 0 1 1 0 0 0 1
	...
	1 1 1 1 1 1 0 1
	1 1 1 1 1 1 1 0
	1 1 1 1 1 1 1 1

9 Applications and Implementation

9.1 Application Information

One of the most significant benefits of the TAS5754M device is the ability to be used in a variety of applications and with an assortment of signal processing options. This section details the information needed to configure the device for several popular configurations and provides guidance on integrating the TAS5754M device into the larger system.

9.1.1 External Component Selection Criteria

The *Supporting Component Requirements* table in each application description section lists the details of the supporting required components in each of the *System Application Schematics*.

Where possible, the supporting component requirements have been consolidated to minimize the number of unique components which are used in the design. Component list consolidation is a method to reduce the number of unique part numbers in a design, to ease inventory management, and reduce the manufacturing steps during board assembly. For this reason, some capacitors are specified at a higher voltage than what would normally be required. An example of this is a 50-V capacitor may be used for decoupling of a 3.3-V power supply net.

In this example, a higher voltage capacitor can be used even on the lower voltage net to consolidate all caps of that value into a single component type. Similarly, a several unique resistors, having all the same size and value but with different power ratings can be consolidated by using the highest rated power resistor for each instance of that resistor value.

While this consolidation may seem excessive, the benefits of having fewer components in the design may far outweigh the trivial cost of a higher voltage capacitor. If lower voltage capacitors are already available elsewhere in the design, they can be used instead of the higher voltage capacitors. In all situations, the voltage rating of the capacitors must be at least 1.45 times the voltage of the voltage which appears across them. The power rating of the capacitors should be 1.5 times to 1.75 times the power dissipated in it during normal use case.

9.1.2 Component Selection Impact on Board Layout, Component Placement, and Trace Routing

Because the layout is important to the overall performance of the circuit, the package size of the components shown in the component list were intentionally chosen to allow for proper board layout, component placement, and trace routing. In some cases, traces are passed in between two surface mount pads or ground plane extends from the TAS5754M device between two pads of a surface mount component and into to the surrounding copper for increased heat-sinking of the device. While components may be offered in smaller or larger package sizes, it is highly recommended that the package size remain identical to that used in the application circuit as shown. This consistency ensures that the layout and routing can be matched very closely, optimizing thermal, electromagnetic, and audio performance of the TAS5754M device in circuit in the final system.

9.1.3 Amplifier Output Filtering

The TAS5754M device is often used with a low-pass filter, which is used to filter out the carrier frequency of the PWM modulated output. This filter is frequently referred to as the *L-C Filter*, due to the presence of an inductive element *L* and a capacitive element *C* to make up the 2-pole filter.

The L-C filter removes the carrier frequency, reducing electromagnetic emissions and smoothing the current waveform which is drawn from the power supply. The presence and size of the L-C filter is determined by several system level constraints. In some low-power use cases that do not have other circuits which are sensitive to EMI, a simple ferrite bead or ferrite bead and capacitor can replace the traditional large inductor and capacitor that are commonly used. In other high-power applications, large toroid inductors are required for maximum power and film capacitors may be preferred due to audio characteristics. Refer to the application report SLOA119 for a detailed description on proper component selection and design of an L-C filter based upon the desired load and response.

9.2 Typical Applications

9.2.1 2.0 (Stereo BTL) System

For the stereo (BTL) PCB layout, see Figure 87.

A 2.0 system generally refers to a system in which there are two full range speakers without a separate amplifier path for the speakers which reproduce the low-frequency content. In this system, two channels are presented to the amplifier via the digital input signal. These two channels are amplified and then sent to two separate speakers. In some cases, the amplified signal is further separated based upon frequency by a passive crossover network after the L-C filter. Even so, the application is considered 2.0.

Most commonly, the two channels are a pair of signals called a *stereo pair*, with one channel containing the audio for the left channel and the other channel containing the audio for the right channel. While certainly the two channels can contain any two audio channels, such as two surround channels of a multi-channel speaker system, the most popular occurrence in two channels systems is a stereo pair.

It is important to note that the HybridFlows which have been developed for specifically for stereo applications will frequently apply the same equalizer curves to the left channel and the right channel. This maximizes the processing capabilities of each HybridFlow by minimizing the cycles required by the BiQuad filters.

When two signals that are not two separate signals, but instead are derived from a single signal which is separated into low frequency and high frequency by the signal processor, the application is commonly referred to as 1.1 or *Bi-Amped* systems. The 2.0 (Stereo BTL) System application is shown in Figure 80.

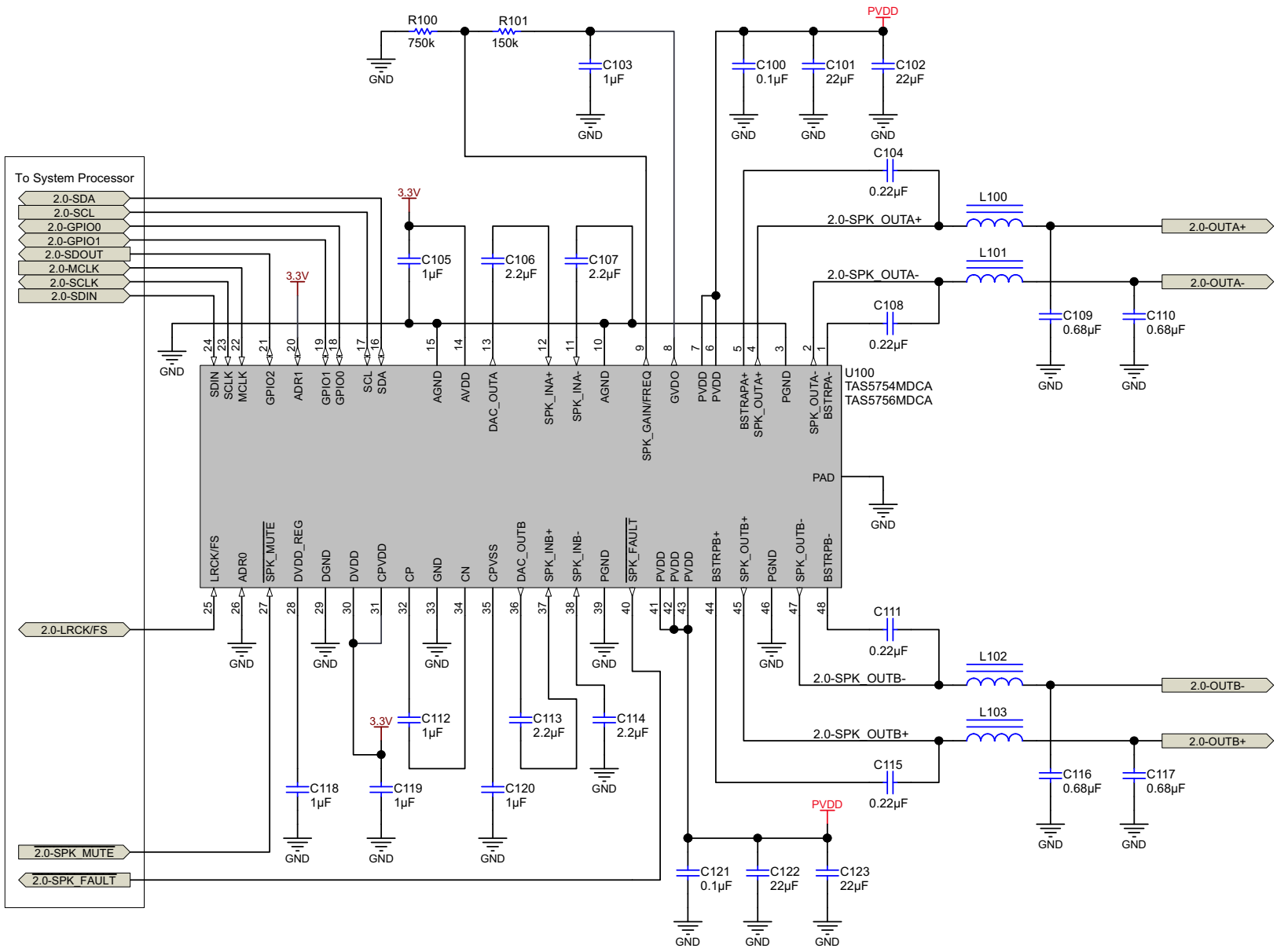


Figure 80. 2.0 (Stereo BTL) System Application Schematic

9.2.1.1 Design Requirements

- Power Supplies:
  - 3.3-V Supply
  - 5-V to 24-V Supply
- Communication: Host Processor serving as I^2C Compliant Master
- External Memory (such as EEPROM and Flash) used for coefficients and RAM portions of HybridFlow < 5 kB

The requirements for the supporting components for the TAS5754M device in a Mono (PBTL) System is provided in Table 22.

Table 22. Supporting Component Requirements for Stereo 2.0 (BTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U100	TAS5754M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier with HybridFlow processing
R100	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
R101	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
L100, L101, L102, L103	See Amplifier Output Filtering		
C196, C197, C198, C199	0.01 µF	0603	Ceramic, 0.01 µF, 50V, ±10%, X7R
C100, C121	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C104, C108, C111, C115	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C109, C110, C116, C117	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}
C103	1 µF	0603	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C105, C118, C119, C120	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R
C106, C107, C113, C114	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C101, C102, C122, C123	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout and routing give in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical section of the circuit is the the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. It is recommended that these be constructed to ensure they are given precedent as design trade-offs are made.
  - For questions and support go to the E2E forums (e2e.ti.com). If it is necessary to deviate from the recommended layout, please visit the E2E forum to request a layout review.

9.2.1.2.2 Step Two: HybridFlow Selection and System Level Tuning

- Use the *TAS5754/6M HybridFlow Processsor User Guide and HybridFlow Documentation* (SLAU577) to select the HybridFlow that meets the needs of the target application.
- Use the TAS5754_56MEVM evaluation module and the PurePath ControlConsole (PPC) software, to load the

appropriate HybridFlow. Tune the end equipment by following the instructions in the SLAU577 .

9.2.1.2.3 Step Three: Software Integration

- Use the *Register Dump* feature of the PPC software to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.2.1.3 Application Specific Performance Plots for Stereo 2.0 (BTL) Systems

Table 23. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 25. Output Power vs PVDD	C036
Figure 26. THD+N vs Frequency, V_{PVDD} = 12 V	C034
Figure 27. THD+N vs Frequency, V_{PVDD} = 15 V	C002
Figure 28. THD+N vs Frequency, V_{PVDD} = 18 V	C037
Figure 29. THD+N vs Frequency, V_{PVDD} = 24 V	C003
Figure 30. THD+N vs Power, V_{PVDD} = 12 V	C035
Figure 31. THD+N vs Power, V_{PVDD} = 15 V	C004
Figure 32. THD+N vs Power, V_{PVDD} = 18 V	C038
Figure 33. THD+N vs Power, V_{PVDD} = 24 V	C005
Figure 34. Idle Channel Noise vs PVDD	C006
Figure 35. Efficiency vs Output Power	C007
Figure 36. Idle Current Draw (Filterless) vs PVDD	C013
Figure 37. Idle Current Draw (Traditional LC Filter) vs PVDD	C015
Figure 40. DVDD PSRR vs. Frequency	C028
Figure 41. AVDD PSRR vs. Frequency	C029
Figure 42. C_{PVDD} PSRR vs. Frequency	C030
Figure 43. Powerdown Current Draw vs. PVDD	C032

9.2.2 Mono (PBTL) Systems

For the mono (PBTL) PCB layout, see Figure 89.

A mono system refers to a system in which the amplifier is used to drive a single loudspeaker. Parallel Bridge Tied Load (PBTL) indicates that the two full-bridge channels of the device are placed in parallel and drive the loudspeaker simultaneously using an identical audio signal. The primary benefit of operating the TAS5754M device in PBTL operation is to reduce the power dissipation and increase the current sourcing capabilities of the amplifier output. In this mode of operation, the current limit of the audio amplifier is approximately doubled while the on-resistance is approximately halved.

The loudspeaker can be a full-range transducer or one that only reproduces the low-frequency content of an audio signal, as in the case of a powered subwoofer. Often in this use case, two stereo signals are mixed together and sent through a low-pass filter in order to create a single audio signal which contains the low frequency information of the two channels. Conversely, advanced digital signal processing can create a low-frequency signal for a multichannel system, with audio processing which is specifically targeted on low-frequency effects.

Although any of the HybridFlows can be made to work with a mono speaker, it is strongly recommended that HybridFlows which have been created specifically for mono applications be used. These HybridFlows contain the mixing and filtering required to generate the mono signal. They also include processing which is targeted at improving the low-frequency performance of an audio system- a feature that, while targeted at subwoofers, can also be used to enhance the low-frequency performance of a full-range speaker.

Because low-frequency signals are not perceived as having a direction (at least to the extent of high-frequency signals) it is common to reproduce the low-frequency content of a stereo signal that is sent to two separate channels. This configuration pairs one device in Mono PBTL configuration and another device in Stereo BTL configuration in a single system called a 2.1 system. The Mono PBTL configuration is detailed in the 2.1 (Stereo BTL + External Mono Amplifier) Systems section.

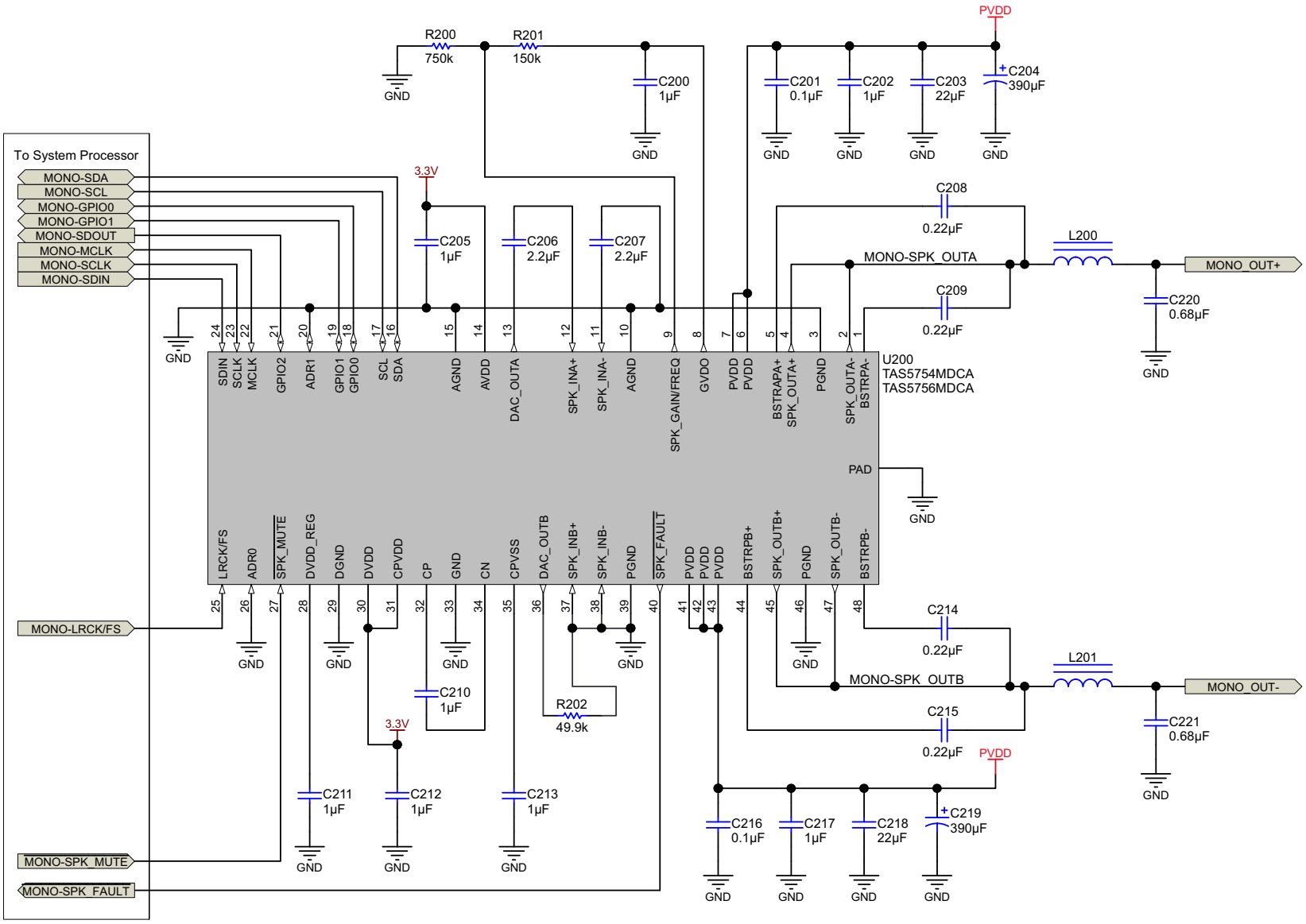


Figure 81. Mono (PBTL) System Application Schematic

9.2.2.1 Design Requirements

- Power Supplies:
  - 3.3-V Supply
  - 5-V to 24-V Supply
- Communication: Host Processor serving as I^2C Compliant Master
- External Memory (EEPROM, Flash, Etc.) used for Coefficients and RAM portions of HybridFlow < 5 kB

The requirements for the supporting components for the TAS5754M device in a Mono (PBTL) System is provided in Table 24.

Table 24. Supporting Component Requirements for Mono (PBTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U200	TAS5754M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier with HybridFlow processing
R200	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
R201	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
R202	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
L200, L201	See Amplifier Output Filtering		
C298, C299	0.01 µF	0603	Ceramic, 0.01 µF, 50 V, ±10%, X7R
C216	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C208, C209, C214, C215	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C220, C221	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}
C200	1 µF	0603	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C205, C211, C213, C212	1 µF	0402	Ceramic, 1 µF, 6.3 V, ±10%, X5R
C202, C217, C352, C367	1 µF	0805	Ceramic, 1 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C206, C207	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C203, C218	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C204, C219	390 µF	10 × 10	Aluminum, 390 µF, ±20%, 0.08-Ω Voltage rating must be > 1.45 × V_{PVDD}

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout and routing give in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical section of the circuit is the the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. It is recommended that these be constructed to ensure they are given precedent as design trade-offs are made.
  - For questions and support go to the E2E forums (e2e.ti.com). If it is necessary to deviate from the

recommended layout, please visit the E2E forum to request a layout review.

9.2.2.2.2 Step Two: HybridFlow Selection and System Level Tuning

- Use the *TAS5754/6M HybridFlow Processsor User Guide and HybridFlow Documentation* (SLAU577) to select the HybridFlow that meets the needs of the target application.
- Use the TAS5754_56MEVM evaluation module and the PurePath ControlConsole (PPC) software, to load the appropriate HybridFlow. Tune the end equipment by following the instructions in the SLAU577 .

9.2.2.2.3 Step Three: Software Integration

- Use the *Register Dump* feature of the PPC software to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.2.2.3 Application Specific Performance Plots for Mono (PBTL) Systems

Table 25. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 44. Output Power vs PVDD	C039
. THD+N vs Frequency, V_{PVDD} = 12 V	C017
. THD+N vs Frequency, V_{PVDD} = 15 V	C018
Figure 47. THD+N vs Frequency, V_{PVDD} = 18 V	C019
Figure 48. THD+N vs Frequency, V_{PVDD} = 24 V	C020
Figure 49. THD+N vs Power, V_{PVDD} = 12 V	C021
Figure 50. THD+N vs Power, V_{PVDD} = 15 V	C022
Figure 51. THD+N vs Power, V_{PVDD} = 18 V	C023
Figure 52. THD+N vs Power, V_{PVDD} = 24 V	C024
Figure 53. Idle Channel Noise vs PVDD	C025
Figure 54. Efficiency vs Output Power	C026
Figure 55. Idle Current Draw (filterless) vs PVDD	C031
Figure 56. Idle Current Draw (traditional LC filter) vs PVDD	C032
Figure 57. PVDD PSRR vs Frequency	C027
Figure 40. DVDD PSRR vs. Frequency	C028
Figure 41. AVDD PSRR vs. Frequency	C029
Figure 42. C_{PVDD} PSRR vs. Frequency	C030
Figure 43. Powerdown Current Draw vs. PVDD	C032

9.2.3 2.1 (Stereo BTL + External Mono Amplifier) Systems

Figure 91 shows the PCB Layout for the 2.1 System.

To increase the low-frequency output capabilities of an audio system, a single subwoofer can be added to the system. Because the spatial clues for audio are predominately higher frequency than that reproduced by the subwoofer, often a single subwoofer can be used to reproduce the low frequency content of several other channels in the system. This is frequently referred to as a *dot one* system. A stereo system with a subwoofer is referred to as a 2.1 (two-dot-one), a 3 channel system with subwoofer is referred to as a 3.1 (three-dot-one), a popular surround system with five speakers and one subwoofer is referred to as a 5.1, and so on.

9.2.3.1 Basic 2.1 System (TAS5754M Device + Simple Digital Input Amplifier)

In the most basic 2.1 system, a subwoofer is added to a stereo left and right pair of speakers as discussed above. The audio amplifiers include one TAS5754M device for the high frequency channels and one simple digital input device without integrated audio processing for the subwoofer channel. A member of the popular TAS5760xx family of devices is a popular choice for the subwoofer amplifier. In this system, the subwoofer content is generated by summing the two channels of audio and sending them through a high-pass filter to filter out the high frequency content. This is then sent to the SDIN pin of the subwoofer amplifier, which is operating in PBTL, via the SDOUT line of the TAS5754M device . In the basic 2.1 system, only HybridFlows which included subwoofer signal generation can be used, because the subwoofer amplifier depends on the TAS5754M device to create its stereo low-frequency input signal.

9.2.3.2 Advanced 2.1 System (Two TAS5754M devices)

In higher performance systems, the subwoofer output can be enhanced using digital audio processing as was done in the high-frequency channels. To accomplish this, two TAS5754M devices are used- one for the high frequency left and right speakers and one for the mono subwoofer speaker. In this system, the audio signal can be sent from the TAS5754M device through the SDOUT pin. Alternatively, the subwoofer amplifier can accept the same digital input as the stereo, which might come from a central systems processor. In advanced 2.1 systems, any HybridFlow can be used for the subwoofer, provided the sample rates for the two are the same. While any of the HybridFlows can be used, it is highly recommended that only mono HybridFlows are used for the subwoofer. Doing so streamlines development time and effort by minimizing confusion and complexity.

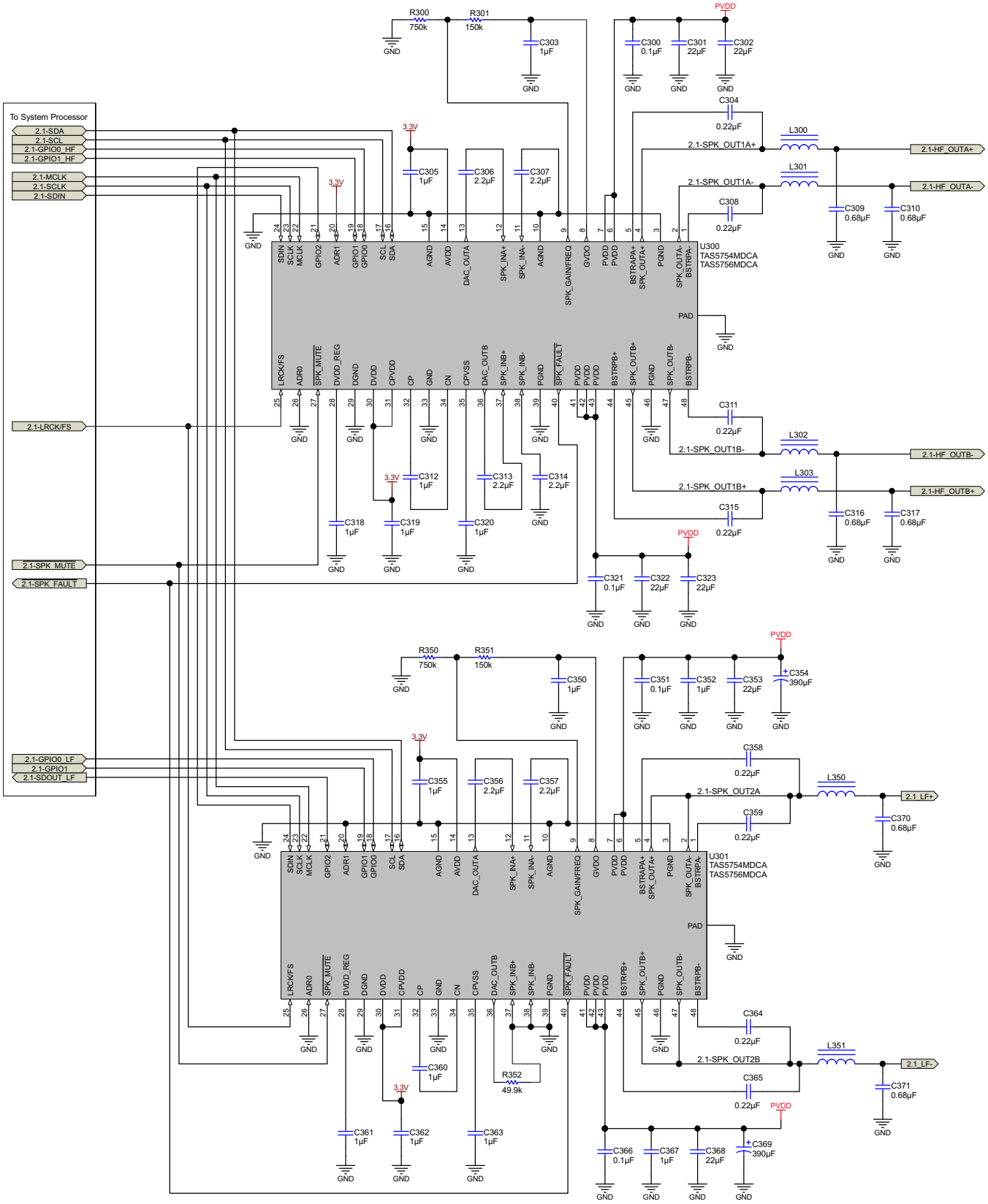


Figure 82. 2.1 (Stereo BTL + External Mono Amplifier) Application Schematic

9.2.3.3 Design Requirements

- Power Supplies:
  - 3.3-V Supply
  - 5-V to 24-V Supply
- Communication: Host Processor serving as I^2C Compliant Master
- External Memory (EEPROM, Flash, Etc.) used for Coefficients and RAM portions of HybridFlow < 5 kB

The requirements for the supporting components for the TAS5754M device in a 2.1 (Stereo BTL + External Mono Amplifier) System is provided in Table 26.

Table 26. Supporting Component Requirements for 2.1 (Stereo BTL + External Mono Amplifier) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U300	TAS5754M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier with HybridFlow processing
R300, R350	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
R301, R351	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
R352	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
L300, L301, L302, L303	See Amplifier Output Filtering		
L350, L351	See Amplifier Output Filtering		
C394, C395, C396, C397, C398, C399	0.01 µF	0603	Ceramic, 0.01µF, 50V, +/-10%, X7R
C300, C321, C351, C366	0.1 µF	0402	Ceramic, 0.1µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C304, C308, C311, C315, C358, C359, C364, C365	0.22 µF	0603	Ceramic, 0.22µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C309, C310, C316, C317, C370, C371	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}
C303, C350, C312, C360	1 µF	0603	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C305, C318, C319, C320, C355, C361, C363, C312, C362	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R
C352, C367	1 µF	0805	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C306, C307, C313, C314, C356, C357,	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C301, C302, C322, C323, C353, C368	22 µF	0805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C354, C369	390 µF	10 × 10	Aluminum, 390 µF, ±20%, 0.08 Ω Voltage rating must be > 1.45 × V_{PVDD}

9.2.3.4 Detailed Design Procedure

9.2.3.4.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout and routing give in the example layout above, integrate the device and its supporting components into the system PCB file.

– The most critical section of the circuit is the the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. It is recommended that these be constructed to ensure they are given precedent as design trade-offs are made.
– For questions and support go to the E2E forums (e2e.ti.com). If it is necessary to deviate from the recommended layout, please visit the E2E forum to request a layout review.

9.2.3.4.2 Step Two: HybridFlow Selection and System Level Tuning

- Use the *TAS5754/6M HybridFlow Processsor User Guide and HybridFlow Documentation* (SLAU577) to select the HybridFlow that meets the needs of the target application.
- Use the TAS5754_56MEVM evaluation module and the PurePath ControlConsole (PPC) software, to load the appropriate HybridFlow. Tune the end equipment by following the instructions in the SLAU577 .

9.2.3.4.3 Step Three: Software Integration

- Use the *Register Dump* feature of the PPC software to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.2.3.5 Application Specific Performance Plots for 2.1 (Stereo BTL + External Mono Amplifier) Systems

Table 27. Relevant Performance Plots

DEVICE	PLOT TITLE	PLOT NUMBER
U300	Figure 25. Output Power vs PVDD	C036
	Figure 26. THD+N vs Frequency, V_{PVDD} = 12 V	C034
	Figure 27. THD+N vs Frequency, V_{PVDD} = 15 V	C002
	Figure 28. THD+N vs Frequency, V_{PVDD} = 18 V	C037
	Figure 29. THD+N vs Frequency, V_{PVDD} = 24 V	C003
	Figure 30. THD+N vs Power, V_{PVDD} = 12 V	C035
	Figure 31. THD+N vs Power, V_{PVDD} = 15 V	C004
	Figure 32. THD+N vs Power, V_{PVDD} = 18 V	C038
	Figure 33. THD+N vs Power, V_{PVDD} = 24 V	C005
	Figure 34. Idle Channel Noise vs PVDD	C006
	Figure 35. Efficiency vs Output Power	C007
	Figure 36. Idle Current Draw (Filterless) vs PVDD	C013
	Figure 37. Idle Current Draw (Traditional LC Filter) vs PVDD	C015
U301	Figure 44. Output Power vs PVDD	C039
	. THD+N vs Frequency, V_{PVDD} = 12 V	C017
	. THD+N vs Frequency, V_{PVDD} = 15 V	C018
	Figure 47. THD+N vs Frequency, V_{PVDD} = 18 V	C019
	Figure 48. THD+N vs Frequency, V_{PVDD} = 24 V	C020
	Figure 49. THD+N vs Power, V_{PVDD} = 12 V	C021
	Figure 50. THD+N vs Power, V_{PVDD} = 15 V	C022
	Figure 51. THD+N vs Power, V_{PVDD} = 18 V	C023
	Figure 52. THD+N vs Power, V_{PVDD} = 24 V	C024
	Figure 53. Idle Channel Noise vs PVDD	C025
	Figure 54. Efficiency vs Output Power	C026
	Figure 55. Idle Current Draw (filterless) vs PVDD	C031
	Figure 56. Idle Current Draw (traditional LC filter) vs PVDD	C032
	Figure 57. PVDD PSRR vs Frequency	C027

Table 27. Relevant Performance Plots (continued)

DEVICE	PLOT TITLE	PLOT NUMBER
U300 and U301	Figure 40. DVDD PSRR vs. Frequency	C028
	Figure 41. AVDD PSRR vs. Frequency	C029
	Figure 42. C_{PVDD} PSRR vs. Frequency	C030
	Figure 43. Powerdown Current Draw vs. PVDD	C032

9.2.4 2.2 (Dual Stereo BTL) Systems

For the 2.2 (Dual Stereo BTL) PCB layout, see Figure 93.

A 2.2 system consists of a stereo pair of loudspeakers with a pair of low frequency loudspeakers. In some cases, this is implemented as two stereo full-range speakers and two subwoofers. In others, it is implemented as two high frequency speakers and two mid-range speakers.

As in the case of the 2.1 system, the 2.2 system can be created by using the audio processing inside of the TAS5754M device and creating a subwoofer signal which is sent to a simple digital input amplifier like one of the TAS5760xx devices (or similar). This requires that a HybridFlow that contains a subwoofer generation processing block be used in the TAS5754M device. This signal is created by summing the left and right channel, filtering with a high-pass filter and sending it to the subwoofer amplifier. For this type of system, the TAS5754M device used for the high-frequency drivers must have a subwoofer generation processing block in order to provide the appropriate signal to the subwoofer amplifiers.

Alternatively, the low-frequency drivers can be implemented by using two TAS5754M devices; each receiving their input from a central systems processor. This type of implementation allows for any stereo HybridFlow to be used for both the low-frequency and high-frequency drivers, increasing the processing options available for the system. This expands the processing capabilities of the system, introducing digital signal processing to the low-frequency drivers as well as the high-frequency drivers. This type of 2.2 system is described in Figure 83.

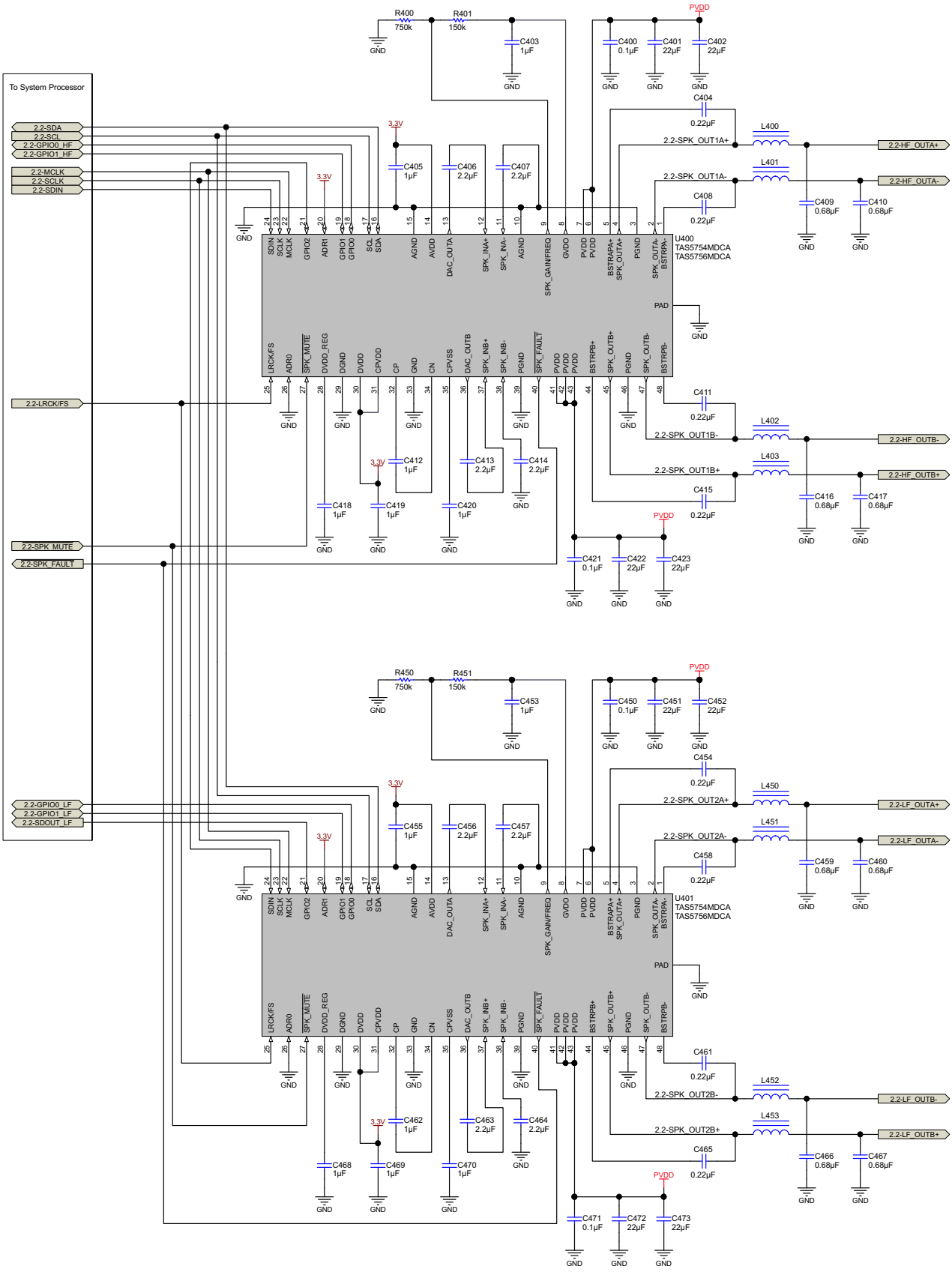


Figure 83. 2.2 (Dual Stereo BTL) Application Schematic

9.2.4.1 Design Requirements

- Power Supplies:
  - 3.3-V Supply
  - 5-V to 24-V Supply
- Communication: Host Processor serving as I^2C Compliant Master
- External Memory (EEPROM, Flash, Etc.) used for Coefficients and RAM portions of HybridFlow < 5 kB

The requirements for the supporting components for the TAS5754M device in a 2.1 (Stereo BTL + External Mono Amplifier) System is provided in Figure 89.

Table 28. Supporting Component Requirements for 2.2 (Dual Stereo BTL) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U400, U401	TAS5754M device	48-pin TSSOP	Digital Input, Closed-Loop Class-D Amplifier with HybridFlow Processing
R400, R450	See Figure 84	0402	1%, 0.063 W
R401, R451	See Figure 84	0402	1%, 0.063 W
L400, L401, L402, L403, L450, L451, L452, L453	See Amplifier Output Filtering		
C492, C493, C494, C495, C496, C497, C498, C499	0.01 µF	0603	Ceramic, 0.01 µF, 50 V, ±10%, X7R
C400, C421, C450, C471	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R, Voltage rating must be > 1.45 × V_{PVDD}
C404, C408, C411, C415, C454, C458, C461, C465	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R, Voltage rating must be > 1.45 × V_{PVDD}
C409, C410, C416, C417, C459, C460, C466, C467	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R, Voltage rating must be > 1.8 × V_{PVDD}
C403, C453, C462	1 µF	0603	Ceramic, 1 µF, ±10%, X7R, Voltage rating must be > 1.45 × V_{PVDD}
C405, C418, C419, C420, C455, C468, C469, C470, C412, C462	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R
C406, C407, C413, C414, C456, C457, C463, C464	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R, Voltage rating must be > 1.45 × V_{PVDD}
C401, C402, C422, C423, C451, C452, C472, C473	22 µF	0805	Ceramic, 22 µF, ±20%, X5R, Voltage rating must be > 1.45 × V_{PVDD}

9.2.4.2 Detailed Design Procedure

9.2.4.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout and routing give in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical section of the circuit is the the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. It is recommended that these be constructed to ensure they are given precedent as design trade-offs are made.
  - For questions and support go to the E2E forums (e2e.ti.com). If it is necessary to deviate from the recommended layout, please visit the E2E forum to request a layout review.

9.2.4.2.2 Step Two: HybridFlow Selection and System Level Tuning

- Use the *TAS5754/6M HybridFlow Processsor User Guide and HybridFlow Documentation* (SLAU577) to select the HybridFlow that meets the needs of the target application.

- Use the TAS5754_56MEVM evaluation module and the PurePath ControlConsole (PPC) software, to load the appropriate HybridFlow. Tune the end equipment by following the instructions in the SLAU577 .

9.2.4.2.3 Step Three: Software Integration

- Use the *Register Dump* feature of the PPC software to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.2.4.3 Application Specific Performance Plots for 2.2 (Dual Stereo BTL) Systems

Table 29. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 25. Output Power vs PVDD	C036
Figure 26. THD+N vs Frequency, V_{PVDD} = 12 V	C034
Figure 27. THD+N vs Frequency, V_{PVDD} = 15 V	C002
Figure 28. THD+N vs Frequency, V_{PVDD} = 18 V	C037
Figure 29. THD+N vs Frequency, V_{PVDD} = 24 V	C003
Figure 30. THD+N vs Power, V_{PVDD} = 12 V	C035
Figure 31. THD+N vs Power, V_{PVDD} = 15 V	C004
Figure 32. THD+N vs Power, V_{PVDD} = 18 V	C038
Figure 33. THD+N vs Power, V_{PVDD} = 24 V	C005
Figure 34. Idle Channel Noise vs PVDD	C006
Figure 35. Efficiency vs Output Power	C007
Figure 36. Idle Current Draw (Filterless) vs PVDD	C013
Figure 37. Idle Current Draw (Traditional LC Filter) vs PVDD	C015
Figure 40. DVDD PSRR vs. Frequency	C028
Figure 41. AVDD PSRR vs. Frequency	C029
Figure 42. C_{PVDD} PSRR vs. Frequency	C030
Figure 43. Powerdown Current Draw vs. PVDD	C032

9.2.5 1.1 (Dual BTL, Bi-Amped) Systems

The 1.1 use case is a special application of the 2.0 stereo BTL system. In this system, two channels of an amplifier are used to reproduce a single channel of an audio signal that has been separated based on frequency. This configuration removes the need for passive cross-over elements inside of a loudspeaker, because the signal is separated into a low-frequency and a high-frequency component before it is amplified. Systems which operate in this configuration, in which separate amplifier channels drive the low and high-frequency loudspeakers directly, are often called “bi-amped” systems.

Popular applications for this configuration include:

- Powered near-field monitors
- Blue-tooth Speakers
- Co-axial Loudspeakers
- Surround/Fill Speakers for multi-channel audio

From a hardware perspective, the TAS5754M device is configured in the same way as the Stereo BTL system. However, special HybridFlows which support 1.1 operation must be used, because HybridFlows that are designed for stereo applications frequently apply the same equalizer curves to the left and the right hand channel. Additionally, many 1.1 HybridFlows include a delay element which can improve time alignment between two loudspeakers that are mounted on the same baffle some distance apart.

For the 1.1 (Dual BTL, Bi-Amped) PCB layout, see Figure 95.

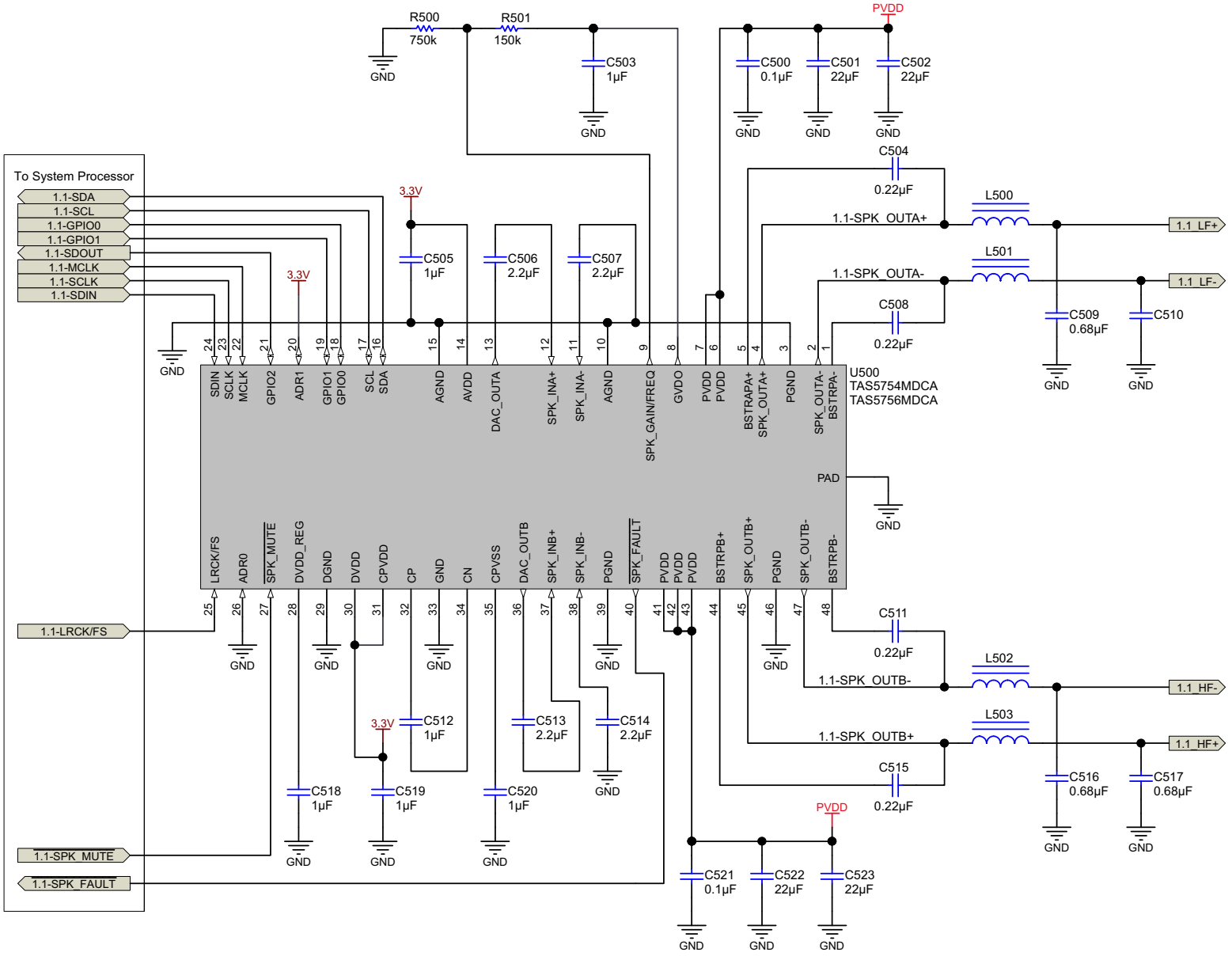


Figure 84. 1.1 (Dual BTL, Bi-Amped) Application Schematic

9.2.5.1 Design Requirements

- Power Supplies:
  - DVDD Supply, in compliance with the voltage ranges shown in the *Recommended Operating Conditions* table.
  - PVDD Supply, in compliance with the voltage ranges shown in the *Recommended Operating Conditions* table.
- Communication: Host Processor serving as I^2C Compliant Master
- External Memory (EEPROM, Flash, Etc.) used for Coefficients and RAM portions of HybridFlow < 5 kB

The requirements for the supporting components for the TAS5754M device in a Dual BTL, Bi-Amped System is provided in Figure 95.

Table 30. Supporting Component Requirements for 1.1 (Dual BTL, Bi-Amped) Systems

REFERENCE DESIGNATOR	VALUE	SIZE	DETAILED DESCRIPTION
U500	TAS5754M	48 Pin TSSOP	Digital-input, closed-loop class-D amplifier with HybridFlow processing
R500	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
R501	See Adjustable Amplifier Gain and Switching Frequency Selection	0402	1%, 0.063 W
L500, L501, L502, L503	See Amplifier Output Filtering		
C596, C597, C598, C599	0.01 µF	0603	Ceramic, 0.01 µF, 50 V, ±10%, X7R
C500, C521	0.1 µF	0402	Ceramic, 0.1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C504, C508, C511, C515	0.22 µF	0603	Ceramic, 0.22 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C509, C510, C516, C517	0.68 µF	0805	Ceramic, 0.68 µF, ±10%, X7R Voltage rating must be > 1.8 × V_{PVDD}
C503	1 µF	0603	Ceramic, 1 µF, ±10%, X7R Voltage rating must be > 1.45 × V_{PVDD}
C505, C518, C519, C520, C512	1 µF	0402	Ceramic, 1 µF, 6.3V, ±10%, X5R
C506, C507, C513, C514	2.2 µF	0402	Ceramic, 2.2 µF, ±10%, X5R Voltage rating must be > 1.45 × V_{PVDD}
C501, C502, C522, C523	22 µF	805	Ceramic, 22 µF, ±20%, X5R Voltage rating must be > 1.45 × V_{PVDD}

9.2.5.2 Detailed Design Procedure

9.2.5.2.1 Step One: Hardware Integration

- Using the *Typical Application Schematic* as a guide, integrate the hardware into the system schematic.
- Following the recommended component placement, board layout and routing give in the example layout above, integrate the device and its supporting components into the system PCB file.
  - The most critical section of the circuit is the the power supply inputs, the amplifier output signals, and the high-frequency signals which go to the serial audio port. It is recommended that these be constructed to ensure they are given precedent as design trade-offs are made.
  - For questions and support go to the E2E forums (e2e.ti.com). If it is necessary to deviate from the recommended layout, please visit the E2E forum to request a layout review.

9.2.5.2.2 Step Two: HybridFlow Selection and System Level Tuning

- Use the *TAS5754/6M HybridFlow Processsor User Guide and HybridFlow Documentation* (SLAU577) to

select the HybridFlow that meets the needs of the target application.

- Use the TAS5754_56MEVM evaluation module and the PurePath ControlConsole (PPC) software, to load the appropriate HybridFlow. Tune the end equipment by following the instructions in the SLAU577 .

9.2.5.2.3 Step Three: Software Integration

- Use the *Register Dump* feature of the PPC software to generate a baseline configuration file.
- Generate additional configuration files based upon operating modes of the end-equipment and integrate static configuration information into initialization files.
- Integrate dynamic controls (such as volume controls, mute commands, and mode-based EQ curves) into the main system program.

9.2.5.3 Application Specific Performance Plots for 1.1 (Dual BTL, Bi-Amped) Systems

Table 31. Relevant Performance Plots

PLOT TITLE	PLOT NUMBER
Figure 25. Output Power vs PVDD	C036
Figure 26. THD+N vs Frequency, V_{PVDD} = 12 V	C034
Figure 27. THD+N vs Frequency, V_{PVDD} = 15 V	C002
Figure 28. THD+N vs Frequency, V_{PVDD} = 18 V	C037
Figure 29. THD+N vs Frequency, V_{PVDD} = 24 V	C003
Figure 30. THD+N vs Power, V_{PVDD} = 12 V	C035
Figure 31. THD+N vs Power, V_{PVDD} = 15 V	C004
Figure 32. THD+N vs Power, V_{PVDD} = 18 V	C038
Figure 33. THD+N vs Power, V_{PVDD} = 24 V	C005
Figure 34. Idle Channel Noise vs PVDD	C006
Figure 35. Efficiency vs Output Power	C007
Figure 36. Idle Current Draw (Filterless) vs PVDD	C013
Figure 37. Idle Current Draw (Traditional LC Filter) vs PVDD	C015
Figure 40. DVDD PSRR vs. Frequency	C028
Figure 41. AVDD PSRR vs. Frequency	C029
Figure 42. C_{PVDD} PSRR vs. Frequency	C030
Figure 43. Powerdown Current Draw vs. PVDD	C032

10 Power Supply Recommendations

10.1 Power Supplies

The TAS5754M device requires two power supplies for proper operation. A *high-voltage* supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one *low-voltage* power supply called DVDD is required to power the various low-power portions of the device. The allowable voltage range for both the PVDD and the DVDD supply are listed in the *Recommended Operating Conditions* table.

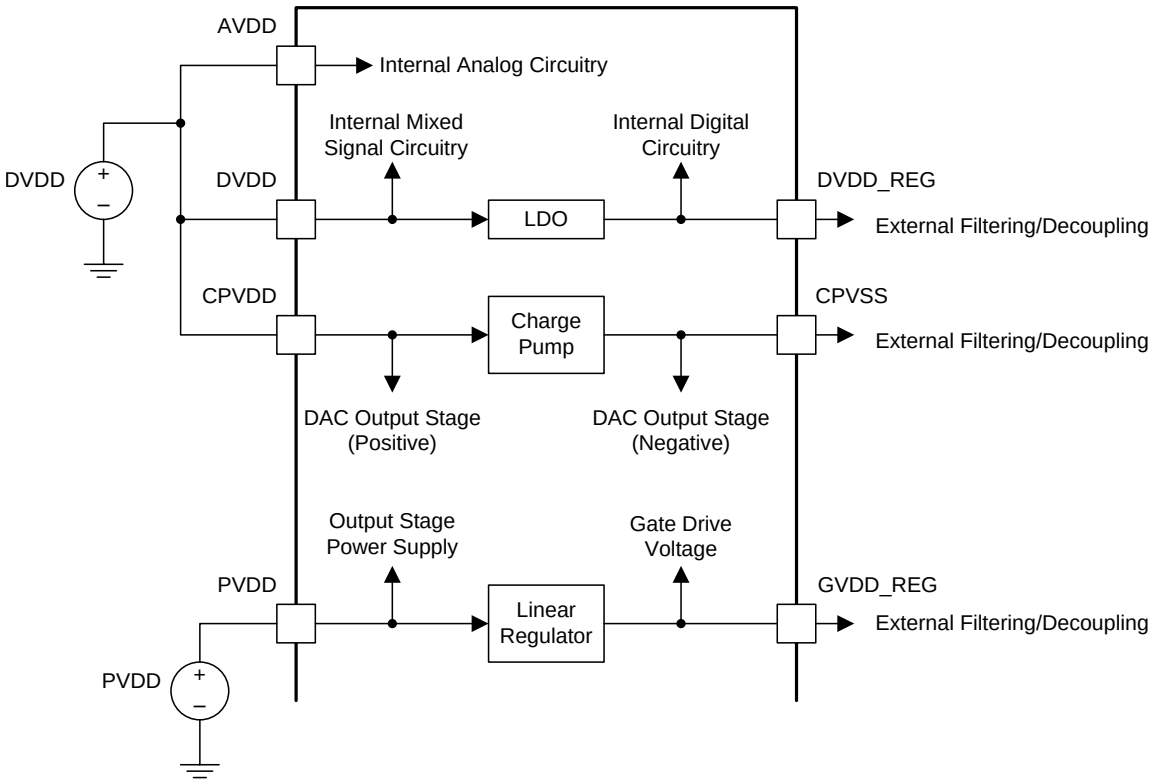


Figure 85. Power Supply Functional Block Diagram

10.1.1 DVDD Supply

The DVDD supply required from the system is used to power several portions of the device. As shown in the *Figure 85*, it provides power to the DVDD pin, the CPVDD pin, and the AVDD pin. Proper connection, routing, and decoupling techniques are highlighted in the TAS5754M device *EVM User's Guide* SLAU583 (as well as the *Applications and Implementation* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TAS5754M device *EVM User's Guide*, which followed the same techniques as those shown in the *Applications and Implementation* section, may result in reduced performance, errant functionality, or even damage to the TAS5754M device.

Some portions of the device also require a separate power supply which is a lower voltage than the DVDD supply. To simplify the power supply requirements for the system, the TAS5754M device includes an integrated low-dropout (LDO) linear regulator to create this supply. This linear regulator is internally connected to the DVDD supply and its output is presented on the DVDD_REG pin, providing a connection point for an external bypass capacitor. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

Power Supplies (continued)

The outputs of the high-performance DACs used in the TAS5754M device are ground centered, requiring both a positive low-voltage supply and a negative low-voltage supply. The positive power supply for the DAC output stage is taken from the AVDD pin, which is connected to the DVDD supply provided by the system. A charge pump is integrated in the TAS5754M device to generate the negative low-voltage supply. The power supply input for the charge pump is the CPVDD pin. The CPVSS pin is provided to allow the connection of a filter capacitor on the negative low-voltage supply. As is the case with the other supplies, the component selection, placement, and routing of the external components for these low voltage supplies are shown in the evmName and should be followed as closely as possible to ensure proper operation of the device.

10.1.2 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the evmName and must be followed as closely as possible for proper operation and performance. Due the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TAS5754M device *EVM User's Guide*. Lack of proper decoupling, like that shown in the *EVM User's Guide*, results in voltage spikes which can damage the device.

A separate power supply is required to drive the gates of the MOSFETs used in the output stage of the speaker amplifier. This power supply is derived from the PVDD supply via an integrated linear regulator. A GVDD_REG pin is provided for the attachment of decoupling capacitor for the gate drive voltage regulator. It is important to note that the linear regulator integrated in the device has only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on this pin could cause the voltage to sag, negatively affecting the performance and operation of the device.

11 Layout

11.1 Layout Guidelines

11.1.1 General Guidelines for Audio Amplifiers

Audio amplifiers which incorporate switching output stages must have special attention paid to their layout and the layout of the supporting components used around them. The system level performance metrics, including thermal performance, electromagnetic compliance (EMC), device reliability, and audio performance are all affected by the device and supporting component layout.

Ideally, the guidance provided in the applications section with regard to device and component selection can be followed by precise adherence to the layout guidance shown in . These examples represent exemplary *baseline* balance of the engineering trade-offs involved with laying out the device. These designs can be modified slightly as needed to meet the needs of a given application. In some applications, for instance, solution size can be compromised in order to improve thermal performance through the use of additional contiguous copper near the device. Conversely, EMI performance can be prioritized over thermal performance by routing on internal traces and incorporating a via picket-fence and additional filtering components. In all cases, it is recommended to start from the guidance shown in the *Layout Examples* section and the TAS5754M-56MEVM, and work with TI field application engineers or through the E2E community in order to modify it based upon the application specific goals.

11.1.2 Importance of PVDD Bypass Capacitor Placement on PVDD Network

Placing the bypassing and decoupling capacitors close to supply has been long understood in the industry. This applies to DVDD, AVDD, CPVDD, and PVDD. However, the capacitors on the PVDD net for the TAS5754M device deserve special attention.

It is imperative that the small bypass capacitors on the PVDD lines of the DUT be placed as close the PVDD pins as possible. Not only does placing these devices far away from the pins increase the electromagnetic interference in the system, but doing so can also negatively affect the reliability of the device. Placement of these components too far from the TAS5754M device may cause ringing on the output pins that can cause the voltage on the output pin to exceed the maximum allowable ratings shown in the *Absolute Maximum Ratings* table, damaging the device. For that reason, the capacitors on the PVDD net must be no further away from their associated PVDD pins than what is shown in the example layouts in the *Layout Examples* section

11.1.3 Optimizing Thermal Performance

Follow the layout examples shown in the *Layout Examples* section of this document to achieve the best balance of solution size, thermal, audio, and electromagnetic performance. In some cases, deviation from this guidance may be required due to design constraints which cannot be avoided. In these instances, the system designer should ensure that the heat can get out of the device and into the ambient air surrounding the device. Fortunately, the heat created in the device would prefer to travel away from the device and into the lower temperature structures around the device.

11.1.3.1 Device, Copper, and Component Layout

Primarily, the goal of the PCB design is to minimize the thermal impedance in the path to those cooler structures. These tips should be followed to achieve that goal:

- Avoid placing other heat producing components or structures near the amplifier (including above or below in the end equipment).
- If possible, use a higher layer count PCB to provide more heat sinking capability for the TAS5754M device and to prevent traces and copper signal and power planes from breaking up the contiguous copper on the top and bottom layer.
- Place the TAS5754M device away from the edge of the PCB when possible to ensure that heat can travel away from the device on all four sides.
- Avoid cutting off the flow of heat from the TAS5754M device to the surrounding areas with traces or via strings. Instead, route traces perpendicular to the device and line up vias in columns which are perpendicular to the device.
- Unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads, orient it so that the narrow end of the passive component is facing the TAS5754M

Layout Guidelines (continued)

device .

- Because the ground pins are the best conductors of heat in the package, maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible.

11.1.3.2 Stencil Pattern

The recommended drawings for the TAS5754M device PCB foot print and associated stencil pattern are shown at the end of this document in the package addendum. Additionally, baseline recommendations for the via arrangement under and around the device are given as a starting point for the PCB design. This guidance is provided to suit the majority of manufacturing capabilities in the industry and prioritizes manufacturability over all other performance criteria. In elevated ambient temperatures or under high-power dissipation use-cases, this guidance may be too conservative and advanced PCB design techniques may be used to improve thermal performance of the system. It is important to note that the customer must verify that deviation from the guidance shown in the package addendum, including the deviation explained in this section, meets the customer's quality, reliability, and manufacturability goals.

11.1.3.2.1 PCB footprint and Via Arrangement

The PCB footprint (also known as a *symbol* or *land pattern*) communicates to the PCB fabrication vendor the shape and position of the copper patterns to which the TAS5754M device will be soldered to. This footprint can be followed directly from the guidance in the package addendum at the end of this data sheet. It is important to make sure that the thermal pad, which connects electrically and thermally to the PowerPAD of the TAS5754M device , be made no smaller than what is specified in the package addendum. This ensures that the TAS5754M device has the largest interface possible to move heat from the device to the board.

The via pattern shown in the package addendum provides an improved interface to carry the heat from the device through to the layers of the PCB, because small diameter plated vias (with minimally-sized annular rings) present a low thermal-impedance path from the device into the PCB. Once into the PCB, the heat travels away from the device and into the surrounding structures and air. By increasing the number of vias, as shown in the *Layout Examples* section, this interface can benefit from improved thermal performance.

NOTE

Vias can obstruct heat flow if they are not constructed properly.

- Remove thermal reliefs on thermal vias, because they impede the flow of heat through the via.
- Vias filled with thermally conductive material are best, but a simple plated via can be used to avoid the additional cost of filled vias.
- The drill diameter should be no more than 8mils in diameter. Also, the distance between the via barrel and the surrounding planes should be minimized to help heat flow from the via into the surrounding copper material. In all cases, minimum spacing should be determined by the voltages present on the planes surrounding the via and minimized wherever possible.
- Vias should be arranged in columns, which extend in a line radially from the heat source to the surrounding area. This arrangement is shown in the *Layout Examples* section.
-
- Ensure that vias do not cut-off power current flow from the power supply through the planes on internal layers. If needed, remove some vias which are farthest from the TAS5754M device to open up the current path to and from the device.

11.1.3.2.1.1 Solder Stencil

During the PCB assembly process, a piece of metal called a *stencil* on top of the PCB and deposits solder paste on the PCB wherever there is an opening (called an aperture) in the stencil. The stencil determines the quantity and the location of solder paste that is applied to the PCB in the electronic manufacturing process. In most cases, the aperture for each of the component pads is almost the same size as the pad itself.

Layout Guidelines (continued)

However, the thermal pad on the PCB is quite large and depositing a large, single deposition of solder paste would lead to manufacturing issues. Instead, the solder is applied to the board in multiple apertures, to allow the solder paste to outgas during the assembly process and reduce the risk of solder bridging under the device. This structure is called an aperture array, and is shown in the *Layout Examples* section. It is important that the total area of the aperture array (the area of all of the small apertures combined) covers between 70% and 80% of the area of the thermal pad itself.

11.2 Layout Examples

11.2.1 2.0 (Stereo BTL) System

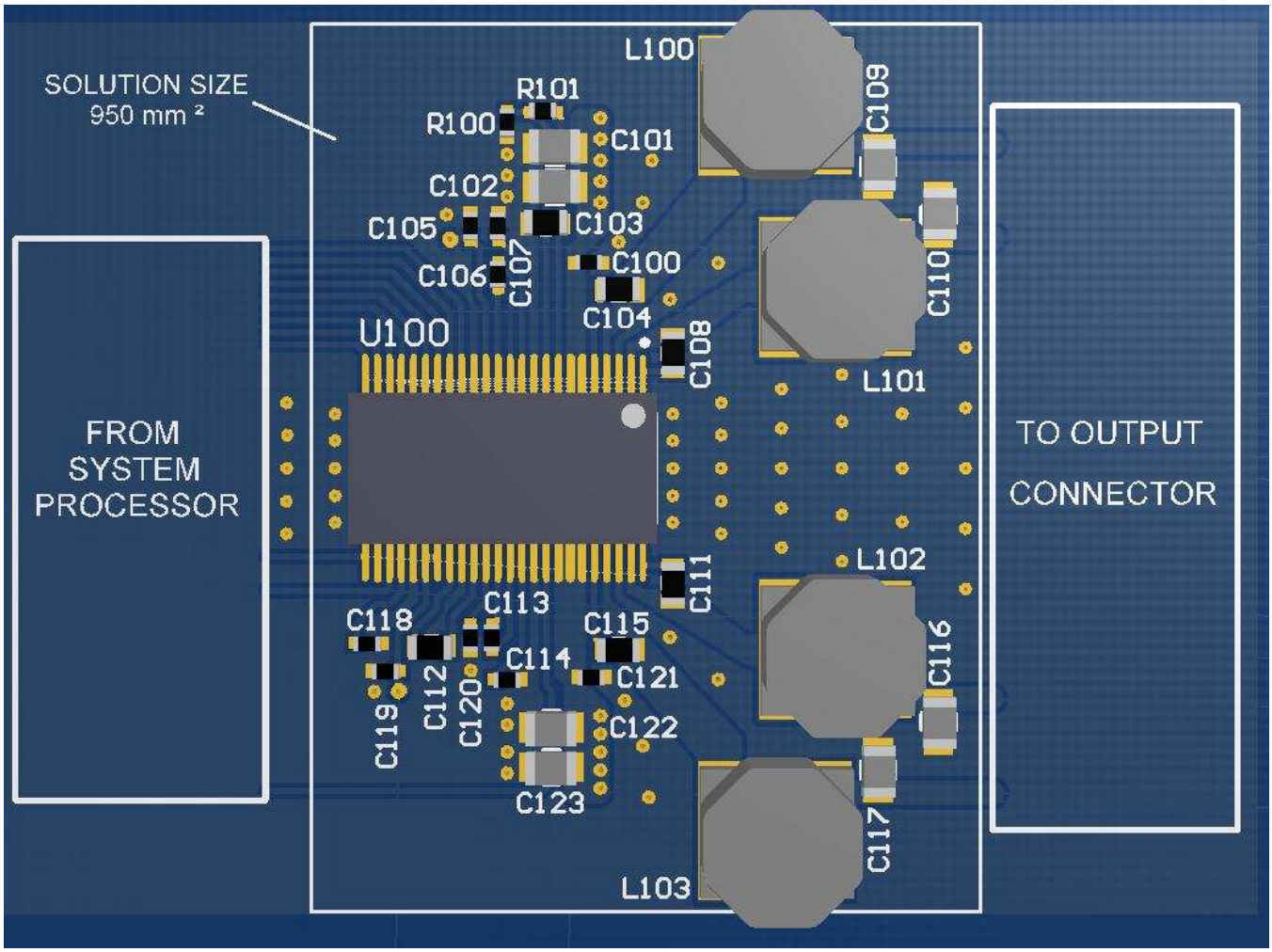


Figure 86. 2.0 (Stereo BTL) 3-D View

Layout Examples (continued)

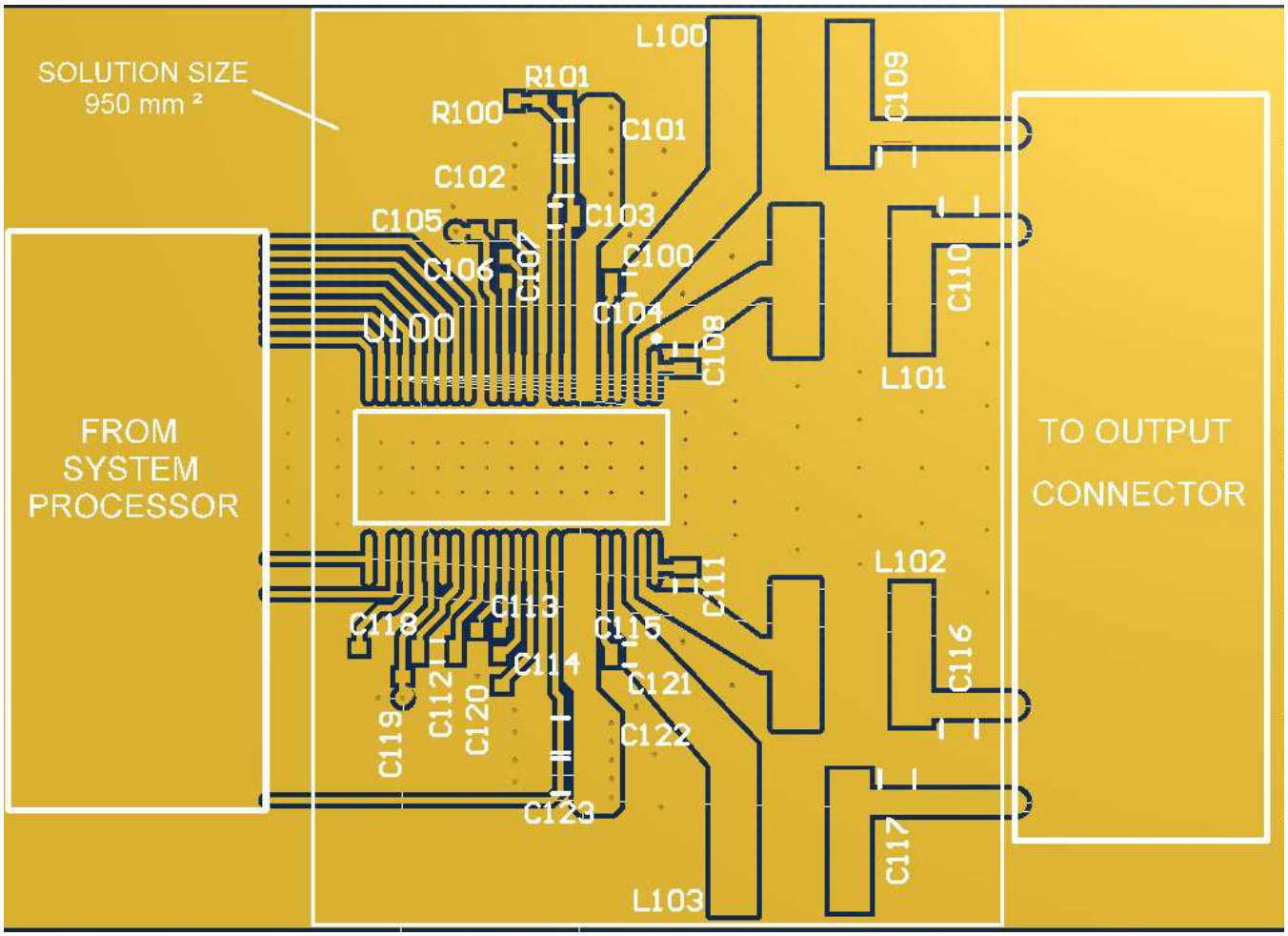


Figure 87. 2.0 (Stereo BTL) Top Copper View

Layout Examples (continued)

11.2.2 Mono (PBTL) System

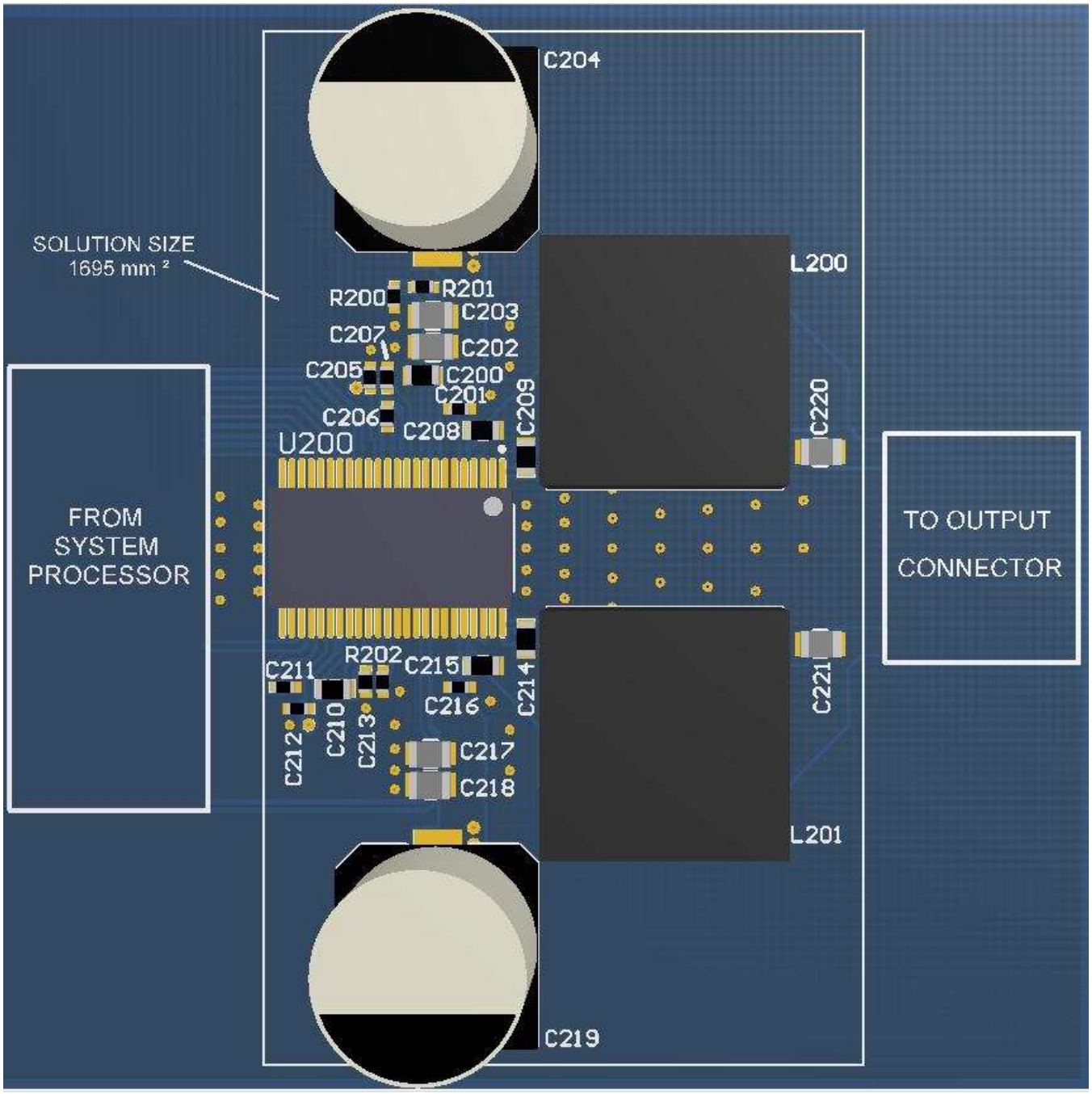


Figure 88. Mono (PBTL) 3-D View

Layout Examples (continued)

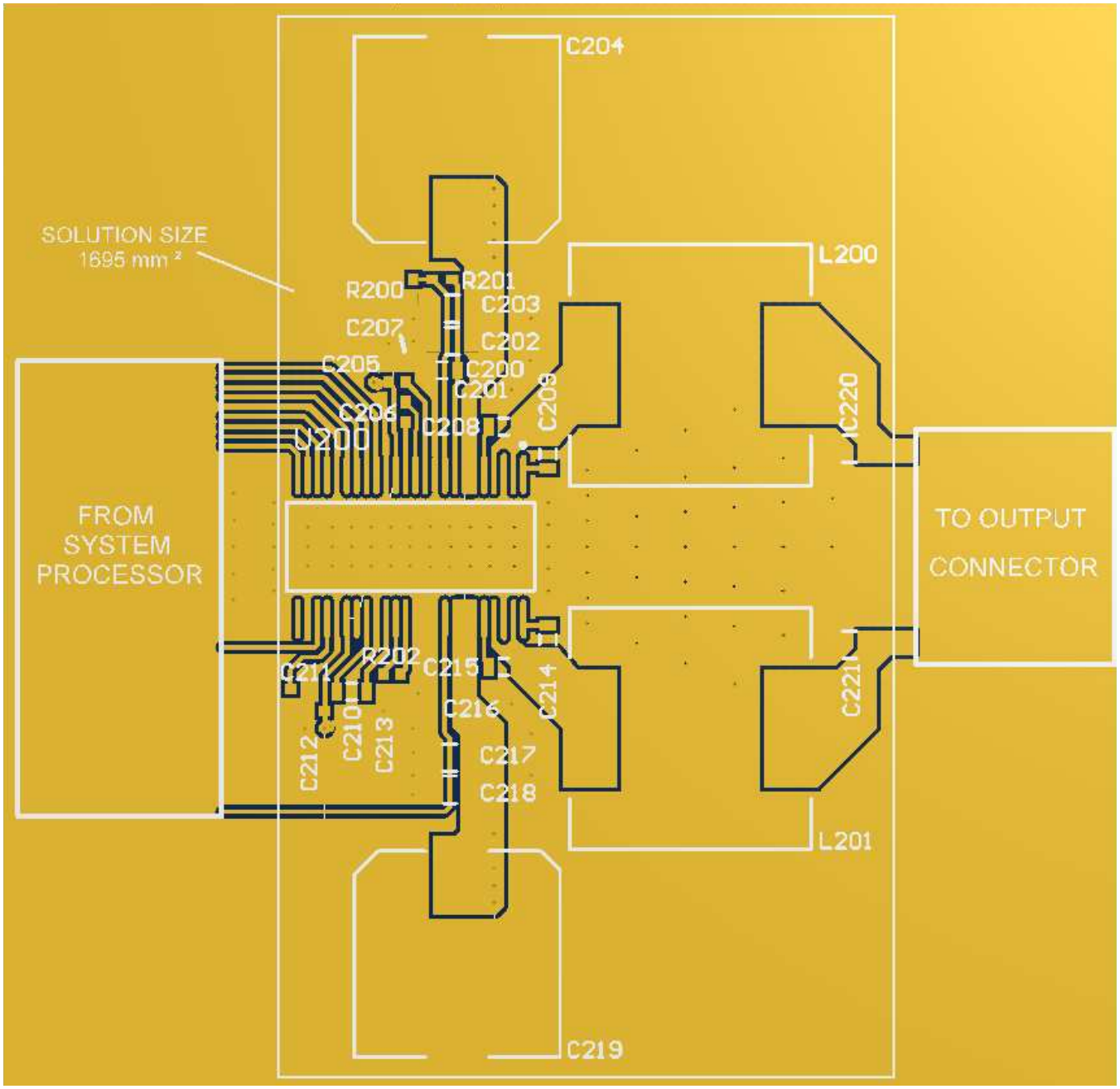


Figure 89. Mono (PBTL) Top Copper View

Layout Examples (continued)

11.2.3 2.1 (Stereo BTL + Mono PBTL) Systems

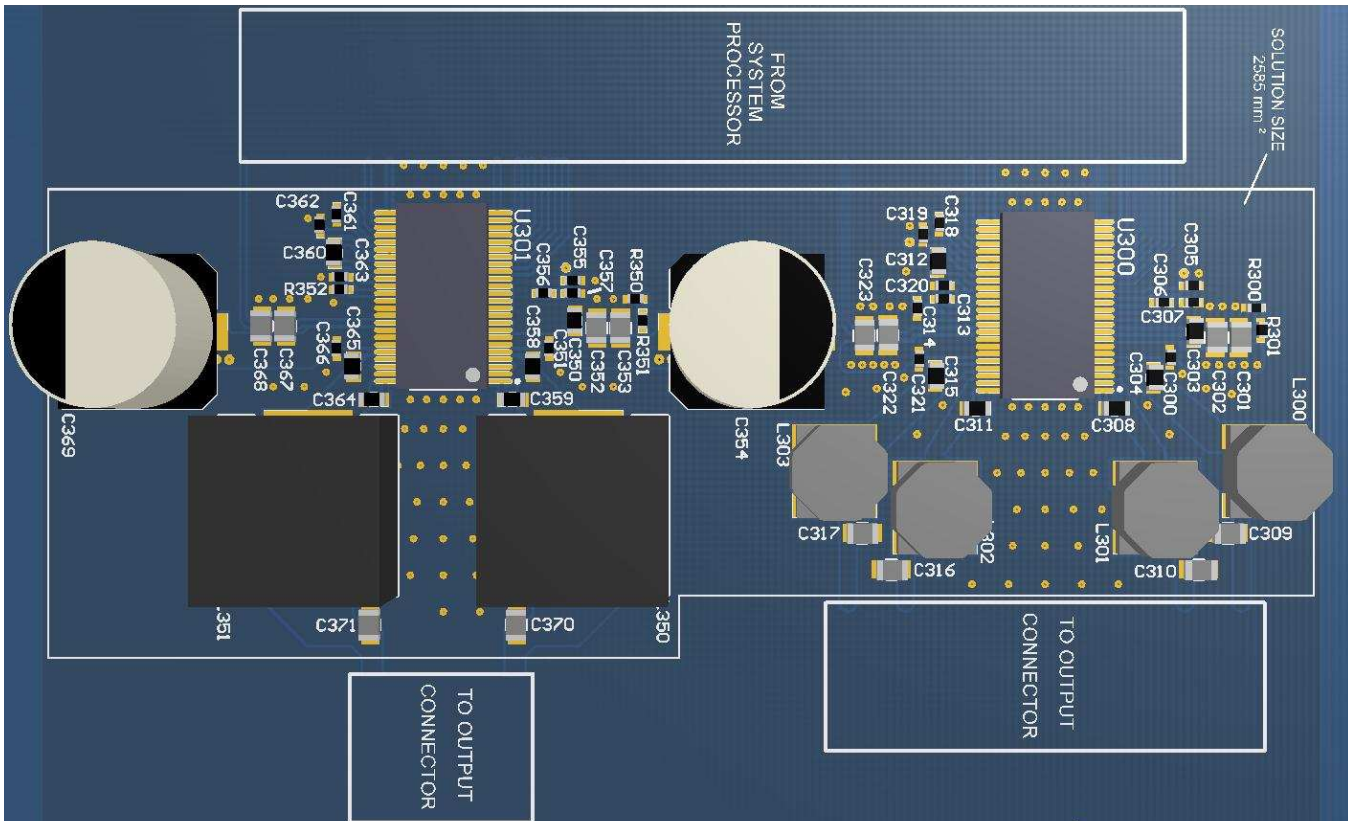


Figure 90. 2.1 (Stereo BTL + Mono PBTL) 3-D View

Layout Examples (continued)

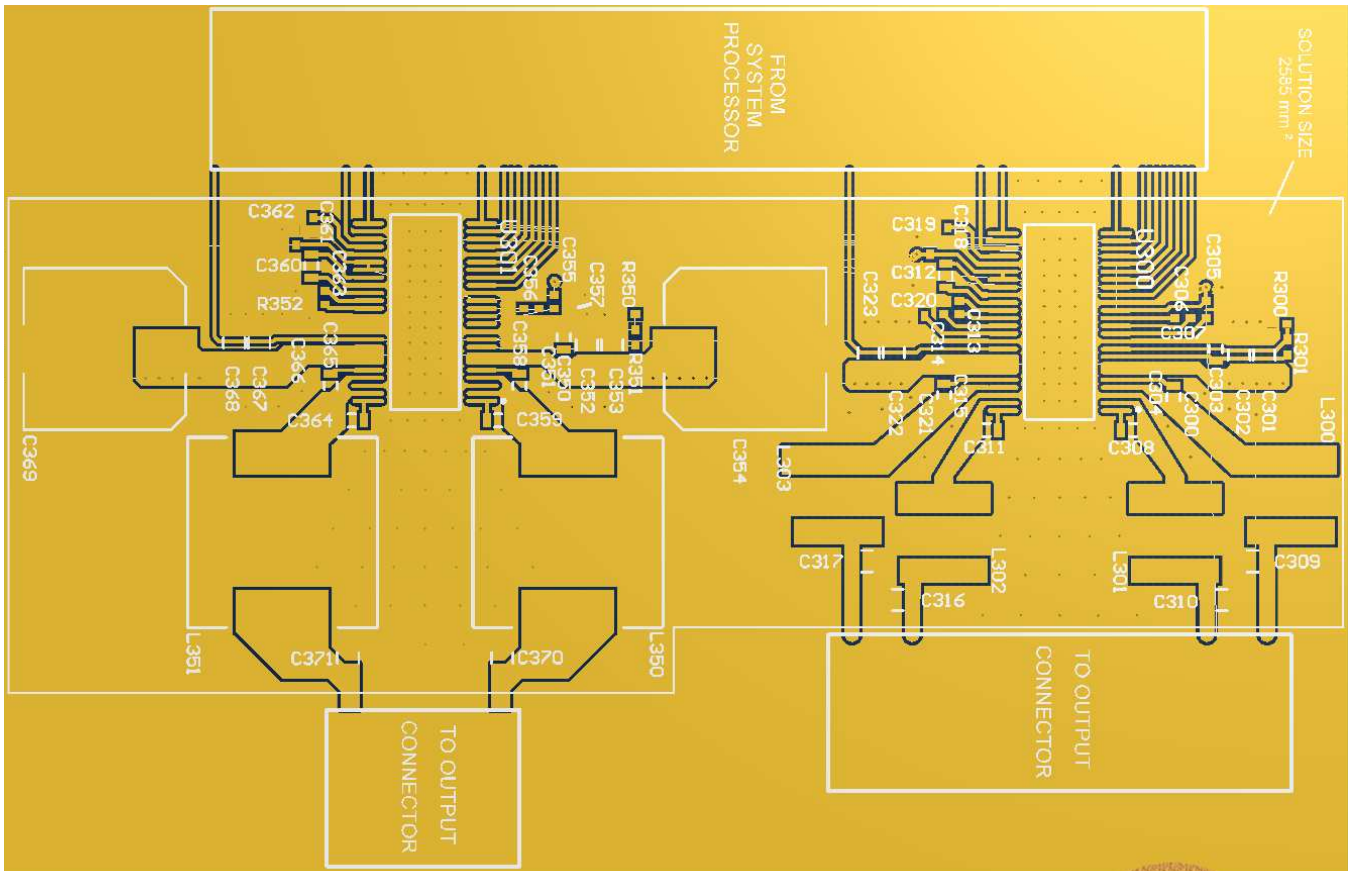


Figure 91. 2.1 (Stereo BTL + Mono PBTL) Top Copper View

Layout Examples (continued)

11.2.4 2.2 (Dual Stereo BTL) Systems

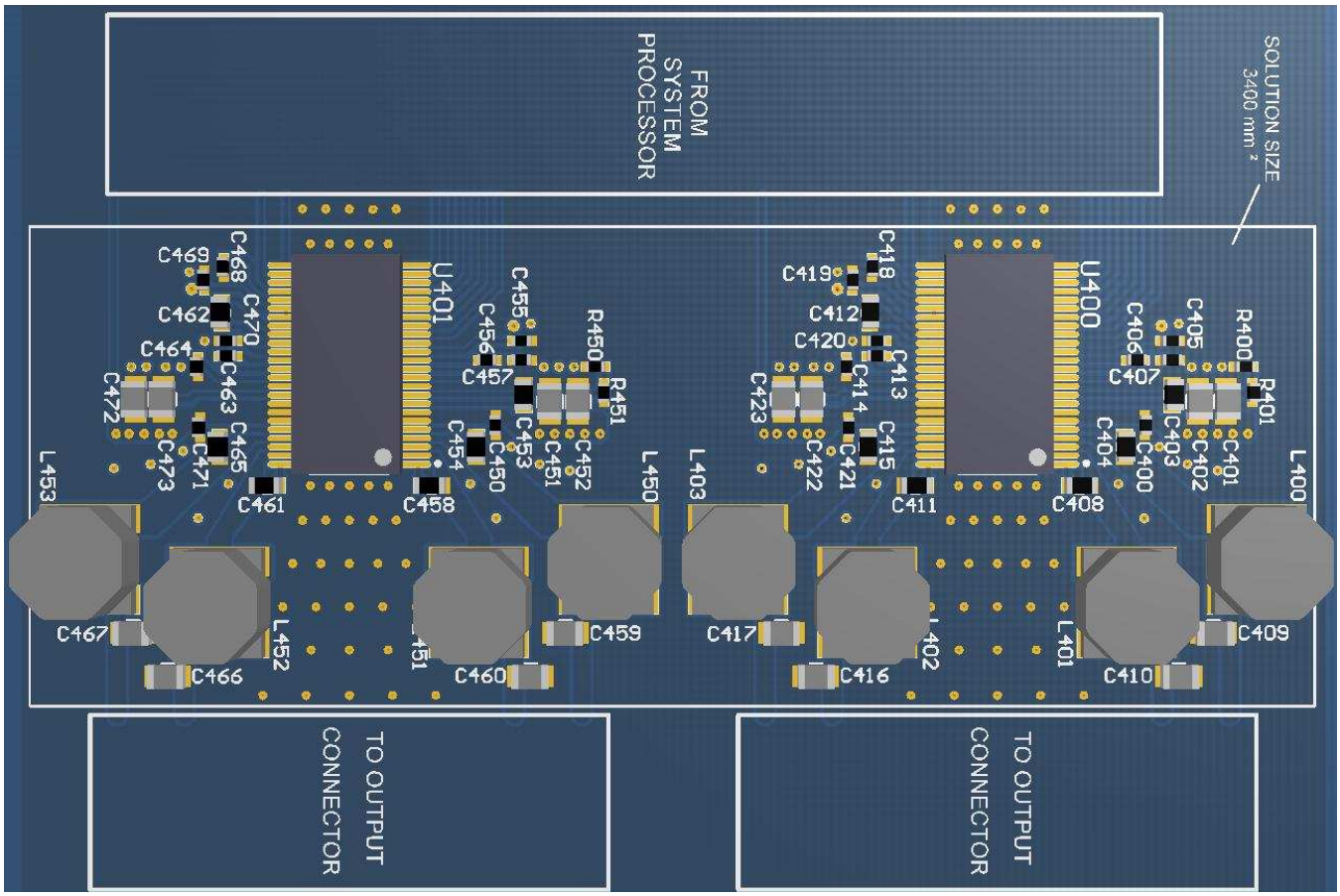


Figure 92. 2.2 (Dual Stereo BTL) 3-D View

Layout Examples (continued)

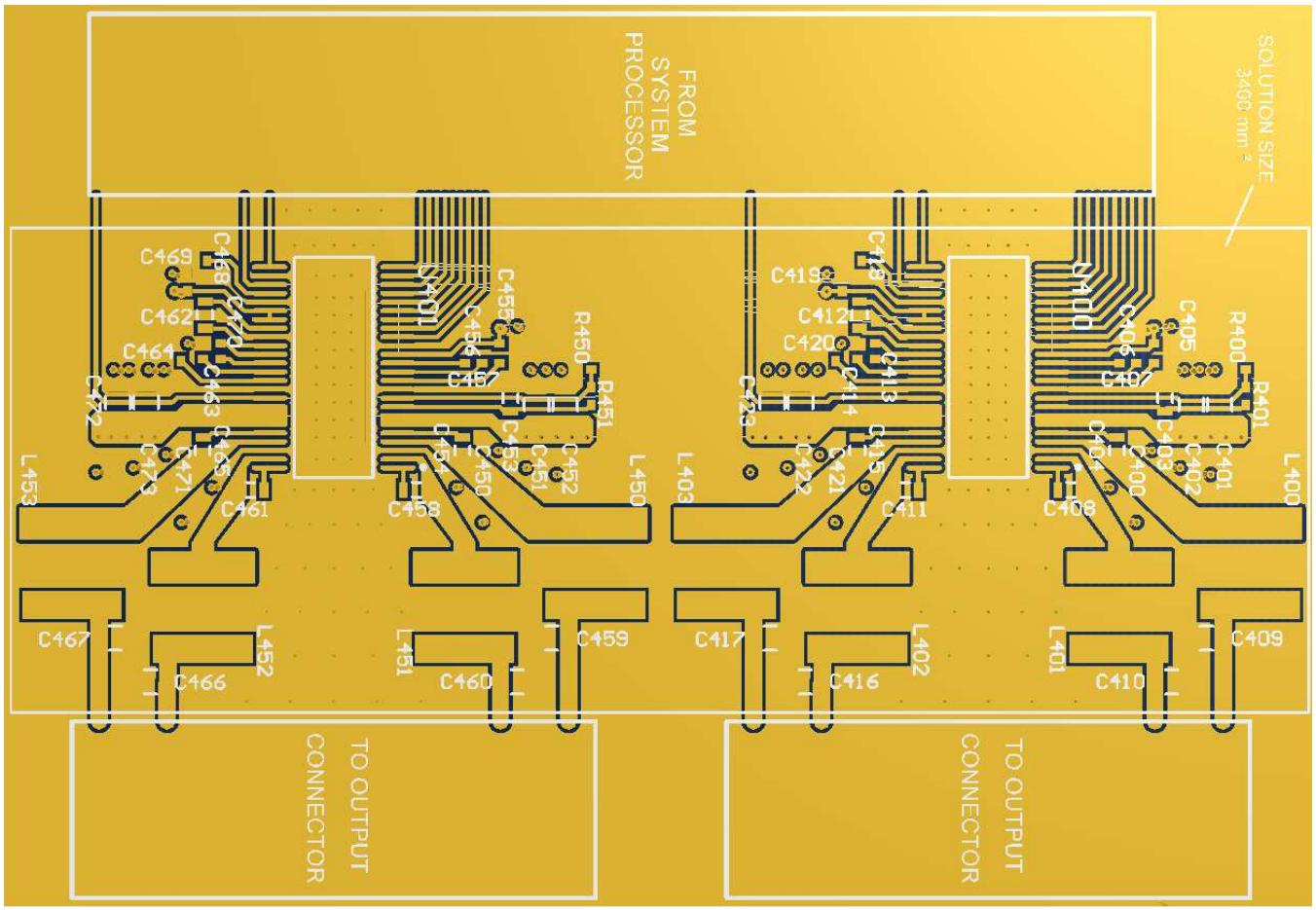


Figure 93. 2.2.2 (Dual Stereo BTL) Top Copper View

Layout Examples (continued)

11.2.5 1.1 (Bi-Amped BTL) Systems

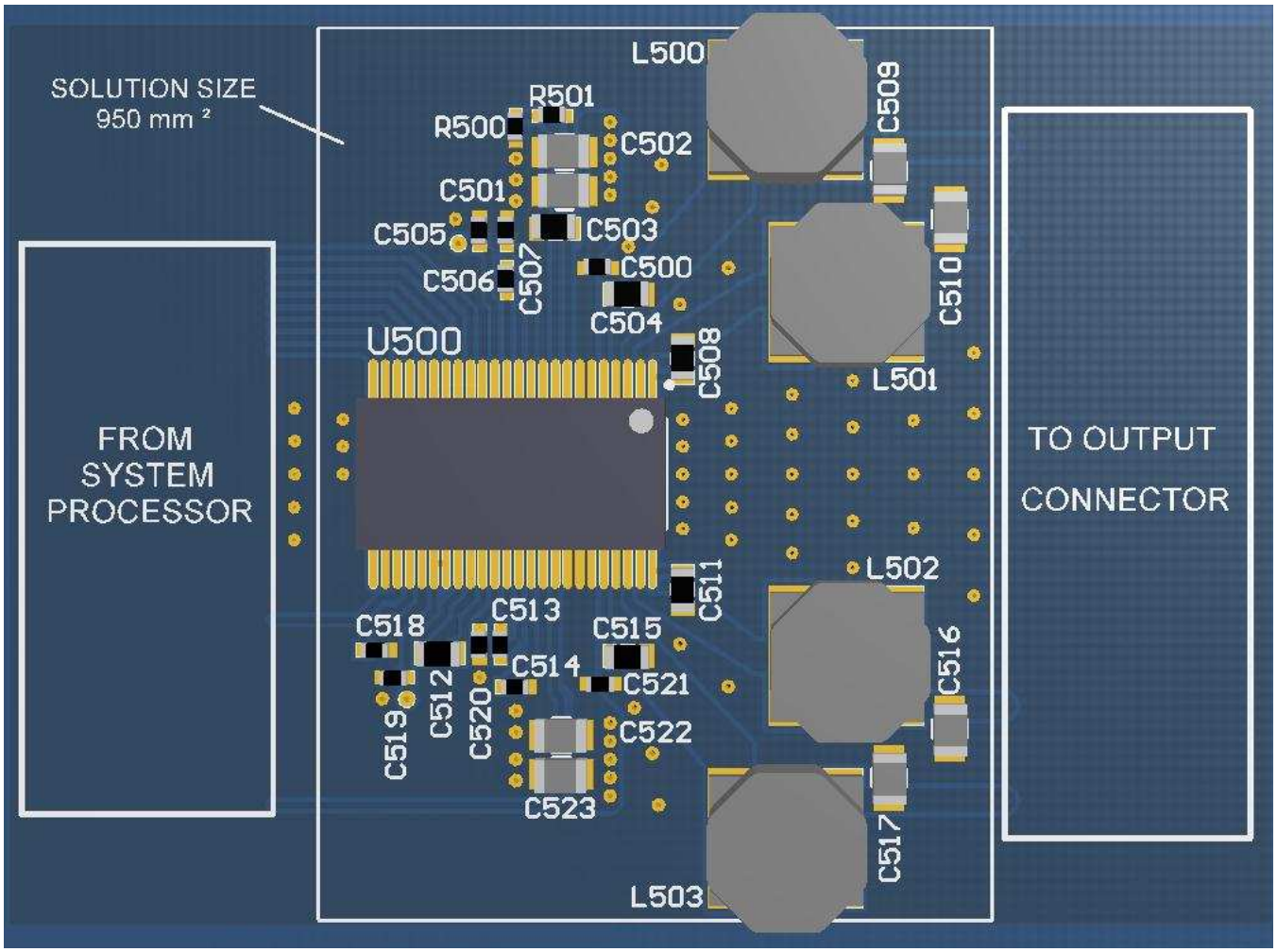


Figure 94. 1.1 (Bi-Amped BTL) 3-D View

Layout Examples (continued)

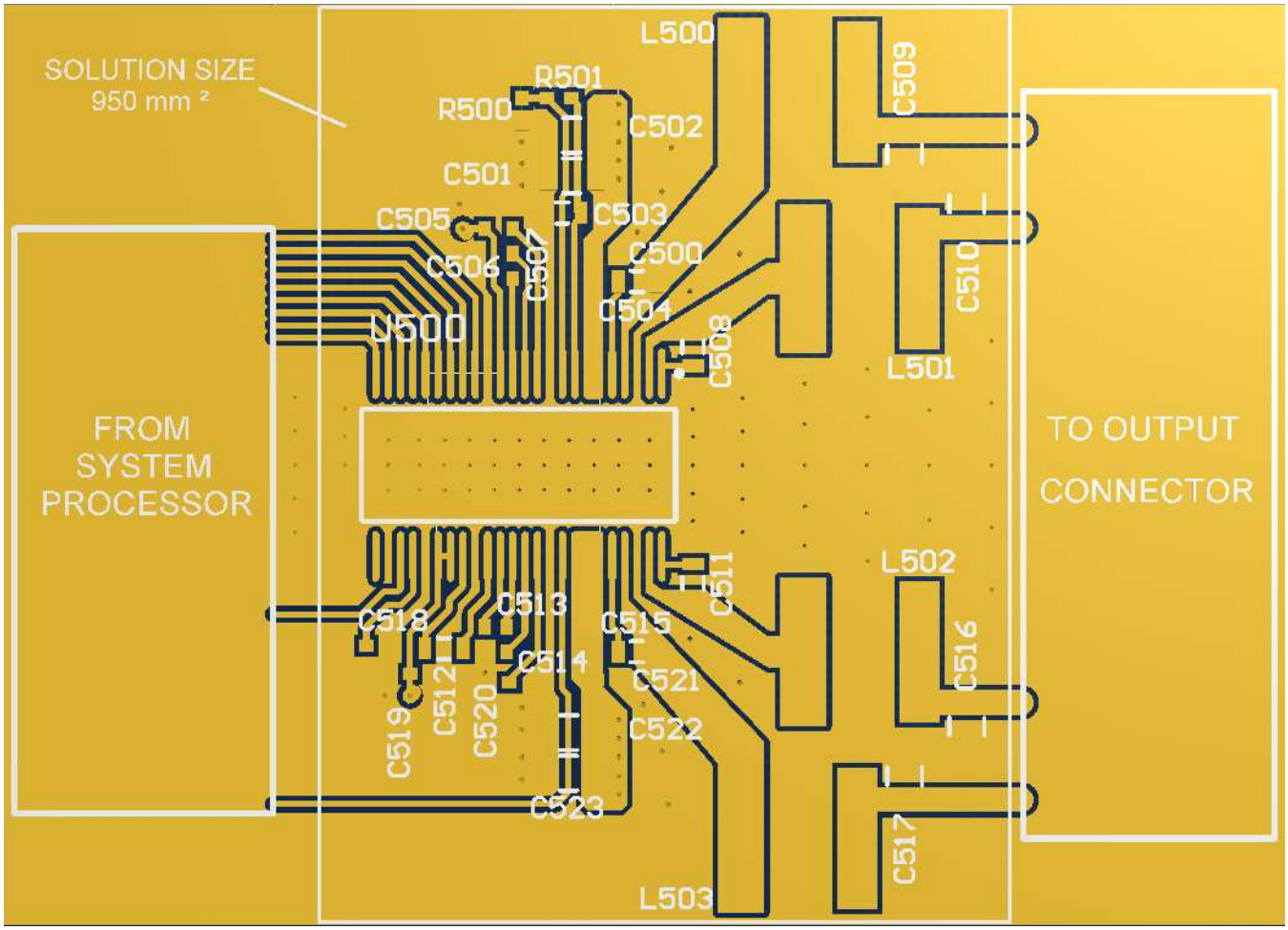


Figure 95. 2. 1.1 (Bi-Amped BTL) Top Copper View

12 Device and Documentation Support

12.1 Device Support

12.1.1 Specification Definitions

The glossary listed in the *Glossary* section is a general glossary with commonly used acronyms and words which are defined in accordance with a broad TI initiative to comply with industry standards such as JEDEC, IPC, IEEE, and others. The glossary provided in this section defines words, phrases, and acronyms that are unique to this product and documentation, collateral, or support tools and software used with this product. For any additional questions regarding definitions and terminology, please see the e2e Audio Amplfier Forum.

Bridge tied load (BTL) is an output configuration in which one terminal of the speaker is connected to one half-bridge and the other terminal is connected to another half-bridge.

DUT refers to a *device under test* to differentiate one device from another.

Closed-loop architecture describes a topology in which the amplifier monitors the output terminals, comparing the output signal to the input signal and attempts to correct for non-linearities in the output.

Dynamic controls are those which are changed during normal use by either the system or the end-user.

GPIO is a general purpose input/output pin. It is a highly configurable, bi-directional digital pin which can perform many functions as required by the system.

Host processor refers to device which serves as a central system controller, providing control information to devices connected to it as well as gathering audio source data from devices upstream from it and distributing it to other devices. Configuring the controls of a device to optimize the audio output of a loudspeaker based on frequency response, time alignment, target sound pressure level, safe operating area of the system, and user preference.

HybridFlow uses components which are built in RAM and components which are built in ROM to make a configurable device that is easier to use than a fully-programmable device while remaining flexible enough to be used in several applications

Maximum continuous output power refers to the maximum output power that the amplifier can continuously deliver without shutting down when operated in a 25°C ambient temperature. Testing is performed for the period of time required that their temperatures reach thermal equilibrium and are no longer increasing

Parallel bridge tied load (PBTL) is an output configuration in which one terminal of the speaker is connected to two half-bridges which have been placed in parallel and the other terminal is connected to another pair of half bridges placed in parallel

$\mathbf{r_{DS(on)}}$ is a measure of the on-resistance of the MOSFETs used in the output stage of the amplifier.

Static configuration information are controls which do not change while the system is in normal use.

Vias are copper-plated through-hole in a PCB.

12.2 Trademarks

PurePath is a trademark of Texas Instruments.
Burr-Brown is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5754MDCA	ACTIVE	HTSSOP	DCA	48	40	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5754M	Samples
TAS5754MDCAR	ACTIVE	HTSSOP	DCA	48	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-25 to 85	TAS5754M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

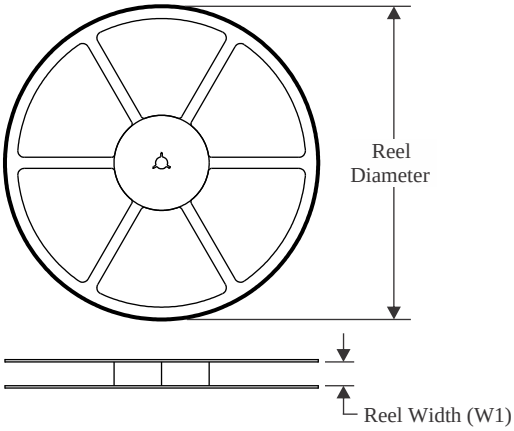
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

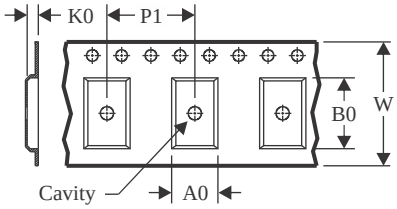
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

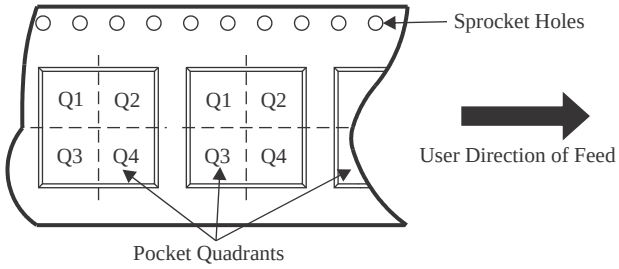


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

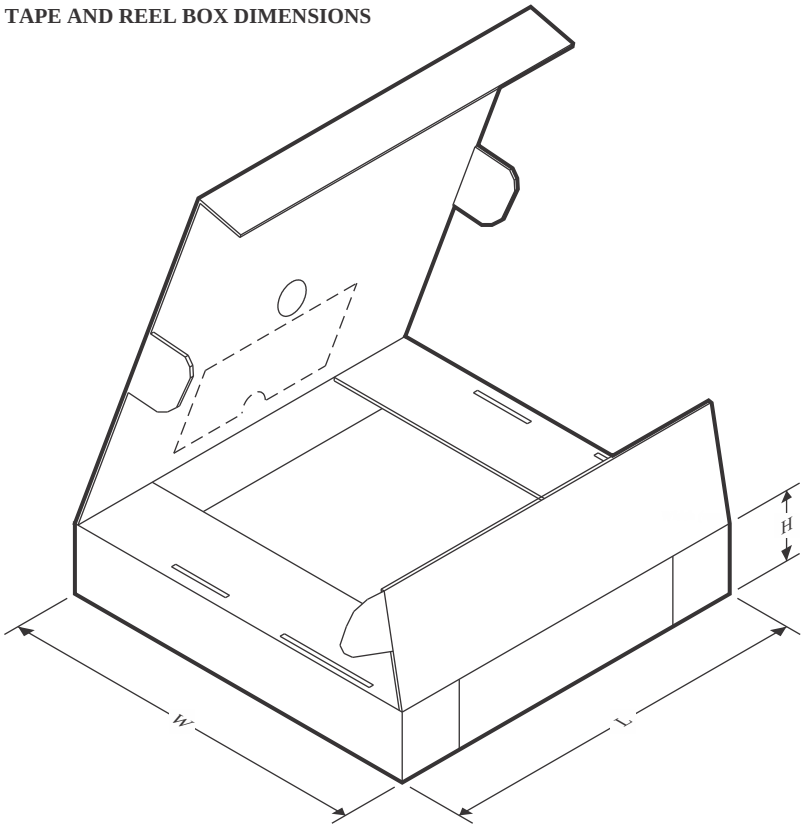
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5754MDCAR	HTSSOP	DCA	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1

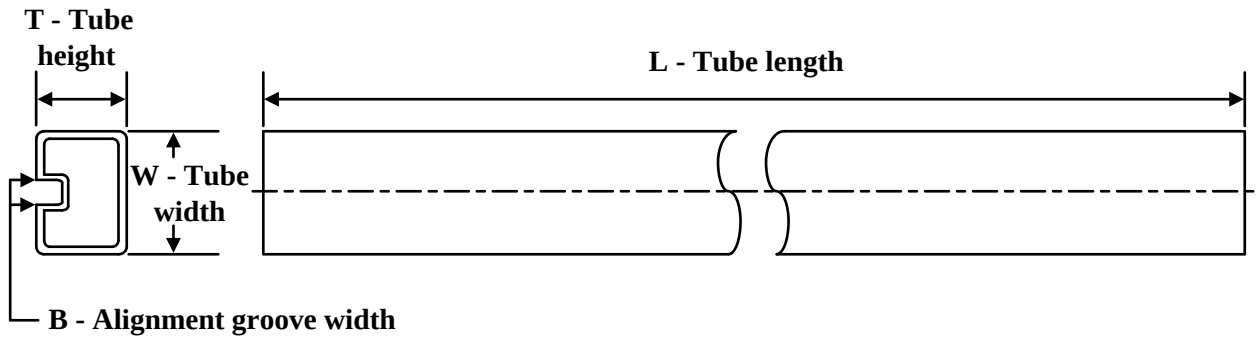
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5754MDCAR	HTSSOP	DCA	48	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5754MDCA	DCA	HTSSOP	48	40	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

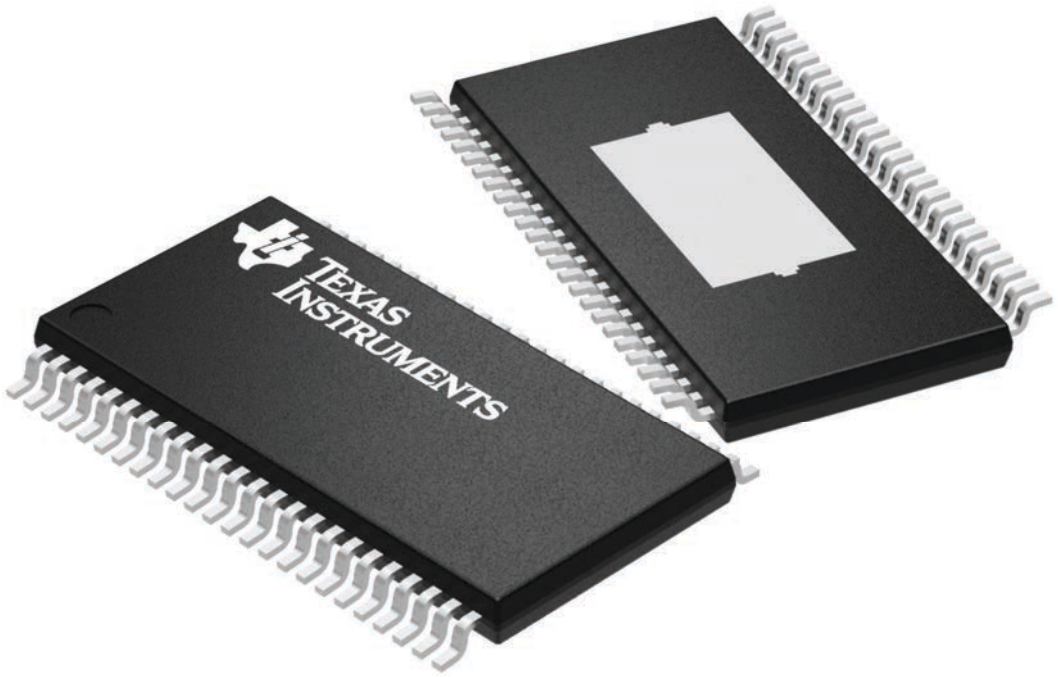
DCA 48

HTSSOP - 1.2 mm max height

12.5 x 6.1, 0.5 mm pitch

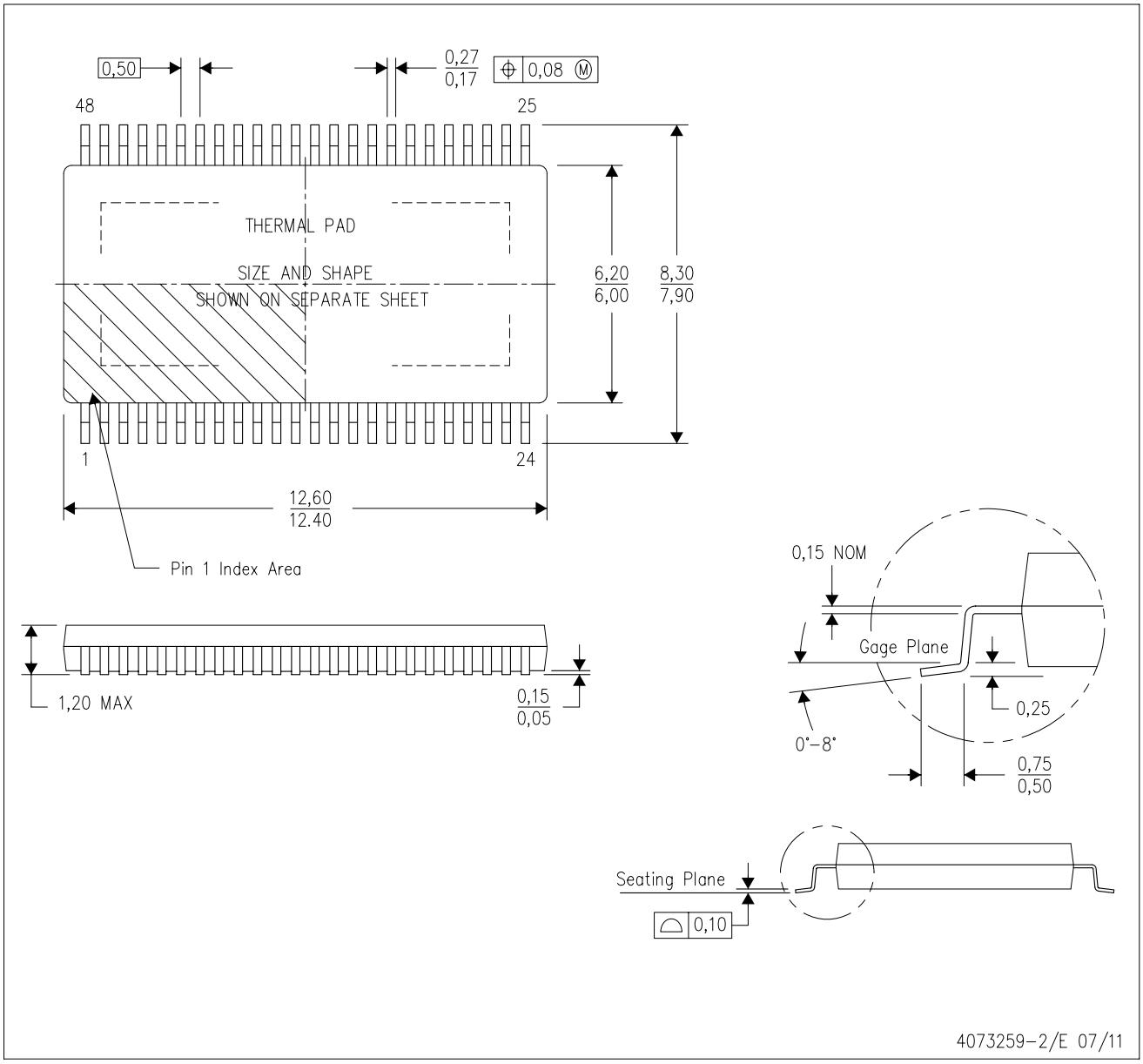
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224608/A

DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–153

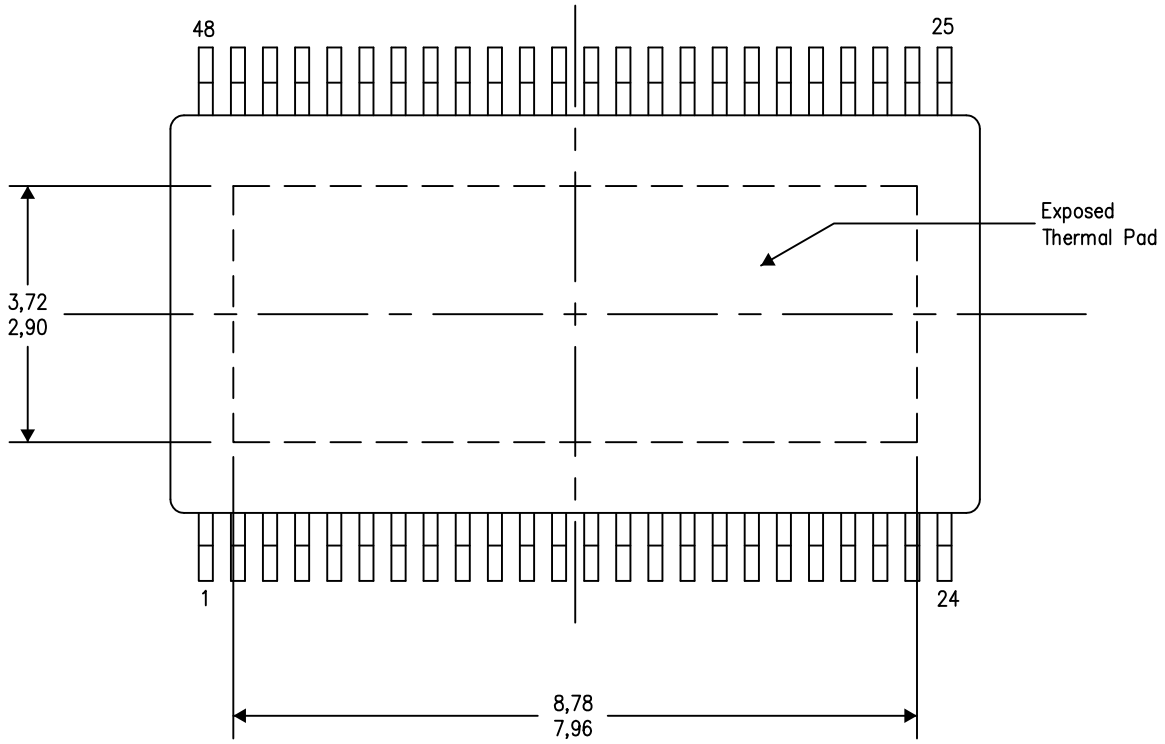
DCA (R–PDSO–G48) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206320–7/S 11/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

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