DLP® Discovery™ 4100 Development Kit Technical Reference Manual

User's Guide

Literature Number: DLPU053
May 2017

This document describes the functionality of the Texas Instruments DLP® Discovery™ 4100 (D4100) Development Kit. The Development Kit provides a reference design and development platform for the D4100 chipset. The D4100 chipset consists of a DLPC410 digital controller, DLPA200 DMD micromirror drivers, DLPR410 PROM, and a digital micromirror device (DMD). The kit is available with four DMD options, two in the visible and two in the ultraviolet (UV) range: DLP7000, DLP7000UV, DLP9500, and DLP9500UV.

Trademarks

Discovery is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.

Overview

The DLP Discovery 4100 is a high performance and highly flexible development kit for a wide variety of light steering applications, such as 3D printing and direct digital imaging. Performance features include resolutions up to 1080p and pattern rates (binary) up to 32552 Hz. These features enable competitive cycle times in industrial markets.

Users of the D4100 Development Kit have the ability to manipulate visible and ultraviolet light with extremely high performance and high resolution. The D4100 offers developers a flexible platform to design products to fit most any application using the proven reliability of DLP technology.

Fast pixel level control of the DMD is provided through the DLPC410 control bus. Both USB and Avnet EXP standard compatible I/O connectors provide a flexible platform for advanced DMD product development. The D4100 supports the following 2XLVDS DMD devices shown in Table 1-1:

Table 1-1. D4100 DMD Types

DMD	Columns	Rows	Global Reset Max Pattern Rate (binary)	Phased Reset Max Pattern Rate (binary)	Data Bus Width
DLP9500 - DLP 0.95 1080p 2xLVDS Type-A DMD	1920	1080	17,636	23,148	64
DLP9500UV - DLP 0.95 1080p 2xLVDS UV Type-A DMD					
DLP7000 - DLP 0.7 XGA 2xLVDS Type-A DMD	1024	768	22,614	32,552	32
DLP7000UV - DLP 0.7 XGA 2xLVDS UV Type-A DMD					

The D4100 Development Kit combines the high performance D4100 chip set with a user programmable Application FPGA (APPSFPGA).

The Virtex 5 (LX50) APPSFPGA provides a user programmable platform for developing custom applications. The APPSFPGA is connected to EXP Expansion Connectors for custom interfaces. An onboard USB interface provides a convenient interface for rapid prototyping. Connections for DDR2 SO-DIMM memory and SPI Flash Memory to the Application FPGA are included for customer use. A Cypress CY7C68013A USB controller is included for customer USB control applications.

This document is provided to facilitate use of the controller board and to provide a reference design for custom hardware development.

1.1 The DLP Discovery D4100 Development Kit

The D4100 Development Kit provides a development platform for general application of the DMD. The D4100 Development Kit includes the following:

- D4100 Controller Board
- DMD board, DMD and flex cable(s)
- Power cable

Not included:

- 5 V @ 6 A power supply (required)
- Xilinx DLC9G programming cable (optional)

Figure 1-1 is a simplified block diagram of the D4100 Development Kit.

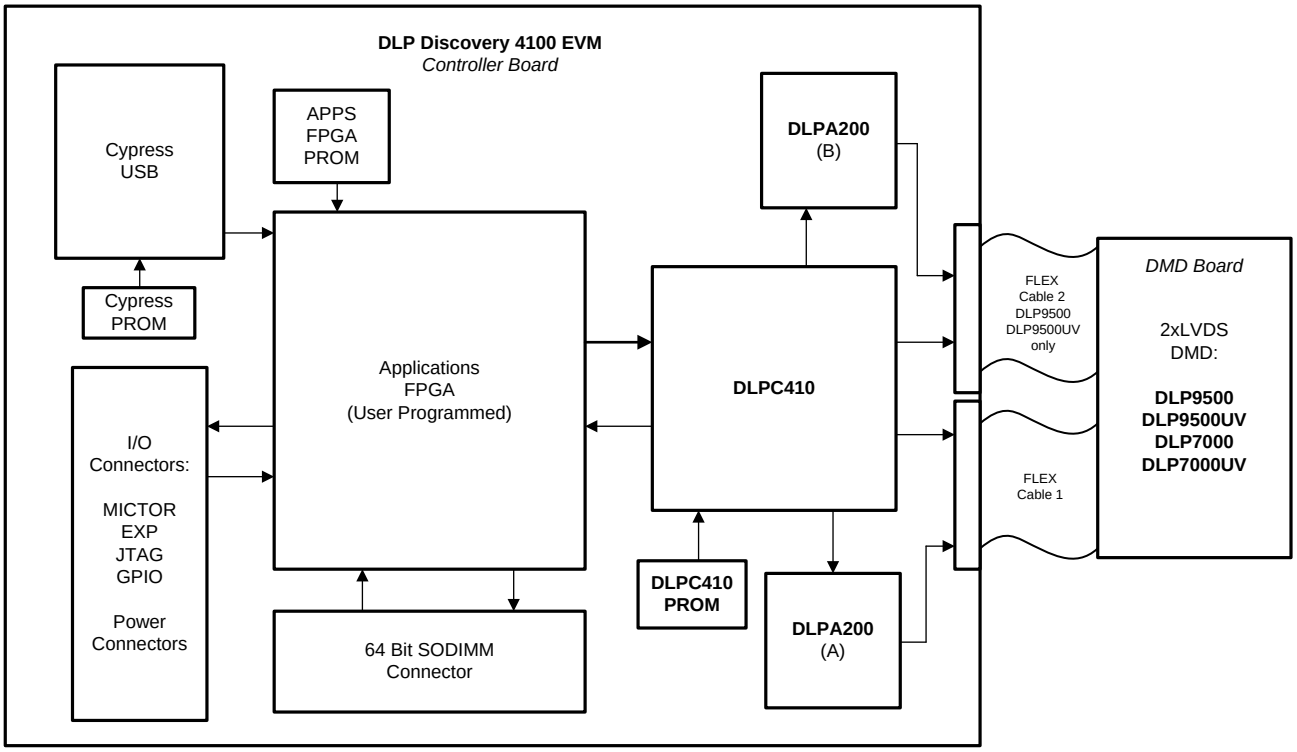

Figure 1-1. D4100 Development Kit Block Diagram

The controller board contains:

- DLPC410 - Digital Controller for DLP Discovery 4100 chipset
  - Provides high speed 32/64 bit LVDS data and control user interface
  - Provides data and control interface to the DMD and DLPA200s
- Two DLPA200 - DMD Micromirror Drivers
  - Generates reset control of 16 banks of DMD mirrors
  - Supports high reset frequencies
  - One DLPA200 required for DLP7000 / DLP7000UV (XGA) operation, and two for DLP9500 / DLP9500UV (1080p) operation
- DLPR410 - PROM for DLP Discovery 4100 chipset
  - Provides configuration data for DLPC410 controller
- 32/64-bit 400 MHz DDR DLPC410 Data Interface
  - 32 bit interface for XGA operation, 64 bit interface for 1080p operation
- 5-V power input connector
  - On-board regulation of other power supplies included
- An APPSFPGA
  - For user development of interface and data manipulation functions
- An APPSFPGA configuration PROM
  - Programmable configuration data for the APPSFPGA for development
- A 64-bit DDR2 SODIMM connector
  - For end user development of image storage
- A Cypress CY7C68013A USB controller
  - For end user development of USB interface

- EXP Expansion Connectors
  - To connect to an EXP compatible interface
  - Board design includes additional LVDS pairs to support 64 bit LVDS connection through EXP connectors with a custom interface board
- Flash Memory (connected to APPSFPGA)
  - Non-volatile storage for end user development
- Various I/O connectors
  - Mictor test connectors for logic analyzer connection
  - JTAG headers for device programming
  - GPIO for general purpose digital I/O

1.2 Development Features

The D4100 Development Kit provides a development solution for the integration of DLP Discovery 4100 chipsets into new applications. Features include:

- A user programmable APPSFPGA (Xilinx Virtex 5 XC5VLX50)
- APPSFPGA platform flash PROM (XCF16P) to load application code
- JTAG connector for APPSFPGA & PROM programming
- Battery support for the APPSFPGA security encryption
- EXP connectors to the APPSFPGA for connection to an EXP compatible board or other accessory board
- Flash memory storage connected to the APPSFPGA
- Cypress CY7C68013A USB
- 64-bit DDR2 SODIMM connector for developer use

1.3 D4100 Photo

The D4100 1080p Development Kit is shown in Figure 1-2.

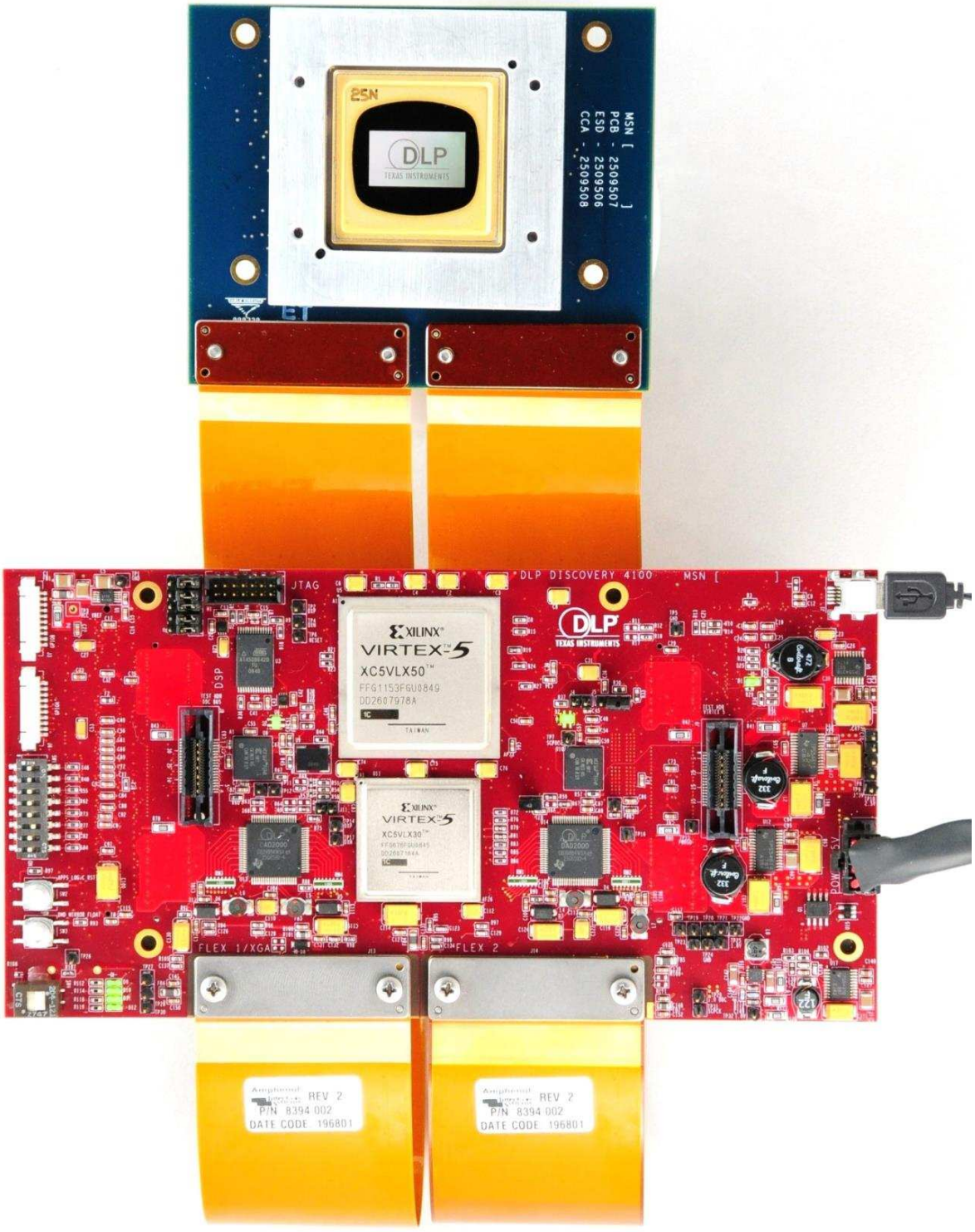

Figure 1-2. D4100 1080p Development Kit Photo

1.4 Key Components

Figure 1-3 shows the D4100 Controller Board key components covered in this section.

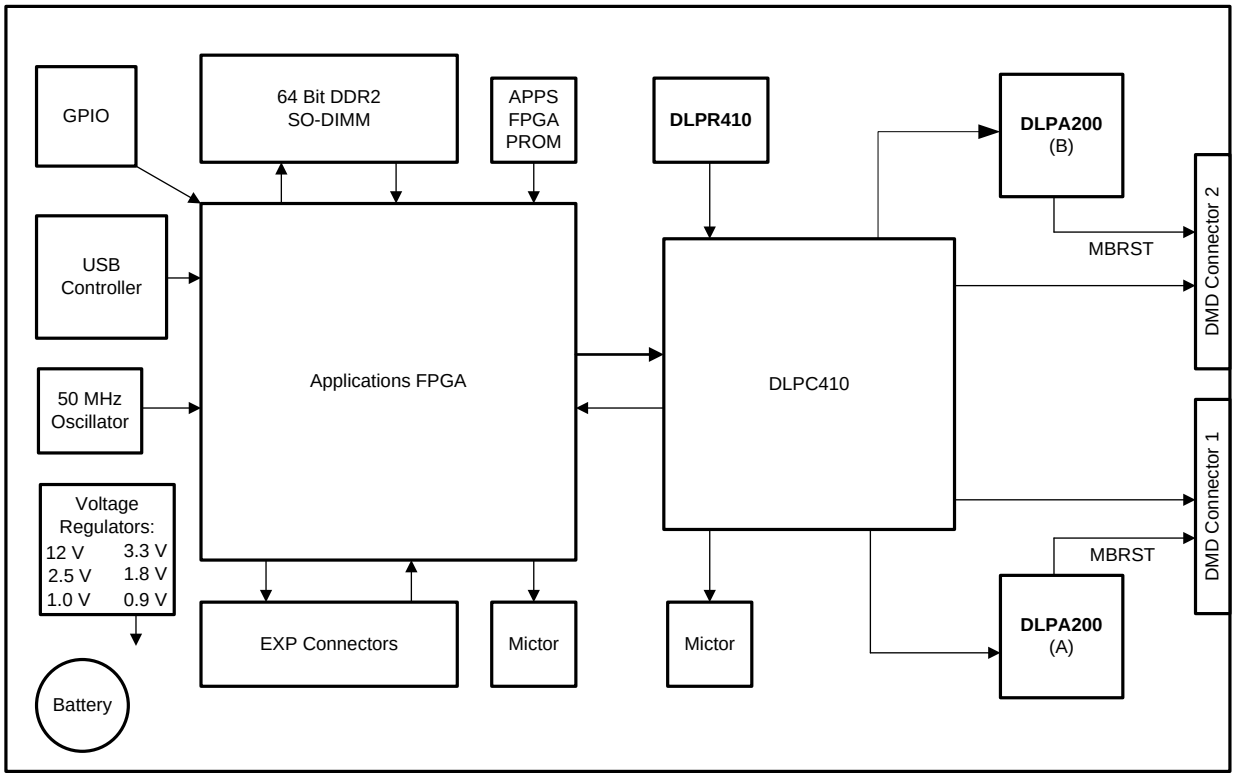

Figure 1-3. D4100 Controller Board Key Components

1.4.1 Xilinx Virtex 5 APPSFPGA

The APPSFPGA (Xilinx Virtex 5 LX50) is used for development of interface and control solutions for the DMD. The APPSFPGA is connected to a number of I/O connectors, interface controllers and memory for use in prototyping a custom control solution prior to developing a custom board solution.

1.4.2 DLPC410 - Digital Controller for DLP Discovery 4100 Chipset

The D4100 chipset includes the DLPC410 controller (configured Xilinx Virtex 5 LX30) which exposes a high-speed LVDS data and control interface for DMD control. This interface is connected to the APPSFPGA to support control from the APPSFPGA. The DLPC410 generates DMD and DLPA200 initialization and control signals in response to the inputs on the control interface.

For more information, refer to the DLPC410 data sheet - DLPS024.

1.4.3 DLPA200 - DMD Micromirror Drivers

Two DLPA200 reset drivers provide the high voltage power and reset driver functions for the DMD. One DLPA200 is required for the DLP7000 / DLP7000UV XGA DMDs, and two for the DLP9500 / DLP9500UV 1080p DMDs. J11 is used to enable/disable the second DLPA200.

For more information on the DLPA200, refer to the DLPA200 data sheet - DLPS015.

1.4.4 DLPR410 - PROM for DLP Discovery 4100 Chipset

The D4100 chipset includes the DLPR410 controller which configures the DLPC410 (Xilinx Virtex 5 LX30). **The contents of this PROM must not be altered and should not be programmed!**

For more information, refer to the DLPR410 data sheet - DLPS027.

1.4.5 50-MHz Oscillator

The controller has a fixed 50-MHz, 2.5-V oscillator connected to the APPSFPGA for clock generation.

1.4.6 USB Controller

A Cypress CY7C68013A USB controller is included for development of USB interface functions.

1.4.7 DDR2 SODIMM Connector

A 64-bit DDR2 SODIMM connector provides a high speed memory connection to the APPSFPGA. Memory controller design for the APPSFPGA is not included. For a memory controller reference design, visit www.xilinx.com.

1.4.8 APPSFPGA Flash Configuration PROM

For APPSFPGA configuration a Xilinx XCF16P Platform Flash PROM is provided. This PROM is pre-loaded with a test pattern generation program. However, the APPSFPGA PROM programming may be changed as needed via JTAG. **We recommend downloading and saving a copy of the pre-loaded test pattern generation program before reprogramming this PROM.**

1.4.9 Connectors

1.4.9.1 JTAG Header H1

The H1 JTAG header port provides a programming interface to the APPSFPGA and flash configuration PROM.

1.4.9.2 Mictor Connectors

The Mictor connectors support connection of a logic analyzer to the APPSFPGA and the Cypress 69013A signals for development support.

1.4.9.3 DMD Connectors

Two DMD connectors accept the DMD flex cable(s). Connect flex cables to J13 and J14 for a 1080p DMD board. Connect one flex cable to J13 for a XGA DMD board.

1.4.9.4 GPIO Connectors

General purpose digital I/O connectors.

1.4.10 Battery

A battery provides power for encryption security in the Virtex 5 FPGA. See Xilinx Virtex 5 data sheet for more detail.

1.4.11 Power Supplies

Onboard voltage regulation is provided for all required power supplies. This section lists controller voltage regulators and their purpose(s).

1.4.11.1 J12 Power Connector

This provides up to 6 A at 5 V to the D4100 controller board.

1.4.11.2 VREG 0.9 V

This delivers 1 A at 0.9 V as a DDR2 reference voltage supply.

1.4.11.3 VREG 1.0 V

This delivers 3 A at 1.0 V as the Virtex 5 core supply.

1.4.11.4 VREG 1.8 V

This delivers 3 A at 1.8 V for the DDR2 supply and FPGA I/O.

1.4.11.5 VREG 2.5 V

This delivers 6 A at 2.5 V to supply the XCF16 FPGA I/O.

1.4.11.6 VREG 3.3 V

This delivers 3 A at 3.3 V to supply the DMD and USB controller.

1.4.11.7 VREG 12 V

This delivers the 0.5 A at 12 V to supply the DLPA200.

Getting Started

The following steps should be followed in starting board operation using the default APPSFPGA code installed at the factory:

1. Connect a 5-V, 6-A power supply to the supplied power cable. Connect the power cable to J12 with the power supply OFF.
2. Confirm all SW1 switches are in the OFF position. Confirm all five J2 jumpers are in place. If using a DLP9500 / DLP9500UV 1080p DMD confirm J10 is installed.
3. Connect the DMD to the board with the flex cable(s). One flex cable attached to J13 is used for DLP7000 / DLP7000UV XGA DMDs, two flex cables attached to J13 and J14 are used for DLP9500 / DLP9500UV 1080p DMD.
4. Turn the power supply ON and then turn on SW4. D2 and D3 should briefly display red then green to indicate APPSFPGA and DLPC410 configuration. D9 should flash green at 1 Hz. D10 should display green. The DMD will repeatedly cycle through several test patterns.

To stop operation:

1. It is recommended to float the DMD mirrors to set the mirrors to a flat state before powering off. Press SW3 to float the DMD.
2. Turn power OFF.

User Connectors and I/O

This section describes the use of each D4100 Controller Board external connector and provides pin out information. Figure 3-1 and Figure 3-2 show connector locations on the D4100 controller board.

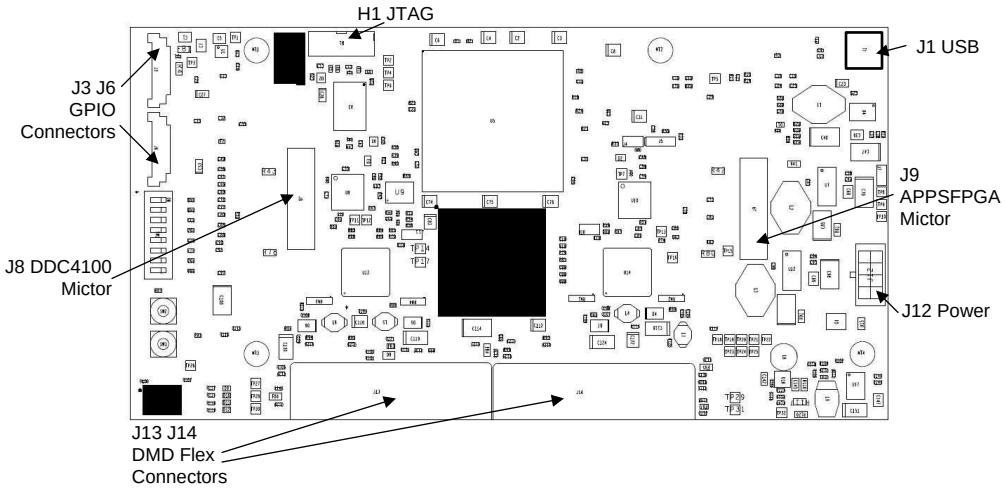

Figure 3-1. D4100 Controller Connectors (Top View)

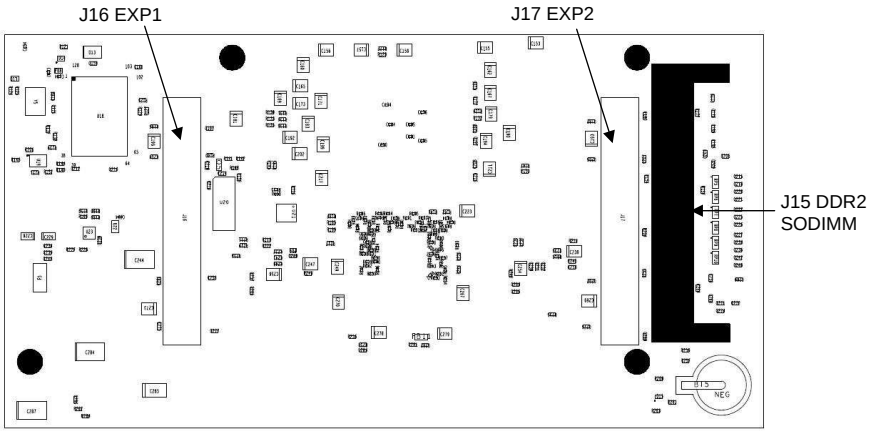

Figure 3-2. D4100 Controller Connectors (Bottom View)

3.1 J1 USB Connector Pinout

Connector J1 provides USB input to the controller board.

Table 3-1. J1 USB

Pin Number	Pin Name	Pin Number	Pin Name
1	USB_5V	2	D-
3	D+	4	NC
5	GND		

3.2 J3 USB GPIO

Connector J3 provides eight general purpose USB I/O pin connections to the USB Controller.

Table 3-2. J3 USB GPIO

Pin Number	Pin Name	Pin Number	Pin Name
1	3.3V	6	USB_GPIO B3
2	USB_GPIO B7	7	USB_GPIO B2
3	USB_GPIO B6	8	USB_GPIO B1
4	USB_GPIO B5	9	USB_GPIO B0
5	USB_GPIO B4	10	GND

3.3 J6 GPIO_A Connector

Connector J6 provides eight general purpose I/O pins to the APPSFPGA.

Table 3-3. J6 GPIO_A Connector

Pin Number	Pin Name	APPSFPGA Pin Number	Pin Number	Pin Name	APPSFPGA Pin Number
1	2.5V	NC	6	GPIO A3	AG16
2	GPIO A7	AF20	7	GPIO A2	AG17
3	GPIO A6	AF19	8	GPIO A1	AH19
4	GPIO A5	AG12	9	GPIO A0	AG20
5	GPIO A4	AH12	10	GND	NC

3.4 J8 DLPC410 Mictor Connector

J8 provides connection to the DLPC410 for a logic analyzer. This connector should not be used for normal development or operation.

Table 3-4. J8 DLPC410 Mictor Connector

J8 Pin Number	Pin Name	DLPC410 Pin Number	J8 Pin Number	Pin Name	DLPC410 Pin Number
1	NC	NC	2	ECP2_M_TP0	AD9
3	GND	NC	4	ECP2_M_TP1	AA11
5	DDCSPARE0	L7	6	ECP2_M_TP2	W11
7	DDCSPARE1	AC13	8	ECP2_M_TP3	AB26
9	NC	NC	10	ECP2_M_TP4	AB9
11	NC	NC	12	ECP2_M_TP5	AB11
13	ECP2_M_TP31	AA13	14	ECP2_M_TP6	AA10
15	ECP2_M_TP3O	AB13	16	ECP2_M_TP7	AA12
17	ECP2_M_TP29	AD14	18	ECP2_M_TP8	Y11
19	ECP2_M_TP28	L5	20	ECP2_M_TP9	AB17
21	ECP2_M_TP27	AC14	22	ECP2_M_TP10	AA17
23	ECP2_M_TP26	AB15	24	ECP2_M_TP11	AA15
25	ECP2_M_TP25	H19	26	ECP2_M_TP12	AF12
27	ECP2_M_TP24	J18	28	ECP2_M_TP13	AE11
29	ECP2_M_TP23	H18	30	ECP2_M_TP14	AC9
31	ECP2_M_TP22	G15	32	ECP2_M_TP15	AF11
33	ECP2_M_TP21	G14	34	ECP2_M_TP16	AB12
35	ECP2_M_TP20	H17	36	ECP2_M_TP17	AA16
37	ECP2_M_TP19	G20	38	ECP2_M_TP18	AD13

3.5 J9 USB/APPSFPGA Mictor Connector

J9 is the Mictor connector for the USB controller and APPSFPGA. Signals from the USB or APPSFPGA are routed to the connector as selected by jumper J6. Refer to the D4100 controller board schematic (DLPC410 Board Design Files) for more information. Signals can be routed to the connector by HDL code and monitored with a logic analyzer to support development.

Table 3-5. J9 USB/APPSFPGA Mictor Connector

J9 Pin Number	Pin Name	APPSFPGA Pin Number	J9 Pin Number	Pin Name	APPSFPGA Pin Number
1	NC	NC	2	NC	NC
3	GND	NC	4	D4100_I2C_CLK	P29
5	USB_IF_CLK/TEST_CLK_0	N29	6	D4100_I2C_DATA	U28
7	USB_FDO/TST_HDR_BY0_0	H29	8	GPIFADR0/TST_HDR_BY2_0	K31
9	USB_FD1/TST_HDR_BY0_1	H30	10	GPIFADR1/TST_HDR_BY2_1	L31
11	USB_FD2/TST_HDR_BY0_2	J31	12	GPIFADR2/TST_HDR_BY2_2	P31
13	USB_FD3/TST_HDR_BY0_3	G30	14	GPIFADR3/TST_HDR_BY2_3	P30
15	USB_FD4/TST_HDR_BY0_4	J30	16	GPIFADR4/TST_HDR_BY2_4	N30
17	USB_FD5/TST_HDR_BY0_5	G31	18	GPIFADR5/TST_HDR_BY2_5	M31
19	USB_FD6/TST_HDR_BY0_6	J29	20	GPIFADR6/TST_HDR_BY2_6	R28
21	USB_FD7/TST_HDR_BY0_7	F29	22	GPIFADR7/TST_HDR_BY2_7	R29
23	USB_FD8/TST_HDR_BY1_0	K29	24	GPIFADR8/TST_HDR_BY3_0	T31
25	USB_FD9/TST_HDR_BY1_1	F30	26	USB_CTRL0/TST_HDR_BY3_1	R31
27	USB_FD1O/TST_HDR_BY1_2	L30	28	USB_CTRL1/TST_HDR_BY3_2	U30
29	USB_FD11/TST_HDR_BY1_3	F31	30	USB_CTRL2/TST_HDR_BY3_3	T30
31	USB_FD12/TST_HDR_BY1_4	L29	32	USB_CTRL3/TST_HDR_BY3_4	T28
33	USB_FD13/TST_HDR_BY1_5	E29	34	USB_FPGA_RESET/TST_HDR_BY3_5	T29
35	USB_FD14/TST_HDR_BY1_6	E31	36	USB_INT5/TST_HDR_BY3_6	U27
37	USB_FD15/TST_HDR_BY1_7	M30	38	NC	NC

3.6 J13 DMD Flex Connector 1

Connector J13 provides control and data signals to the DMD flex connector 1. This connector is used for connection to all DMD types.

Table 3-6. J13 DMD Flex Connector 1

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1A	GND	1B	3.3V	1C	3.3V
2C	GND	2A	DDC_DOUT_A13_DPP	2B	DDC_DOUT_A13_DPN
3A	GND	3B	DDC_DOUT_A11_DPP	3C	DDC_DOUT_A11_DPN
4C	GND	4A	DDC_DOUT_A9_DPP	4B	DDC_DOUT_A9_DPN
5A	GND	5B	DDC_DCLKOUT_A_DPP	5C	DDC_DCLKOUT_A_DPN
6C	GND	6A	DDC_DOUT_A7_DPP	6B	DDC_DOUT_A7_DPP
7A	GND	7B	DDC_DOUT_A5_DPP	7C	DDC_DOUT_A5_DPN
8C	GND	8A	DDC_DOUT_A3_DPP	8B	DDC_DOUT_A3_DPN
9A	GND	9B	DDC_DOUT_A1_DPP	9C	DDC_DOUT_A1_DPN
10C	GND	10A	DAD_A_SCPDO	10B	DAD_A_SCPCLK
11A	GND	11B	DMDSPARE1	11C	DMD_A_SCPEN
12C	GND	12A	MBRST1_15	12B	MBRST1_14
13A	GND	13B	DMD_VCC2	13C	DMD_VCC2
14C	GND	14A	MBRST1_10	14B	MBRST1_6
15A	GND	15B	MBRST1_9	15C	MBRST1_7
16C	GND	16A	MBRST1_13	16B	MBRST1_12
17A	GND	17B	DDC_DOUT_B1_DPP	17C	DDC_DOUT_B1_DPN
18C	GND	18A	DDC_DOUT_B3_DPP	18B	DDC_DOUT_B3_DPN
19A	GND	19B	DDC_DOUT_B5_DPP	19C	DDC_DOUT_B5_DPN
20C	GND	20A	DDC_DOUT_B7_DPP	20B	DDC_DOUT_B7_DPN
21A	GND	21B	DDC_DCLKOUT_B_DPP	21C	DDC_DCLKOUT_B_DPN
22C	GND	22A	DDC_DOUT_B9_DPP	22B	DDC_DOUT_B9_DPN
23A	GND	23B	DDC_DOUT_B11_DPP	23C	DDC_DOUT_B11_DPN
24C	GND	24A	DDC_DOUT_B13_DPP	24B	DDC_DOUT_B13_DPN
25A	GND	25B	DDC_DOUT_B15_DPP	25C	DDC_DOUT_B15_DPN
1D	GND	1E	DDC_DOUT_A15_DPP	1F	DDC_DOUT_A15_DPN
2F	GND	2D	DDC_DOUT_A14_DPP	2E	DDC_DOUT_A14_DPN
3D	GND	3E	DDC_DOUT_A12_DPP	3F	DDC_DOUT_A12_DPN
4F	GND	4D	DDC_DOUT_A10_DPP	4E	DDC_DOUT_A10_DPN
5D	GND	5E	DDC_DOUT_A8_DPP	5F	DDC_DOUT_A8_DPN
6F	GND	6D	DDC_SCTRL_A_DPP	6E	DDC_SCTRL_A_DPN
7D	GND	7E	DDC_DOUT_A6_DPP	7F	DDC_DOUT_A6_DPN
8F	GND	8D	DDC_DOUT_A4_DPP	8E	DDC_DOUT_A4_DPN
9D	GND	9E	DDC_DOUT_A2_DPP	9F	DDC_DOUT_A2_DPN
10F	GND	10D	DDC_DOUT_A0_DPP	10E	DDC_DOUT_A0_DPN
11D	GND	11E	SCPDI	11F	DMD_A_RESET
12F	GND	12D	DMDSPARE0	12E	MBRST1_11
13D	GND	13E	MBRST1_5	13F	MBRST1_4
14F	GND	14D	MBRST1_0	14E	MBRST1_3
15D	GND	15E	MBRST1_2	15F	MBRST1_8
16F	GND	16D	DDC_DOUT_B0_DPP	16E	DDC_DOUT_B0_DPN
17D	GND	17E	DDC_DOUT_B2_DPP	17F	DDC_DOUT_B2_DPN
18F	GND	18D	DDC_DOUT_B4_DPP	18E	DDC_DOUT_B4_DPN
19D	GND	19E	DDC_DOUT_B6_DPP	19F	DDC_DOUT_B6_DPN
20F	GND	20D	DDC_SCTRL_B_DPP	20E	DDC_SCTRL_B_DPP
21D	GND	21E	DDC_DOUT_B8_DPP	21F	DDC_DOUT_B8_DPN
22F	GND	22D	DDC_DOUT_B10_DPP	22E	DDC_DOUT_B10_DPN
23D	GND	23E	DDC_DOUT_B12_DPP	23F	DDC_DOUT_B12_DPN
24F	GND	24D	DDC_DOUT_B14_DPP	24E	DDC_DOUT_B14_DPN
25D	GND	25E	3.3V	25F	3.3V

3.7 J14 DMD Flex Connector 2

Connector J14 provides control and data signals to the DMD flex connector 2. This connector is only used for connection to DLP9500 and DLP9500UV DMDs.

Table 3-7. J14 DMD Flex Connector 2

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1A	GND	1B	3.3V	1C	3.3V
2C	GND	2A	DDC_DOUT_C13_DPP	2B	DDC_DOUT_C13_DPN
3A	GND	3B	DDC_DOUT_C11_DPP	3C	DDC_DOUT_C11_DPN
4C	GND	4A	DDC_DOUT_C9_DPP	4B	DDC_DOUT_C9_DPN
5A	GND	5B	DDC_DCLKOUT_C_DPP	5C	DDC_DCLKOUT_C_DPN
6C	GND	6A	DDC_DOUT_C7_DPP	6B	DDC_DOUT_C7_DPP
7A	GND	7B	DDC_DOUT_C5_DPP	7C	DDC_DOUT_C5_DPN
8C	GND	8A	DDC_DOUT_C3_DPP	8B	DDC_DOUT_C3_DPN
9A	GND	9B	DDC_DOUT_C1_DPP	9C	DDC_DOUT_C1_DPN
10C	GND	10A	DAD_B_SCPDO	10B	DAD_B_SCPCLK
11A	GND	11B	DMDSPARE2	11C	DMD_B_SCPEN
12C	GND	12A	MBRST2_15	12B	MBRST2_14
13A	GND	13B	DMD_VCC2	13C	DMD_VCC2
14C	GND	14A	MBRST2_10	14B	MBRST2_6
15A	GND	15B	MBRST2_9	15C	MBRST2_7
16C	GND	16A	MBRST2_13	16B	MBRST2_12
17A	GND	17B	DDC_DOUT_D1_DPP	17C	DDC_DOUT_D1_DPN
18C	GND	18A	DDC_DOUT_D3_DPP	18B	DDC_DOUT_D3_DPN
19A	GND	19B	DDC_DOUT_D5_DPP	19C	DDC_DOUT_D5_DPN
20C	GND	20A	DDC_DOUT_D7_DPP	20B	DDC_DOUT_D7_DPN
21A	GND	21B	DDC_DCLKOUT_D_DPP	21C	DDC_DCLKOUT_D_DPN
22C	GND	22A	DDC_DOUT_D9_DPP	22B	DDC_DOUT_D9_DPN
23A	GND	23B	DDC_DOUT_D11_DPP	23C	DDC_DOUT_D11_DPN
24C	GND	24A	DDC_DOUT_D13_DPP	24B	DDC_DOUT_D13_DPN
25A	GND	25B	DDC_DOUT_D15_DPP	25C	DDC_DOUT_D15_DPN
1D	GND	1E	DDC_DOUT_C15_DPP	1F	DDC_DOUT_C15_DPN
2F	GND	2D	DDC_DOUT_C14_DPP	2E	DDC_DOUT_C14_DPN
3D	GND	3E	DDC_DOUT_C12_DPP	3F	DDC_DOUT_C12_DPN
4F	GND	4D	DDC_DOUT_C10_DPP	4E	DDC_DOUT_C10_DPN
5D	GND	5E	DDC_DOUT_C8_DPP	5F	DDC_DOUT_C8_DPN
6F	GND	6D	DDC_SCTRL_C_DPP	6E	DDC_SCTRL_C_DPN
7D	GND	7E	DDC_DOUT_C6_DPP	7F	DDC_DOUT_C6_DPN
8F	GND	8D	DDC_DOUT_C4_DPP	8E	DDC_DOUT_C4_DPN
9D	GND	9E	DDC_DOUT_C2_DPP	9F	DDC_DOUT_C2_DPN
10F	GND	10D	DDC_DOUT_C0_DPP	10E	DDC_DOUT_C0_DPN
11D	GND	11E	SCPDI	11F	DMD_B_RESET
12F	GND	12D	DMDSPARE0	12E	MBRST2_11
13D	GND	13E	MBRST2_5	13F	MBRST2_4
14F	GND	14D	MBRST2_0	14E	MBRST2_3
15D	GND	15E	MBRST2_2	15F	MBRST2_8
16F	GND	16D	DDC_DOUT_D0_DPP	16E	DDC_DOUT_D0_DPN
17D	GND	17E	DDC_DOUT_D2_DPP	17F	DDC_DOUT_D2_DPN
18F	GND	18D	DDC_DOUT_D4_DPP	18E	DDC_DOUT_D4_DPN
19D	GND	19E	DDC_DOUT_D6_DPP	19F	DDC_DOUT_D6_DPN
20F	GND	20D	DDC_SCTRL_D_DPP	20E	DDC_SCTRL_D_DPP
21D	GND	21E	DDC_DOUT_D8_DPP	21F	DDC_DOUT_D8_DPN
22F	GND	22D	DDC_DOUT_D10_DPP	22E	DDC_DOUT_D10_DPN
23D	GND	23E	DDC_DOUT_D12_DPP	23F	DDC_DOUT_D12_DPN
24F	GND	24D	DDC_DOUT_D14_DPP	24E	DDC_DOUT_D14_DPN
25D	GND	25E	3.3V	25F	3.3V

3.8 J15 DDR2 SODIMM Connector

Connector J15 provides a DDR2 SODIMM memory socket. No memory module is included. Memory controller design for the APPSFPGA is not included. For a memory controller reference design, visit www.xilinx.com.

Table 3-8. J15 DDR2 SODIMM Connector

Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name	Pin Number	Pin Name
1	VCC_VREF	2	GND	3	GND	4	DDR2_D4
5	DDR2_D0	6	DDR2_D5	7	DDR2_D1	8	GND
9	GND	10	DDR2_DM0	11	DDR2_DQS0_N	12	GND
13	DDR2_DQS0_P	14	DDR2_D6	15	GND	16	DDR2_D7
17	DDR2_D2	18	GND	19	DDR2_D3	20	DDR2_D12
21	GND	22	DDR2_D13	23	DDR2_D8	24	GND
25	DDR2_D9	26	DDR2_DM1	27	GND	28	GND
29	DDR2_DOS1_N	30	DDR2_CK0_P	31	DDR2_DOS1_P	32	DDR2_CK0_N
33	GND	34	GND	35	DDR2_D10	36	DDR2_D14
37	DDR2_D11	38	DDR2_D15	39	GND	40	GND
41	GND	42	GND	43	DDR2_D16	44	DDR2_D20
45	DDR2_D17	46	DDR2_D21	47	GND	48	GND
49	DDR2_DQS2_N	50	NC	51	DDR2_DQS2_P	52	DDR2_DM2
53	GND	54	GND	55	DDR2_D18	56	DDR2_D22
57	DDR2_D19	58	DDR2_D23	59	GND	60	GND
61	DDR2_D24	62	DDR2_D28	63	DDR2_D25	64	DDR2_D29
65	GND	66	GND	67	DDR2_DM3	68	DDR2_DQS3_N
69	NC	70	DDR2_DQS3_P	71	GND	72	GND
73	DDR2_D26	74	DDR2_D30	75	DDR2_D27	76	DDR2_D31
77	GND	78	GND	79	DDR2_CKE0	80	DDR2_CKE0
81	1.8V	82	1.8V	83	NC	84	NC
85	DDR2_BA2	86	NC	87	1.8V	88	1.8V
89	DDR2_A12	90	DDR2_A11	91	DDR2_A9	92	DDR2_A7
93	DDR2_A8	94	DDR2_A6	95	1.8V	96	1.8V
97	DDR2_A5	98	DDR2_A4	99	DDR2_A3	100	DDR2_A2
101	DDR2_A1	102	DDR2_A0	103	1.8V	104	1.8V
105	DDR2_A10	106	DDR2_BA1	107	DDR2_BA0	108	DDR2_RAS_B
109	DDR2_WE_B	110	DDR2_CS0_B	111	1.8V	112	1.8V
113	DDR2_CAS_B	114	DDR2_ODT0	115	DDR2_CS1_B	116	DDR2_A13
117	1.8V	118	1.8V	119	DDR2_ODT1	120	NC
121	GND	122	GND	123	DDR2_D32	124	DDR2_D36
125	DDR2_D33	126	DDR2_D37	127	GND	128	GND
129	DDR2_DQS4_N	130	DDR2_DDM4	131	DDR2_DQS4_P	132	GND
133	GND	134	DDR2_D38	135	DDR2_D34	136	DDR2_D30
137	DDR2_D35	138	GND	139	GND	140	DDR2_D44
141	DDR2_D40	142	DDR2_D44	143	DDR2_D41	144	GND
145	GND	146	DDR2_DQS5_N	147	DDR2_DM5	148	DDR2_DQS5_P
149	GND	150	GND	151	DDR2_D42	152	DDR2_D46
153	DDR2_D43	154	DDR2_D47	155	GND	156	GND
157	DDR2_D48	158	DDR2_D52	159	DDR2_D49	160	DDR2_D53
161	GND	162	GND	163	NC	164	DDR2_CK1_P
165	GND	166	DDR2_CK1_N	167	DDR2_DQ56_N	168	GND
169	DDR2_DQ56_P	170	DDR2_DM6	171	GND	172	GND
173	DDR2_D50	174	DDR2_D54	175	DDR2_D51	176	DDR2_D55
177	GND	178	GND	179	DDR2_D56	180	DDR2_D60
181	DDR2_D57	182	DDR2_D61	183	GND	184	GND
185	DDR2_DM7	186	DDR2_DQS7_N	187	GND	188	DDR2_DQS7_P
189	DDR2_D58	190	GND	191	DDR2_D59	192	DDR2_D62
193	GND	194	DDR2_D63	195	DDR2_SDA	196	GND
197	DDR2_SDL	198	GND	199	1.8V	200	GND

3.9 J16, J17 EXP Connectors

J16 and J17 provide connections to APPSFPGA compatible with the Avnet EXP Bus Specification. J16 and J17 may also be used as high speed interface connectors for accessory boards. The D4100 controller board routes some of the single-ended signals as differential pairs to support a full 64 bit LVDS data bus. This routing may interfere with the EXP single-ended signals as noted in the Table 3-9 and Table 3-11 tablenotes.

Table 3-9. J16 EXP-1 Connector

J16 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number	J16 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number
1	EXP1_SE_IO_1		A33	2	EXP1_SE_IO_0		C34
3	EXP1_SE_IO_3		B32	4	EXP1_SE_IO_2		D32
7	EXP1_SE_IO_5		B33	8	EXP1_SE_IO_4		D34
9	EXP1_SE_IO_7		C32	10	EXP1_SE_IO_6		E34
13	EXP1_SE_IO_9		H32	14	EXP1_SE_IO_8		G32
15	EXP1_SE_IO_11		C33	16	EXP1_SE_IO_10		F33
19	EXP1_SE_IO_13(1)	EXP1_DIFF_23_P	K33	20	EXP1_SE_IO_12(1)	EXP1_DIFF_22	G33
21	EXP1_SE_IO_15(1)	EXP1_DIFF_23_N	K32	22	EXP1_SE_IO_14(1)	EXP1_DIFF_22	F34
25	EXP1_SE_IO_17(1)	EXP1_DIFF_25_P	P34	26	EXP1_SE_IO_16(1)	EXP1_DIFF_24	H34
27	EXP1_SE_IO_19(1)	EXP1_DIFF_25_N	N34	28	EXP1_SE_IO_18(1)	EXP1_DIFF_24	J34
31	EXP1_SE_IO_21(1)	EXP1_DIFF_27_P	N33	32	EXP1_SE_IO_20(1)	EXP1_DIFF_26	L34
33	EXP1_SE_IO_23(1)	EXP1_DIFF_27_N	M33	34	EXP1_SE_IO_22(1)	EXP1_DIFF_26	K34
37	EXP1_SE_IO_25(1)	EXP1_DIFF_29_P	L33	38	EXP1_SE_IO_24(1)	EXP1_DIFF_28	J32
39	EXP1_SE_IO_27(1)	EXP1_DIFF_29_N	M32	40	EXP1_SE_IO_26(1)	EXP1_DIFF_28	H33
41	EXP1_SE_IO_28		E32	42		EXP1_DIFF_CLK_IN_DPP	H19
43	EXP1_SE_CLK_IN		J20	44		EXP1_DIFF_CLK_IN_DPN	H20
47	EXP1_SE_IO_29		E33	48	EXP1_SE_IO_30(1)	EXP1_DIFF_30_P	R33
49	EXP1_SE_CLK_OUT		J21	50	EXP1_SE_IO_3(1)	EXP1_DIFF_30_N	R32
53		EXP1_DIFF_21_P	P32	54		EXP1_DIFF_20_P	AC32
55		EXP1_DIFF_21_N	N32	56		EXP1_DIFF_20_N	AB32
59	EXP1_SE_IO_32(1)	EXP1_DIFF_31_P	T33	60		EXP1_DIFF_18_P	AF34
61	EXP1_SE_IO_33(1)	EXP1_DIFF_31_N	R34	62		EXP1_DIFF_18_N	AE34
65		EXP1_DIFF_19_P	AG32	66		EXP1_DIFF_16_P	U33
67		EXP1_DIFF_19_N	AH32	68		EXP1_DIFF_16_N	T34
71		EXP1_DIFF_17_P	AJ32	72		EXP1_DIFF_CLK_OUT_P	U3
73		EXP1_DIFF_17_N	AK32	74		EXP1_DIFF_CLK_OUT_N	U2
77		EXP1_DIFF_15_P	W34	78		EXP1_DIFF_14_P	V33
79		EXP1_DIFF_15_N	V34	80		EXP1_DIFF_14_N	V32
81		EXP1_DIFF_13_P	AA34	82		EXP1_DIFF_12_P	AD32
83		EXP1_DIFF_13_N	Y34	84		EXP1_DIFF_12_N	AE32
87		EXP1_DIFF_11_P	Y32	88		EXP1_DIFF_10_P	AL34
89		EXP1_DIFF_11_N	W32	90		EXP1_DIFF_10_N	AL33
93		EXP1_DIFF_9_P	AA33	94		EXP1_DIFF_8_P	AK34
95		EXP1_DIFF_9_N	Y33	96		EXP1_DIFF_8_N	AK33
99		EXP1_DIFF_7_P	AC33	100		EXP1_DIFF_6_P	AF33
101		EXP1_DIFF_7_N	AB33	102		EXP1_DIFF_6_N	AE33
105		EXP1_DIFF_5_P	AC34	106		EXP1_DIFF_4_P	AH34
107		EXP1_DIFF_5_N	AD34	108		EXP1_DIFF_4_N	AJ34
111		EXP1_DIFF_3_P	AM33	112		EXP1_DIFF_2_P	AG33
113		EXP1_DIFF_3_N	AM32	114		EXP1_DIFF_2_N	AH33
117		EXP1_DIFF_1_P	AN34	118		EXP1_DIFF_0_P	AN32
119		EXP1_DIFF_1_N	AN33	120		EXP1_DIFF_0_N	AP32

(1) Single ended /IO with shared differential pairs, should only be slow switching signals or only one side of the pair should be used.

Table 3-10. J16 EXP-1 Power and Ground Connections

J16 Pin Number	Power Connection
5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36	VCC_2P5V
45, 46, 41, 52, 57, 58, 63, 64, 69, 70, 75, 76, 121, 122, 124, 125, 126, 127, 128, 129, 130, 131, 132	Ground
85, 86, 91, 92, 97, 98, 103, 104, 109, 110, 115, 116	VCC_3P3V

Table 3-11. J17 EXP-2 Connector

J17 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number	J17 Pin Number	Single Ended Signal Name	Differential Pair Name	APPSFPGA Pin Number
1	EXP2_SE_IO_1		D1	2	EXP2_SE_IO_0		B3
3	EXP2_SE_IO_3		D2	4	EXP2_SE_IO_2		B1
7	EXP2_SE_IO_5		J2	8	EXP2_SE_IO_4		B2
9	EXP2_SE_IO_7		J1	10	EXP2_SE_IO_6		A3
13	EXP9_SE_IO_9		K1	14	EXP2_SE_IO_8		C2
15	EXP2_SE_IO_11		K2	16	EXP2_SE_IO_10		C3
19	EXP2_SE_IO_13(1)	EXP2_DIFF_23_P	H2	20	EXP2_SE_IO_12(1)	EXP2_DIFF_22	E2
21	EXP2_SE_IO_15(1)	EXP2_DIFF_23_N	H3	22	EXP2_SE_IO_14(1)	EXP2_DIFF_22	E1
25	EXP2_SE_IO_17(1)	EXP2_DIFF_25_P	P2	26	EXP2_SE_IO_16(1)	EXP2_DIFF_24	E3
27	EXP2_SE_IO_19(1)	EXP2_DIFF_25_N	R3	28	EXP2_SE_IO_18(1)	EXP2_DIFF_24	F3
31	EXP2_SE_IO_21(1)	EXP2_DIFF_27_P	T1	32	EXP2_SE_IO_20(1)	EXP2_DIFF_26	F1
33	EXP2_SE_IO_23(1)	EXP2_DIFF_27_N	R1	34	EXP2_SE_IO_22(1)	EXP2_DIFF_26	G1
37	EXP2_SE_IO_25(1)	EXP2_DIFF_29_P	K3	38	EXP2_SE_IO_24(1)	EXP2_DIFF_28	G3
39	EXP2_SE_IO_27(1)	EXP2_DIFF_29_N	L3	40	EXP2_SE_IO_26(1)	EXP2_DIFF_28	G2
41	EXP2_SE_IO_28		Y2	42		EXP2_DIFF_CLK_IN_DPP	H18
43	EXP2_SE_CLK_IN		J16	44		EXP2_DIFF_CLK_IN_DPN	J17
47	EXP2_SE_IO_29		Y3	48	EXP2_SE_IO_30(1)	EXP2_DIFF_30_P	N2
49	EXP2_SE_CLK_OUT		J15	50	EXP2_SE_IO_31	EXP2_DIFF_30_N	M2
53		EXP2_DIFF_21_P	M3	54		EXP2_DIFF_20_P	M1
55		EXP2_DIFF_21_N	N3	56		EXP2_DIFF_20_N	L1
59	EXP2_SE_IO_32(1)	EXP2_DIFF_31_P	P1	60		EXP2_DIFF_18_P	V4
61	EXP2_SE_IO_33(1)	EXP2_DIFF_31_N	R2	62		EXP2_DIFF_18_N	V3
65		EXP2_DIFF_19_P	U3	66		EXP2_DIFF_16_P	W1
67		EXP2_DIFF_19_N	T3	68		EXP2_DIFF_16_N	V2
71		EXP2_DIFF_17_P	U1	72		EXP2_DIFF_CLK_OUT_P	AC3
73		EXP2_DIFF_17_N	U2	74		EXP2_DIFF_CLK_OUT_N	AB2
77		EXP2_DIFF_15_P	W2	78		EXP2_DIFF_14_P	AB3
79		EXP2_DIFF_15_N	Y1	80		EXP2_DIFF_14_N	AA3
81		EXP2_DIFF_13_P	AF1	82		EXP2_DIFF_12_P	AG1
83		EXP2_DIFF_13_N	AE1	84		EXP2_DIFF_12_N	AG2
87		EXP2_DIFF_11_P	AF3	88		EXP2_DIFF_10_P	AE2
89		EXP2_DIFF_11_N	AE3	90		EXP2_DIFF_10_N	AD2
93		EXP2_DIFF_9_P	AH2	94		EXP2_DIFF_8_P	AB1
95		EXP2_DIFF_9_N	AJ2	96		EXP2_DIFF_8_N	AA1
99		EXP2_DIFF_7_P	AK2	100		EXP2_DIFF_6_P	AG3
101		EXP2_DIFF_7_N	AK3	102		EXP2_DIFF_6_N	AH3
105		EXP2_DIFF_5_P	AJ1	106		EXP2_DIFF_4_P	AC2
107		EXP2_DIFF_5_N	AK1	108		EXP2_DIFF_4_N	AD1
111		EXP2_DIFF_3_P	AM3	112		EXP2_DIFF_2_P	AN2
113		EXP2_DIFF_3_N	AN3	114		EXP2_DIFF_2_N	AP2
117		EXP2_DIFF_1_P	AL1	118		EXP2_DIFF_0_P	AM2
119		EXP2_DIFF_1_N	AM1	120		EXP2_DIFF_0_N	AL3

(1) Single ended /IO with shared differential pairs, should only be slow switching signals or only one side of the pair should be used.

Table 3-12. J17 EXP-2 Power and Ground Connections

J17 Pin Number	Power Connection
5, 6, 11, 12, 17, 18, 23, 24, 29, 30, 35, 36	VCC_2P5V
45, 46, 41, 52, 57, 58, 63, 64, 69, 70, 75, 76, 121, 122, 124, 125, 126, 127, 128, 129, 130, 131 ,132	Ground
85, 86, 91, 92, 97, 98, 103, 104, 109, 110, 115, 116	VCC_3P3V

3.10 H1 Xilinx FPGA JTAG Header

Provides direct connection for a Xilinx JTAG programming cable. Xilinx Model DLC9G is recommended. Visit www.xilinx.com for more information.

Table 3-13. H1 Xilinx APPSFPGA JTAG Header

H1 Pin Number	Pin Name
1, 3, 5, 7, 9, 11, 13	GND
2	P2P5V
4	TMS
6	TCK
8	TDO
10	TDI
12, 14	NC

Configuration Jumpers

This section describes the D4100 Controller Board configuration jumpers. Figure 4-1 shows jumper locations on the D4100 controller board.

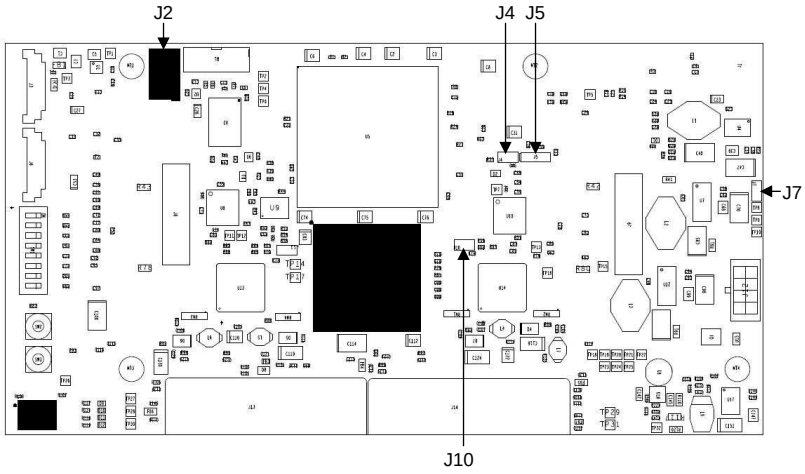

Figure 4-1. D4100 Controller Configuration Jumpers

4.1 J2 – EXP Voltage Select

J2 – Used to select either 2.5-V or 3.3-V voltage supplies for the EXP bus FPGA banks. This setting should match the I/O voltage required by any board attached to the EXP connectors.

Table 4-1. EXP Voltage Select

Position	Bank Voltage
1-2	3.3 V
2-3	2.5 V

4.2 J4 – APPSFPGA Revision Select

J4 – Used to select the revision of firmware loaded from the PROM to the APPSFPGA.

Table 4-2. APPSFPGA Revision Select

Jumper Position	Revision Version
0-1	0
1-2	1

4.3 J5 – Shared USB Signal Enable/Disable

J5 – Used to connect or disconnect the USB signals that are shared between the USB/APPSFPGA Mictor Connector J10. This could be useful to isolate test signals from the FPGA to the Mictor connector.

Table 4-3. Shared USB Signal Enable/Disable

Jumper Position	USB Signals
0-1	Disconnected from FPGA
1-2	Connected to FPGA
2-3	Automatically connect USB signals to FPGA when USB is connected to host PC

4.4 J10 – DLPA200 B Output Enable

J10 – Used to enable the outputs for DLPA200 B. This needs to be enabled only if using the 1080p DMD, otherwise this can be disabled.

Table 4-4. DLPA200 B Output Enable

Jumper Position	DLPA200 B Outputs
0-1	Disabled
1-2	Enabled

4.5 J7 – USB EEPROM Programming Header

J7 – Used to temporally disconnect the USB EEPROM from the device so the device can load its internal boot loader rather than any code in the EEPROM. Install J8 for Cypress internal boot loader.

Switches

This section defines the function of the D4100 switches.

5.1 Dip Switches – SW1

Functionality defined by APPSFPGA programming. In default test pattern code:

Table 5-1. Dip Switch Assignments

Switch Number	Effect
1	ON = float – float all mirrors
2	ON = counter halt – stop counter, this will freeze the image on the DMD
3	ON = complement data – causes DLPC410 to complement all data it receives
4	ON = north/south flip – causes the DLPC410 to reverse order of row loading, effectively flipping the image
6 and 5	Dictates the type of reset being used (where switch 6 is the MSB and ON = 1): • 00 : single block phased reset • 01 : dual block phased reset • 10 : global reset • 11 : quad block phased reset
7	ON = Row Address Mode
8	ON = WDT Enable, disables other resets

5.2 Push Button Momentary Switch – SW2

Functionality defined by APPSFPGA. This switch is used to reset the APPSFPGA logic in the default code.

5.3 Push Button Momentary Switch – SW3

Functionality defined by APPSFPGA. This switch is used for PWR_FLOAT in the default code.

5.4 Slide Switch – SW4

Power switch. This switch interrupts the 5-V input from the Power Connector J12.

Power and Status LEDs

This chapter provides an illustration of indicators used to verify that the D4100 Controller Board is functioning properly. Figure 6-1 shows the controller board indicator locations.

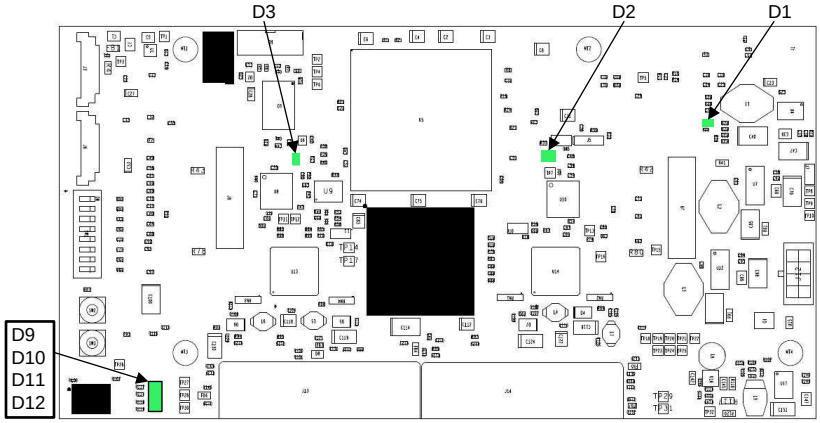

Figure 6-1. D4100 Controller Board Indicators

6.1 D1 – USB Connection Indicator

This LED illuminates when the USB port is successfully connected to a PC.

6.2 D2 – APPSFPGA Done

D2 is a two color LED, red and green.

The red side is turned on when the APPSFPGA DONE pin is low, [not DONE]. Red turns off when the DONE pin goes high indicating the APPSFPGA completed programming successfully. To further assure the APPSFPGA is up and running, the green LED is turned on by internal logic once all pins are turned on. This logic is to be defined by the application, although it could be a DCM lock monitor or a 'heart beat' indicating clocks are operating. The default load drives this with a simple high to turn the green LED on.

6.3 D3 – DDC4100 Done

D3 is a two color LED, red and green.

The red side is turned on when the DDC4100 DONE pin is low [not DONE]. Red turns off when the DONE pin goes high indicating the DLPC410 completed programming successfully. Green turns on when I/O pins are enabled after programming.

6.4 D9 – DDC_LED0

D9 – DDC_LED0: Status LED for the DLPC410. See the DLPC410 data sheet for more details.

6.5 D10 – DDC_LED1

D10 – DDC_LED1: Status LED for the DLPC410. See the DLPC410 data sheet for more details.

6.6 D11 – VLED0

D11 – VLED0: This logic is to be defined by the APPSFPGA application. Drive low to turn on the LED. Drive high to turn off the LED.

6.7 D12 – VLED1

D12 – VLED1: This logic is to be defined by the APPSFPGA application. Drive low to turn on the LED. Drive high to turn off the LED.

Test Points

This chapter defines the location of on-board test points shown in Figure 7-1. Table 7-1 lists these test points.

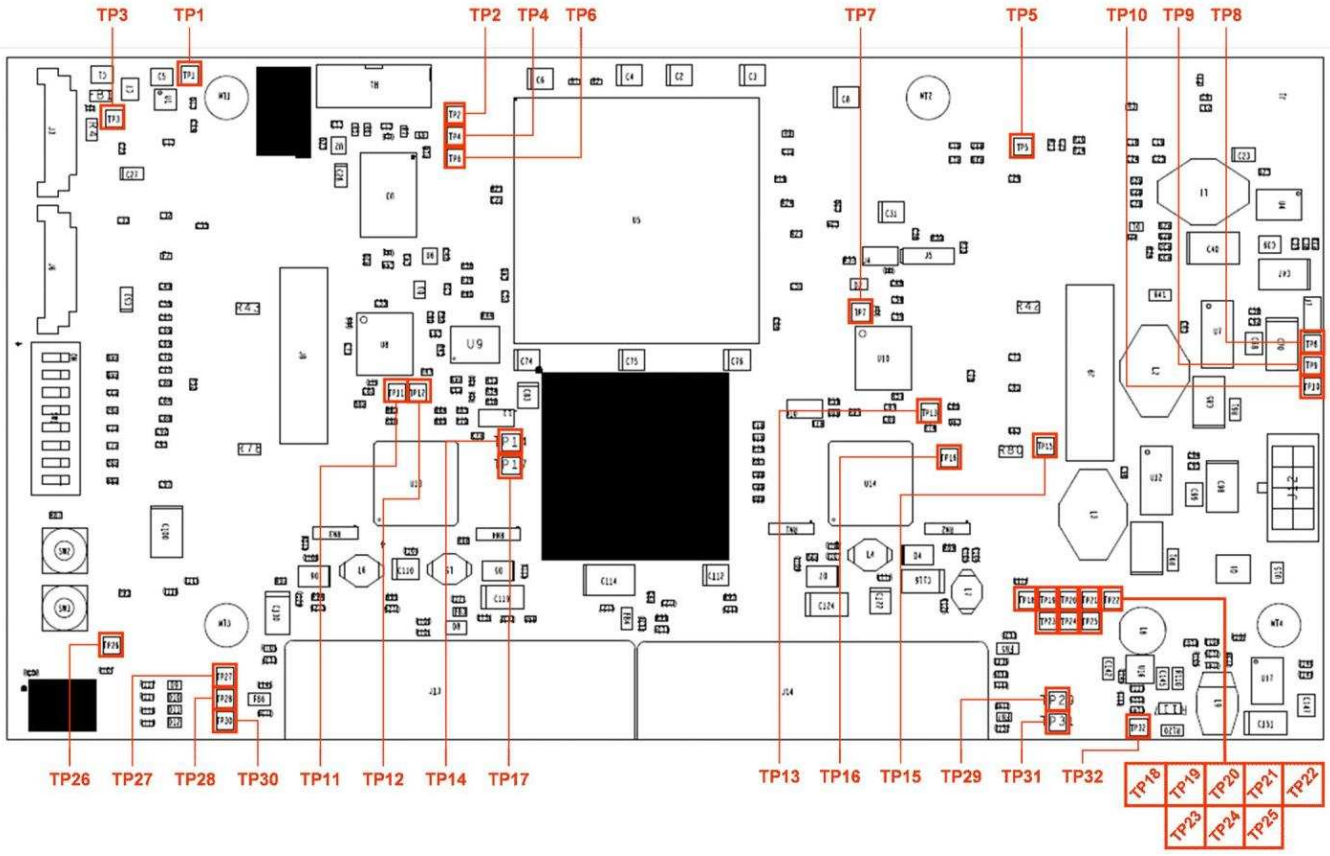

Figure 7-1. Test Point Locations

Table 7-1. Test Points

Test Point	Net Name	Test Point	Net Name
TP1	GROUND	TP2	V5_DXP
TP3	VCC_VREF	TP4	V5_DXN
TP5	GROUND	TP6	RESET
TP7	SCPDO	TP8	BKPT
TP9	VCC_3P3V	TP10	VCC_2P5V
TP11	MBRST1_8	TP12	DAD_A_IRQZ
TP13	DAD_B_IRQZ	TP14	DXP_0
TP15	PWRGD	TP16	MBRST2_0
TP17	DXN_0	TP18	SCPDI
TP19	DMDSPARE2	TP20	MBRST2_8
TP21	VCC_12V	TP22	GROUND
TP23	DMDSPARE3	TP24	GROUND
TP25	VCC_1P8V	TP26	POWER_STANDBY#
TP27	DMDSPARE0	TP28	MBRST1_0
TP29	VCC_1P0V_DDC	TP30	DMDSPARE0
TP31	SCPCLK	TP32	VCC_1P0V

Documentation

This section lists related documents associated with the use of the DLPC410 Controller Board.

DLPC410 - Digital Controller for DLP Discovery 4100 chipset data sheet (DLPS024)

DLPA200 - DMD Micromirror Driver data sheet (DLPS015)

DLPR410 - PROM for DLP Discovery 4100 chipset data sheet (DLPS027)

D4100 Controller Board design files (DLPR018) - contains:

- D4100 Board ESD - electronic schematic
- D4100 Board GERBER & BRD files
- D4100 Board CCA - circuit card assembly
- D4100 Board BOM - circuit card assembly

DLP9500(UV) Board design files (DLPC096) - contains:

- DLP9500 Board ESD - electronic schematic
- DLP9500 Board GERBER & BRD files
- DLP9500 Board CCA - circuit card assembly
- DLP9500 Board BOM - circuit card assembly

DLP7000(UV) Board design files (DLPC095) - contains:

- DLP7000 Board ESD - electronic schematic
- DLP7000 Board GERBER & BRD files
- DLP7000 Board CCA - circuit card assembly
- DLP7000 Board BOM - circuit card assembly

www.xilinx.com APPSFPGA development tools and information

Appendix

A.1 Abbreviations and Acronyms

The following lists abbreviations and acronyms used in this manual.

APPSFPGA— Xilinx Virtex 5 Field Programmable Gate Array for customer applications

BPPS— Binary Patterns per Second

D4100— DLP Discovery 4100

DC— Direct Current

DDR— Double Data Rate

DMD— Digital Micromirror Device

DMA— Direct Memory Access

DRAM— Dynamic Random Access Memory

DRC— DAD Reset Controller

FCC— Federal Communications Commission

FPGA— Field Programmable Gate Array

PROM— Programmable Read Only Memory

SCP— Serial Communications Port

SRAM— Static Random Access Memory

USB— Universal Serial Bus

A.2 Notational Conventions

This document uses the following conventions.

The DLP Discovery 4100 Controller Board is also referred to as Controller Board.

A.2.1 Information About Cautions and Warnings

This book may contain cautions and warnings.

CAUTION

This is a description of a caution statement: A caution statement describes a situation that could potentially damage your software or equipment.

WARNING

This is a description of a warning statement: A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning: This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his/her own expense will be required to take whatever measures may be required to correct this interference.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265