DRV8313 三个半 H 桥驱动器集成电路 (IC)

查询样品: **DRV8313**

特性

- 三个半-**H-**桥驱动器 **IC**
  - 驱动 **3** 相无刷直流 **(DC)** 电机
  - 独立半桥控制
  - 用于低侧电流感测的引脚
  - 低 **MOSFET** 导通电阻
- **24V**，**25°C** 下 **2.5A** 最大驱动器电流
- 通用比较器可被用于电流感测或其它功能
- 内置 **3.3V 10mA** 低压降 **(LDO)** 稳压器
- **8V** 至 **60V** 运行电源电压范围
- 耐热增强型表面贴装封装

应用范围

- **HVAC** 电机
- 消费类产品
- 办公自动化设备
- 工厂自动化
- 机器人

说明

DRV8313 提供三个可独立控制的半 H 桥驱动器。 虽然也可被用于驱动螺线管或其它负载，它主要用于驱动一个三相无刷直流电机。 每个输出驱动器通道包含采用半 H 桥配置的 N 通道功率 MOSFET。 这个设计将每个驱动器的接地端子接至引脚，以在每个输出上执行电流感测。

电流限制电路或其它功能可使用一个通用比较器。

DRV8313 在半 H 桥的每个通道上提供高达 2.5A 峰值电流或者 1.75A 均方根 (RMS) 输出电流（在 24V 和 25°C 时具有适当的印刷电路板 (PCB) 散热）。

此器件提供实现过流保护、短路保护、欠压闭锁和过温保护的内部关断功能。

DRV8313 采用 28 引脚散热薄型小外形尺寸 (HTSSOP) PowerPAD封装™ 封装。

ORDERING INFORMATION(1)

ORDERABLE PART NUMBER	PACKAGE(2)	TOPSIDE MARKING	SHIPPING
DRV8313PWPR	HTSSOP – PWP	DRV8313	Reel of 2000
DRV8313PWP			Tube of 50

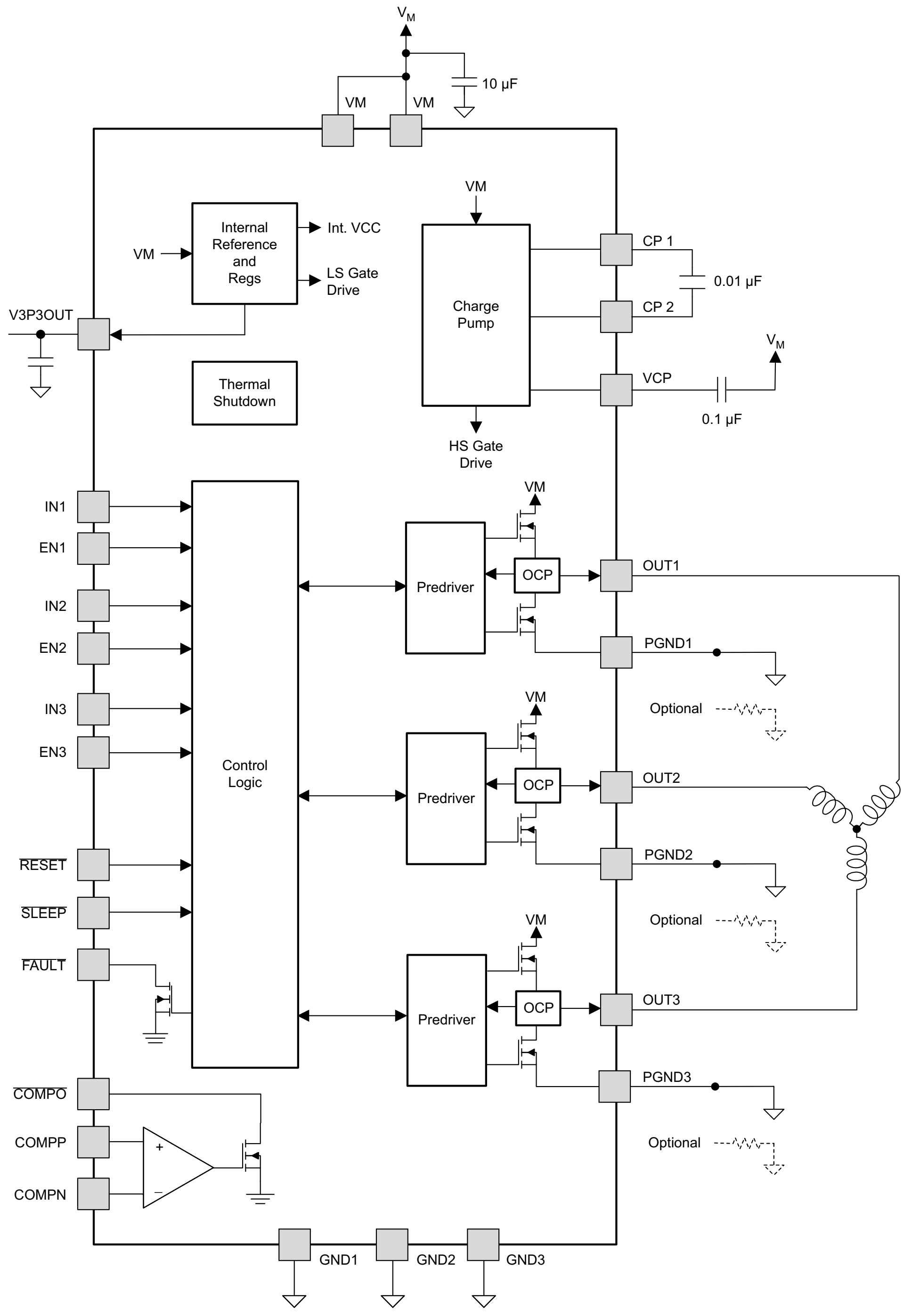
(1) For the most-current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.
(2) See package drawings, thermal data, and symbolization at www.ti.com/packaging.

English Data Sheet: SLVSBA5

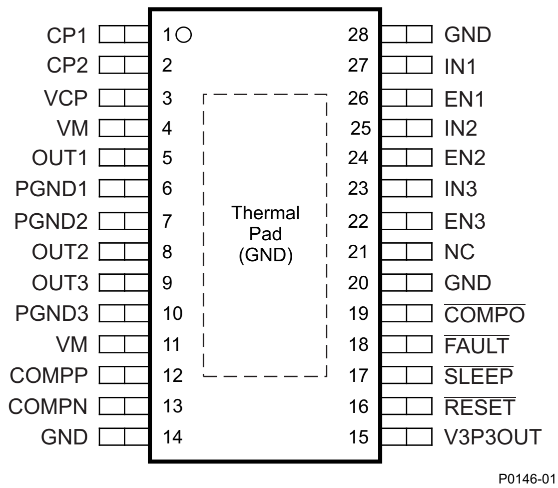
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



PWP Package
(Top View)



PIN DESCRIPTIONS

PIN		TYPE	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
Power and Ground				
CP1	1	IO	Charge-pump flying capacitor	Connect a 0.01-μF 100-V capacitor between CP1 and CP2.
CP2	2	IO	Charge-pump flying capacitor	
GND	12, 20, 28, PPAD	–	Device ground	Connect to system ground
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-μF 6.3-V ceramic capacitor. Use for suppling external loads is permissible.
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-μF 16-V ceramic capacitor to VM.
VM	4, 11	–	Main power supply	Connect to power supply (8.2 V–60 V). Connect both pins to the same supply. Bypass to GND with a 10-μF (minimum) capacitor.
Control				
EN1	26	I	Channel 1 enable	Logic high enables OUT1. Internal pulldown
EN2	24	I	Channel 2 enable	Logic high enables OUT2. Internal pulldown
EN3	22	I	Channel 3 enable	Logic high enables OUT3. Internal pulldown
IN1	27	I	Channel 1 input	Logic input controls state of OUT1. Internal pulldown
IN2	25	I	Channel 2 input	Logic input controls state of OUT2. Internal pulldown
IN3	23	I	Channel 3 input	Logic input controls state of OUT3. Internal pulldown
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the outputs. Internal pulldown
nSLEEP	17	I	Sleep-mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown
Status				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent, UVLO)
Comparator				
COMPN	13	I	Comparator negative input	Negative input of comparator
COMPP	12	I	Comparator positive input	Positive input of comparator
nCOMPO	19	OD	Comparator out	Output of comparator. Open-drain output

PIN DESCRIPTIONS (continued)

PIN		TYPE	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
Output				
OUT1	5	O	Output 1	Connect to loads.
OUT2	8	O	Output 2	
OUT3	9	O	Output 3	
PGND1	6	–	Ground for OUT1	Connect to ground, or to low-side current-sense resistors.
PGND2	7	–	Ground for OUT2	
PGND3	10	–	Ground for OUT3	

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		VALUE	UNIT
	Power-supply voltage range (V_M)	–0.3 V to 65	V
	Digital-pin voltage range	–0.5 to 7	V
	Comparator input-voltage range	–0.5 to 7	V
	Peak motor-drive output current	Internally limited	A
	Pin voltage (GND1, GND2, GND3)	±600	mV
	Continuous motor-drive output current(3)	2.5	A
T_J	Operating virtual junction temperature range	–40 to 150	ºC
T_{stg}	Storage temperature range	–60 to 150	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Observe power dissipation and thermal limits.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8313	UNIT
		PWP	
		28 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(2)	31.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	15.9	°C/W
θ_{JB}	Junction-to-board thermal resistance(4)	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter(6)	5.5	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power-supply voltage range[(1)]	8		60	V
V_{GNDX}	GND1, GND2, GND3 pin voltage	–500	0	500	mV
I_{V3P3}	V3P3OUT load current	0		10	mA

(1) All V_M pins must be connected to the same supply voltage.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supplies						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		1	5	mA
I_{VMQ}	VM sleep-mode supply current	V_M = 24 V		500	800	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		6.3	8	V
V3P3OUT Regulator						
V_{3P3}	V3P3OUT voltage	I_{OUT} = 0 to 10 mA	3.1	3.3	3.52	V
Logic-Level Inputs						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2.2		5.25	V
V_{HYS}	Input hysteresis		50		600	mV
I_{IL}	Input low current	VIN = 0	–5		5	µA
I_{IH}	Input high current	VIN = 3.3 V			100	µA
R_{PD}	Pulldown resistance			100		kΩ
nFAULT and COMPO OutputS (Open-Drain Outputs)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
Comparator						
V_{CM}	Common-mode input-voltage range		0		5	V
V_{IO}	Input offset voltage		–7		7	mV
I_{IB}	Input bias current		–300		300	nA
t_R	Response time	100-mV step with 10-mV overdrive			2	µs
H-Bridge FETs						
$r_{ds(on)}$	High-side FET on-resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
$r_{ds(on)}$	Low-side FET on-resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
I_{OFF}	Off-state leakage current		–2		2	µA
t_{DEAD}	Output dead time			90		ns
Protection Circuits						
I_{OCP}	Overcurrent protection trip level		3			A
t_{OCP}	Overcurrent protection deglitch time			5		µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

SWITCHING CHARACTERISTICS(1)

T_A = 25°, V_M = 24 V, R_L = 20 Ω

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
1	t_1	Delay time, ENx high to OUTx high, INx = 1	130	330	ns
2	t_2	Delay time, ENx low to OUTx low, INx = 1	275	475	ns
3	t_3	Delay time, ENx high to OUTx low, INx = 0	100	300	ns
4	t_4	Delay time, ENx low to OUTx high, INx = 0	200	400	ns
5	t_5	Delay time, INx high to OUTx high	300	500	ns
6	t_6	Delay time, INx low to OUTx low	275	475	ns
7	t_r	Output rise time, resistive load to GND	30	150	ns
8	t_f	Output fall time, resistive load to GND	30	150	ns

(1) Not production tested

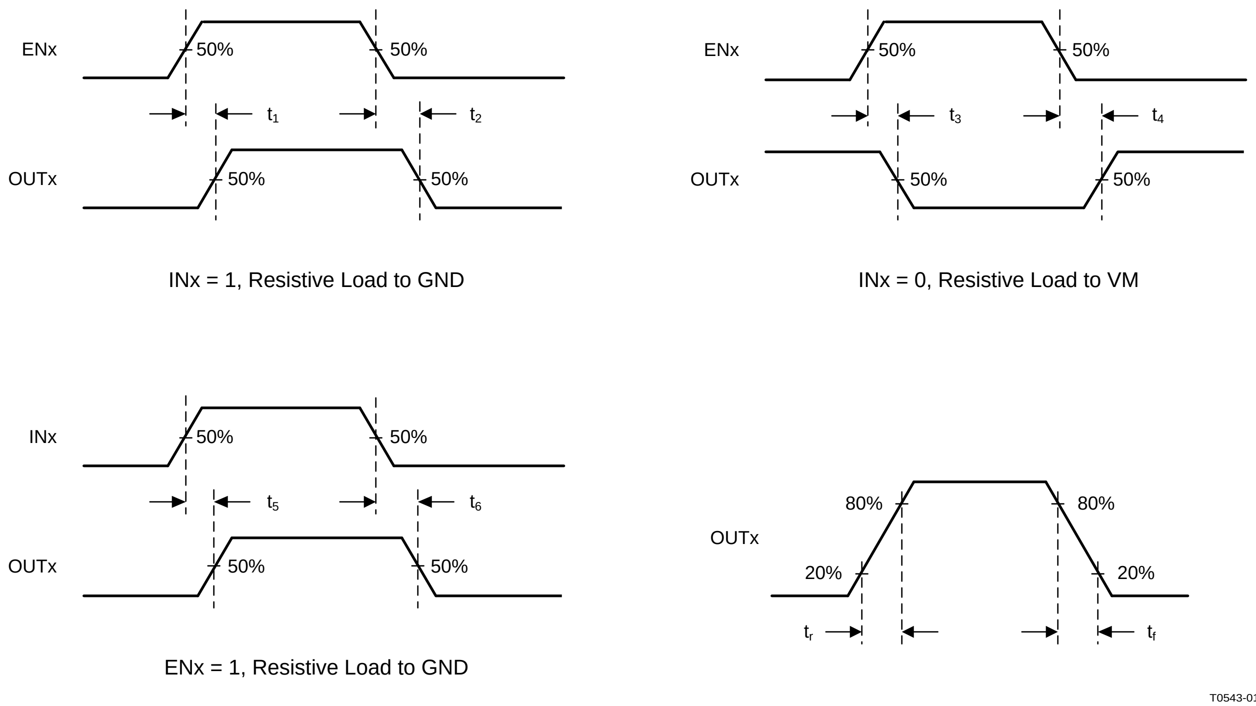


Figure 1. DRV8313 Switching Characteristics

FUNCTIONAL DESCRIPTION

Output Stage

The DRV8313 contains three half-H-bridge drivers. The source terminals of the low-side FETs of all three half-H-bridges terminate at separate pins (GND1, GND2, and GND3) to allow the use of a low-side current-sense resistor on each output, if desired. The user may also connect all three together to a single low-side sense resistor, or may connect them directly to ground if there is no need for current sensing.

If using a low-side sense resistor, take care to ensure that the voltage on the GND1, GND2, or GND3 pin does not exceed ±500 mV.

Note that there are multiple VM motor power-supply pins. Connect all VM pins together to the motor-supply voltage.

Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. The following table shows the logic:

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The DRV8313 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

The charge pump shuts down when nSLEEP is active-low.

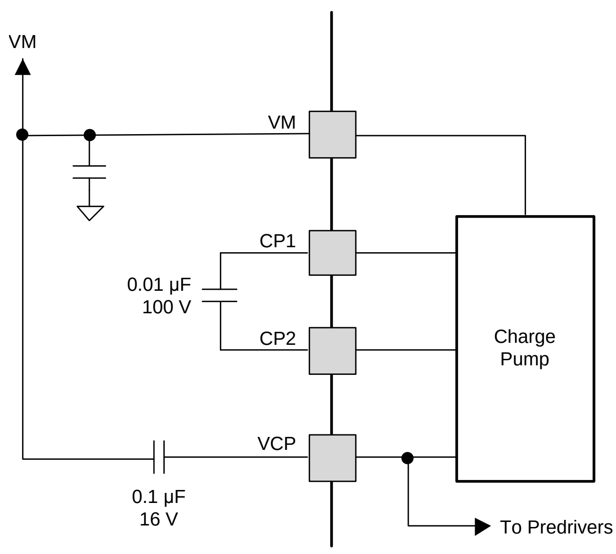


Figure 2. DRV8313 Charge Pump

Comparator

The DRV8313 includes an uncommitted comparator, which can find use as a current-limit comparator or for other purposes.

The following diagram shows connections to use the comparator to sense current for implementing a current limit. Current from all three low-side FETs is sensed using a single low-side sense resistor. The voltage across the sense resistor is compared with a reference, and when the sensed voltage exceeds the reference, a current-limit condition is signaled to the controller. The V3P3OUT internal voltage regulator can be used to set the reference voltage of the comparator.

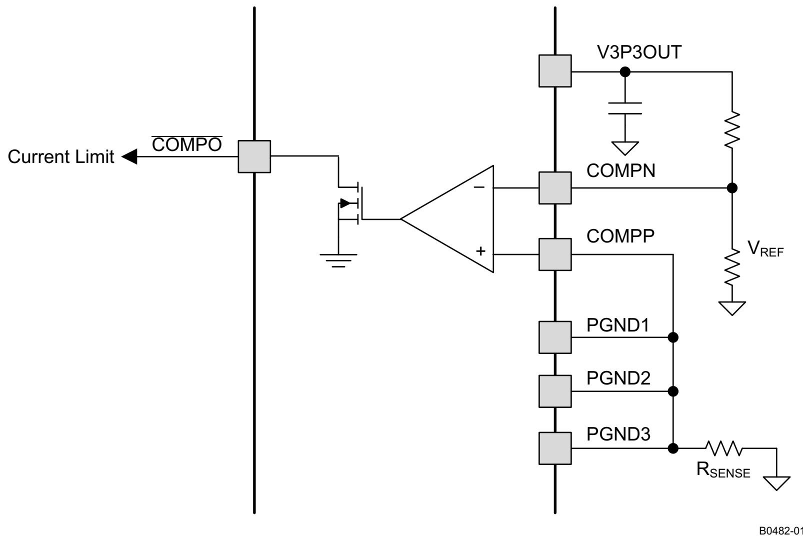


Figure 3. DRV8313 Comparator

nRESET and nSLEEP Operation

The nRESET pin, when driven active-low, resets any faults. It also disables the output drivers while it is active. The device ignores all inputs while nRESET is active. Note that there is an internal power-up-reset circuit, so that driving nRESET at power up is not required.

Driving nSLEEP low puts the device into a low-power sleep state. Entering this state disables the output drivers, stops the gate-drive charge pump, resets all internal logic (including faults), and stops all internal clocks. In this state, the device ignores all inputs until nSLEEP returns inactive-high. When returning from sleep mode, some time (approximately 1 ms) must pass before the motor driver becomes fully operational. Note that the V3P3 regulator remains operational in sleep mode.

Protection Circuits

The DRV8313 has full protection against undervoltage, overcurrent, and overtemperature events.

OVERCURRENT PROTECTION (OCP)

An analog current-limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP deglitch time, the device disables the channel experiencing the overcurrent and drives the nFAULT pin low. The driver remains off until either assertion of nRESET or the cycling of VM power.

Overcurrent conditions on both high- and low-side devices, that is, a short to ground, supply, or across the motor winding, all result in an overcurrent shutdown.

THERMAL SHUTDOWN (TSD)

If the die temperature exceeds safe limits, the device disables all outputs and drives the nFAULT pin low. Once the die temperature has fallen to a safe level, operation automatically resumes.

UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage-lockout threshold voltage, the device disables all outputs, resets internal logic, and drives the nFAULT pin low. Operation resumes when VM rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The DRV8313 has thermal shutdown (TSD) as previously described. A die temperature in excess of approximately 150°C disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

The power dissipated in the output FET resistance, or $r_{DS(on)}$ dominates power dissipation in the DRV8313. A rough estimate of average power dissipation of each half-H-bridge when running a static load is:

$$P = r_{DS(on)} \times (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one H-bridge, $r_{DS(on)}$ is the resistance of each FET, and I_{OUT} is equal to the average current drawn by the load. Note that at start-up and fault conditions, this current is much higher than normal running current; remember to take these peak currents and their duration into consideration.

The total device dissipation is the power dissipated in each of the three half-H-bridges added together.

The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking.

Note that $r_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when sizing the heatsink.

Heatsinking

The PowerPAD package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, add a number of vias to connect the thermal pad to the ground plane to accomplish this. On PCBs without internal planes, add copper area on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, use thermal vias to transfer the heat between the top and bottom layers.

For details about how to design the PCB, see TI Application Report SLMA002, *PowerPAD Thermally Enhanced Package* and TI Application Brief SLMA004, *PowerPAD Made Easy*, available at www.ti.com.

In general, providing more copper area allows the dissipation of more power.

APPLICATION INFORMATION

Output Configurations and Connections

The typical application for the DRV8313 is to drive a 3-phase brushless motor. In this application, the three outputs connect to the three motor leads, as shown in Figure 4.

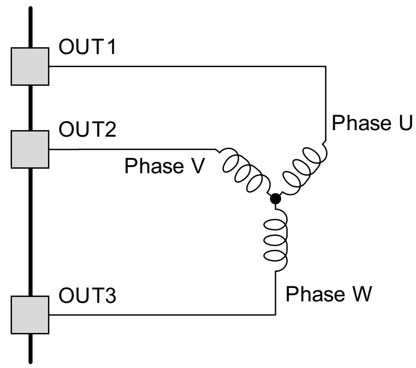


Figure 4. Three-Phase Motor Connection

The device achieves standard 120° (also called trapezoidal or block) commutation, using synchronous rectification, by following the states shown in Table 1

Table 1. Three-Phase Motor Signals

State	OUT1 (Phase U)			OUT2 (Phase V)			OUT3 (Phase W)		
	IN1	EN1	OUT1	IN2	EN2	OUT2	IN3	EN3	OUT3
1	X	0	Z	1 / PWM	1	H / PWM	0	1	L
2	1 / PWM	1	H / PWM	X	0	Z	0	1	L
3	1 / PWM	1	H / PWM	0	1	L	X	0	Z
4	X	0	Z	0	1	L	1 / PWM	1	H / PWM
5	0	1	L	X	0	Z	1 / PWM	1	H / PWM
6	0	1	L	1 / PWM	1	H / PWM	X	0	Z

On can implement asynchronous rectification by also applying the PWM signal to the enable inputs.

The DRV8313 can drive other loads, including dc brush motors and solenoids. For example, one could drive a dc brush motor in both directions, plus a single solenoid or unidirectional dc brush motor:

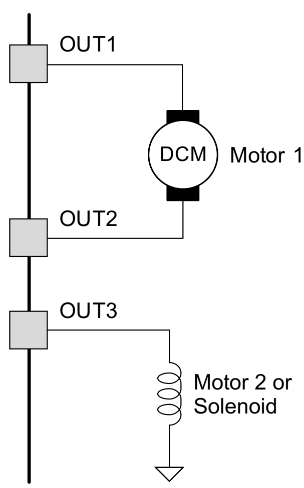


Figure 5. Bidirectional Motor Plus Motor or Solenoid Connection

The functions would be as shown in Table 2.

Table 2. Bidirectional Motor Plus Motor or Solenoid Signals

Motor 1							Motor 2 or Solenoid			
Function	IN1	EN1	OUT1	IN2	EN2	OUT2	Function	IN3	EN3	OUT3
Off or coast	X	0	Z	X	X	X	On	1 / PWM	1	1
Off or coast	X	X	X	X	0	X	Off or slow decay	0	1	0
Forward	1 / PWM	1	1	0	1	0	Off or coast	X	0	X
Reverse	0	1	0	1 / PWM	1	1				
Brake or slow decay	0	1	0	0	1	0				
Brake or slow decay	1	1	1	1	1	1				

Applying a PWM signal to the appropriate INx pin(s) as shown in Table 2 could implement PWM speed control.

Another possibility is controlling three different loads. Note that it is possible to return one side of the load either to the power supply (VM) or to ground.

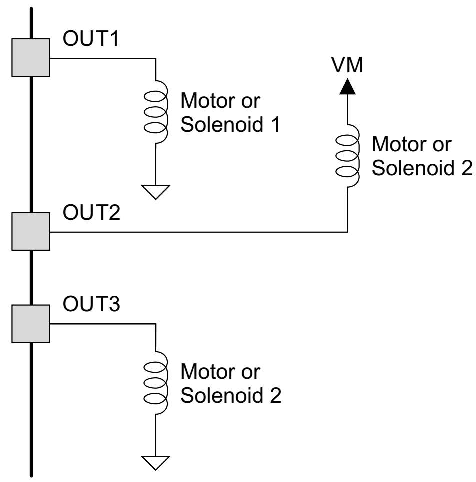


Figure 6. Three Independent Load Connections

Table 3. Three Independent Load Signals

Motor or Solenoid 1				Motor or Solenoid 2				Motor or Solenoid 3			
Function	IN1	EN1	OUT1	Function	IN2	EN2	OUT2	Function	IN3	EN3	OUT3
On	1 / PWM	1	1	On	1 / PWM	1	1	On	1 / PWM	1	1
Off or slow decay	0	1	0	Off or slow decay	0	1	0	Off or slow decay	0	1	0
Off or coast	X	0	X	Off or coast	X	0	X	Off or coast	X	0	X

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8313PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples
DRV8313PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples
DRV8313RHH	ACTIVE	VQFN	RHH	36	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples
DRV8313RHHR	ACTIVE	VQFN	RHH	36	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8313	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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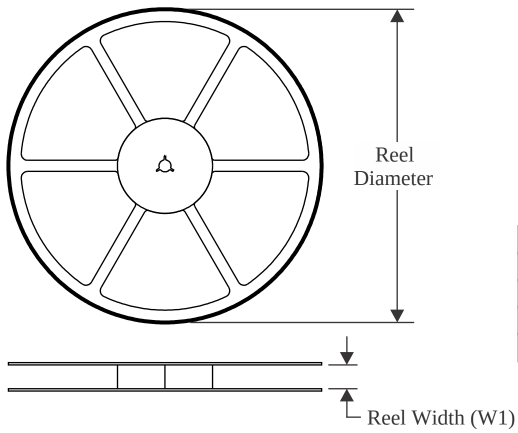
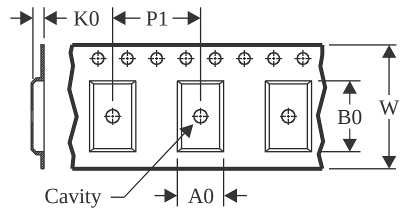
TAPE AND REEL INFORMATION

REEL DIMENSIONS

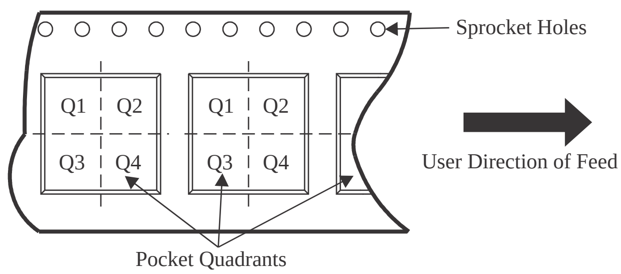


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

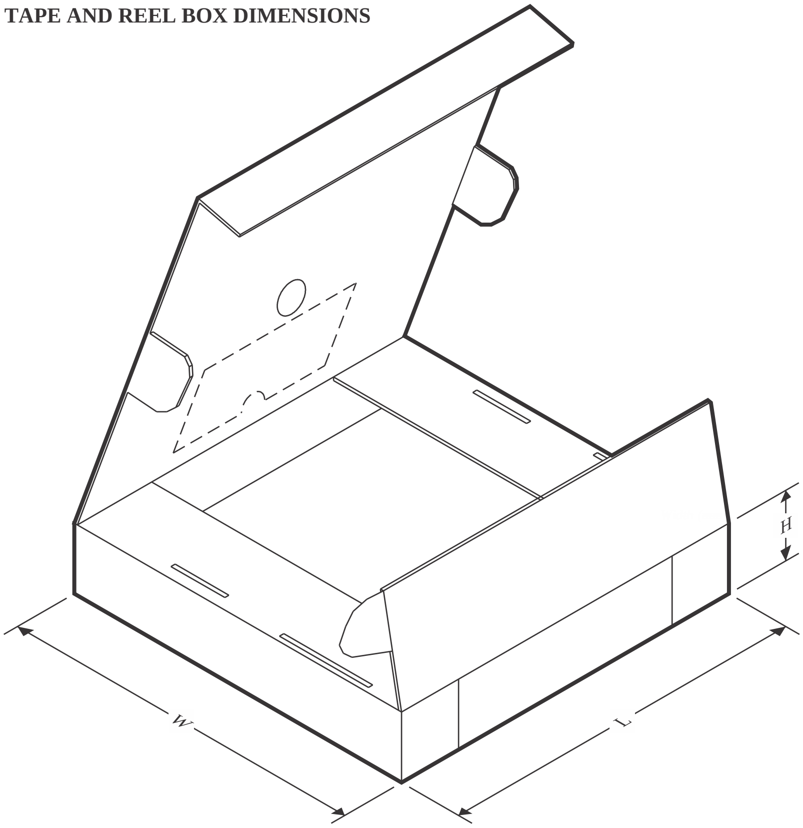
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8313PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
DRV8313RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

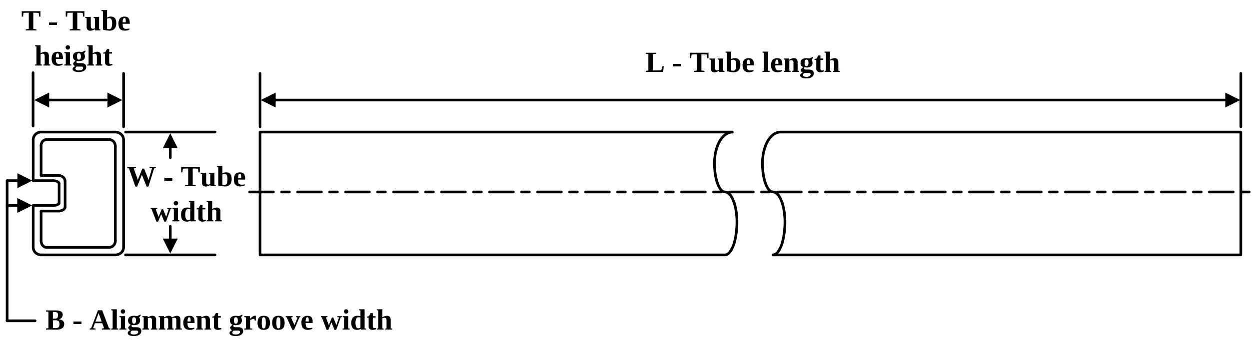
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8313PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
DRV8313RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8313PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5
DRV8313RHH	RHH	VQFN	36	60	381.5	7.92	2286	0

GENERIC PACKAGE VIEW

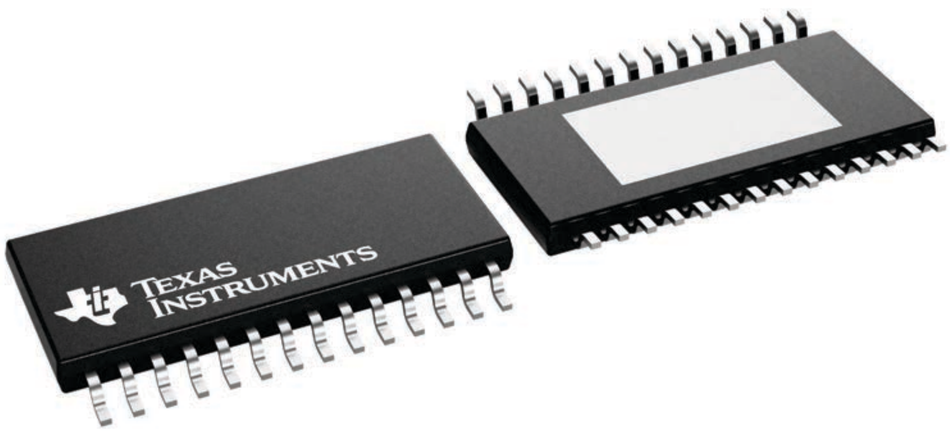
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

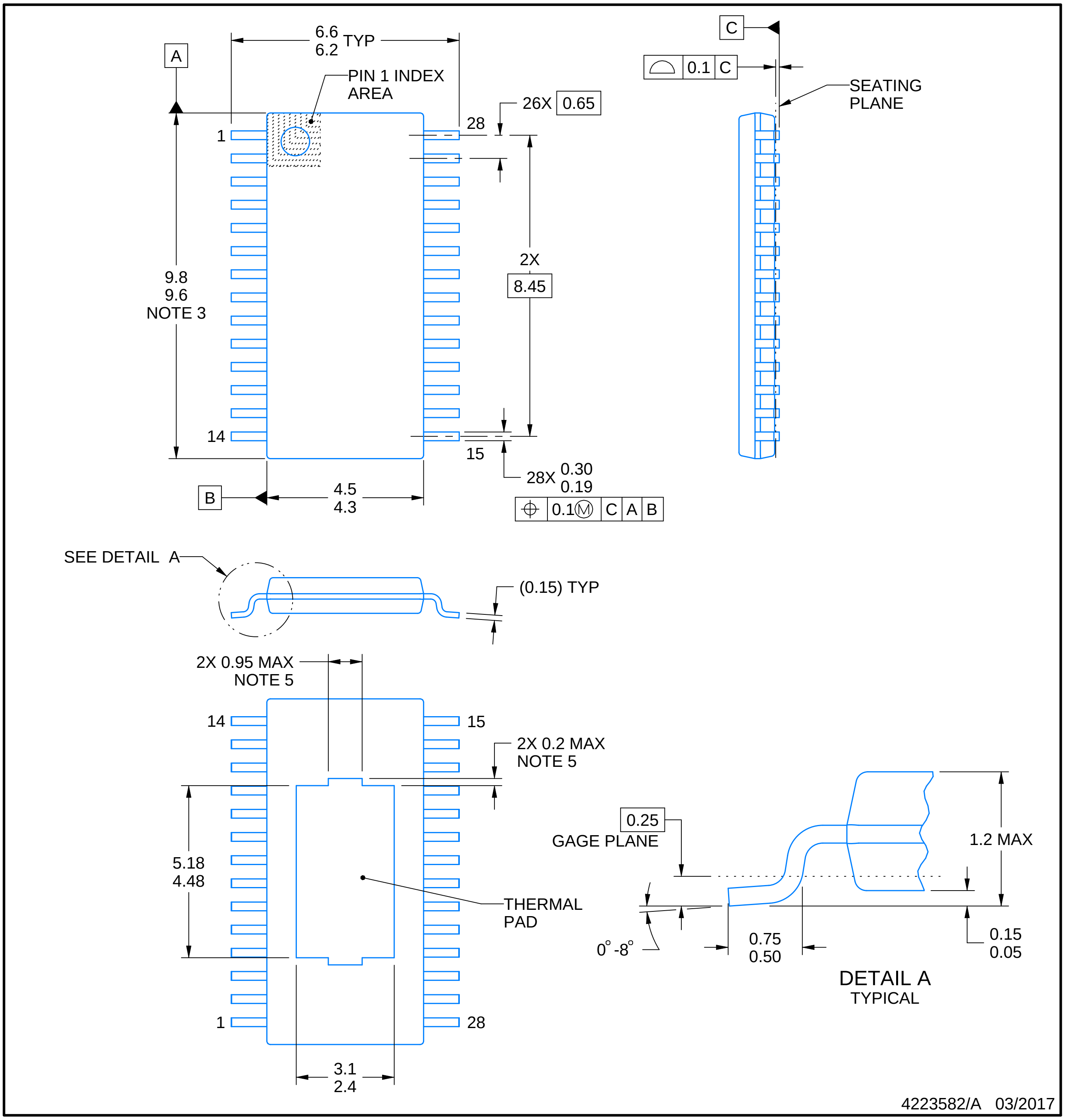
4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



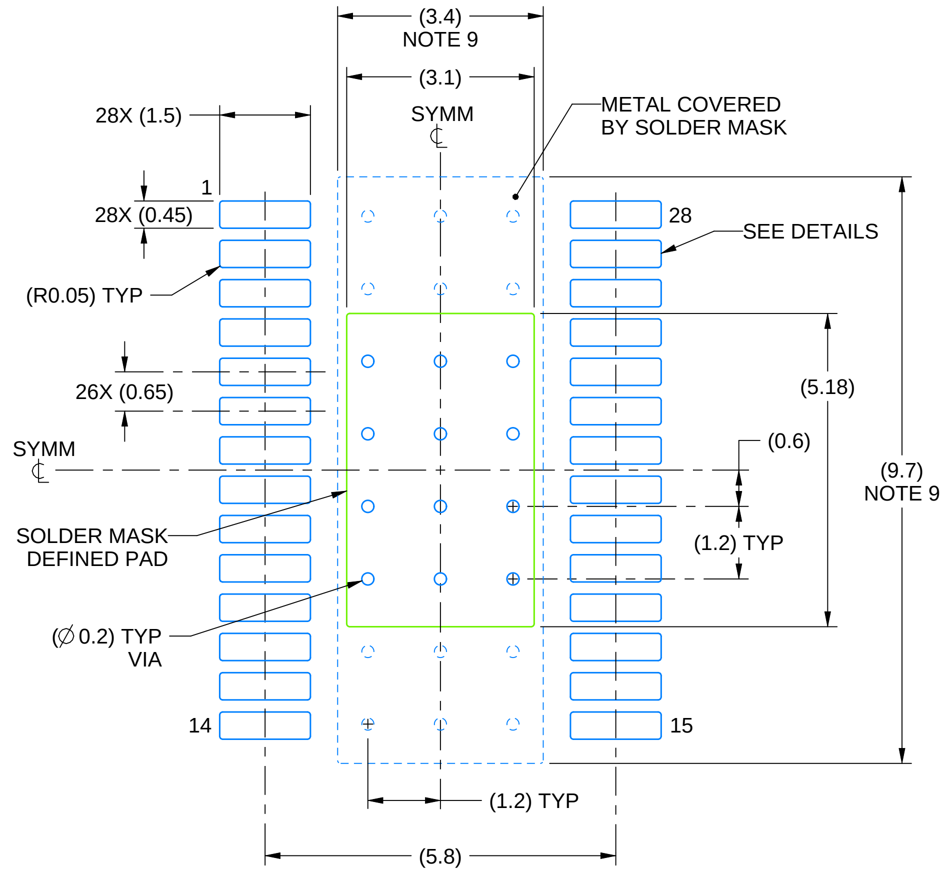
4224765/B



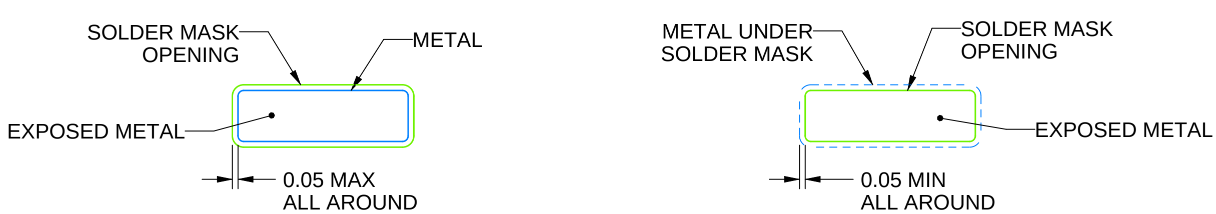
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



NON-SOLDER MASK
DEFINED
(PREFERRED)

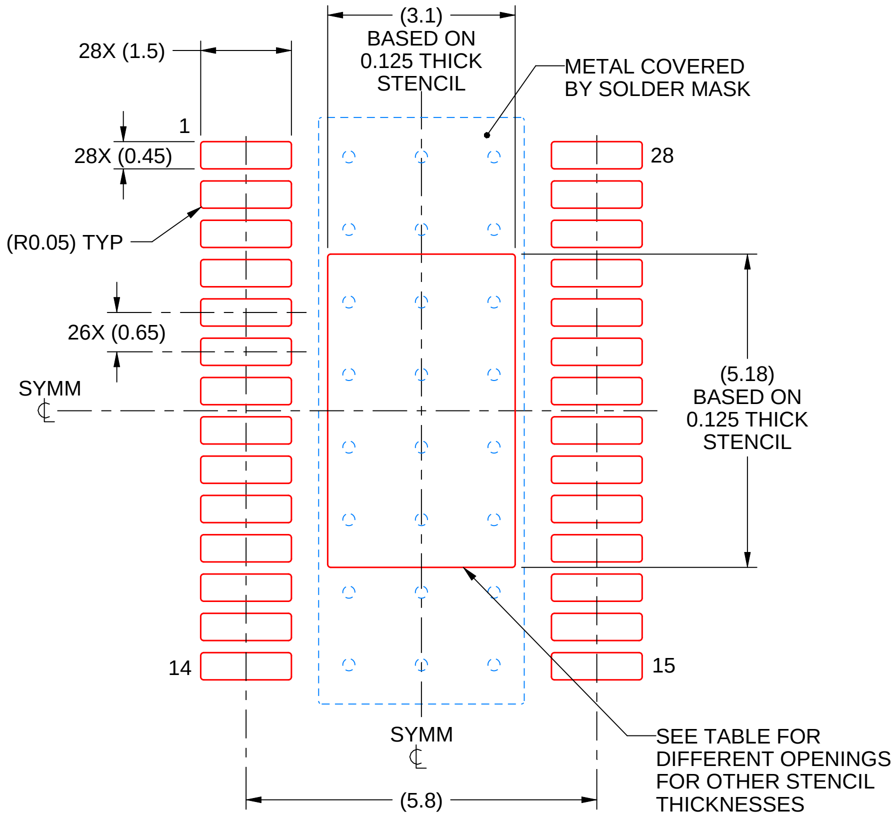
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

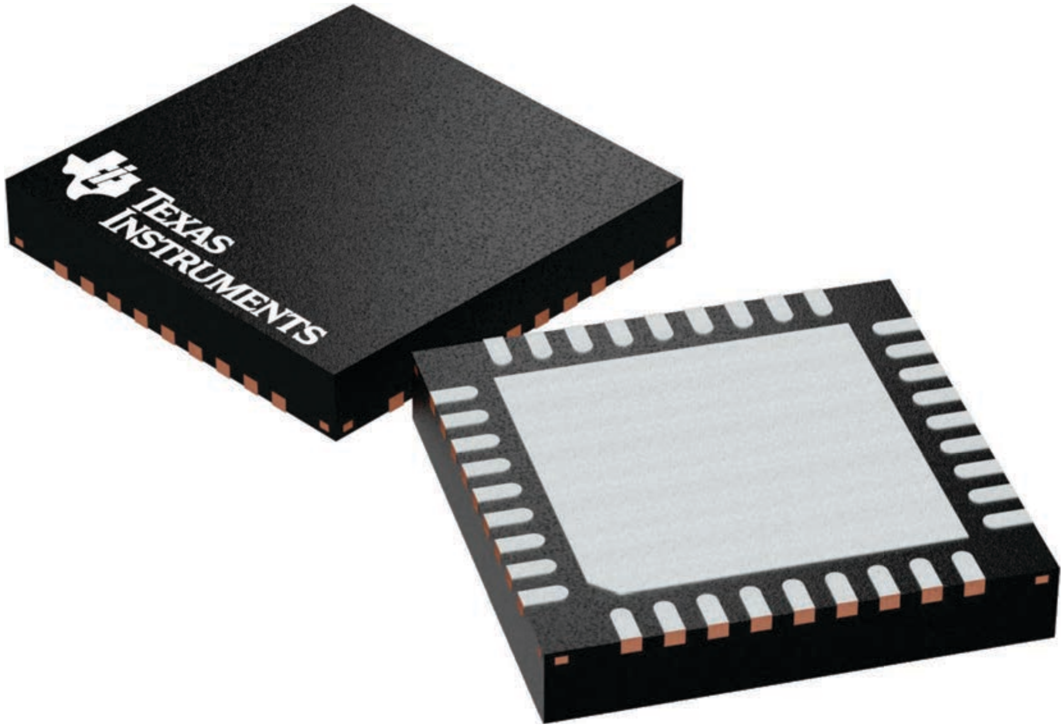
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

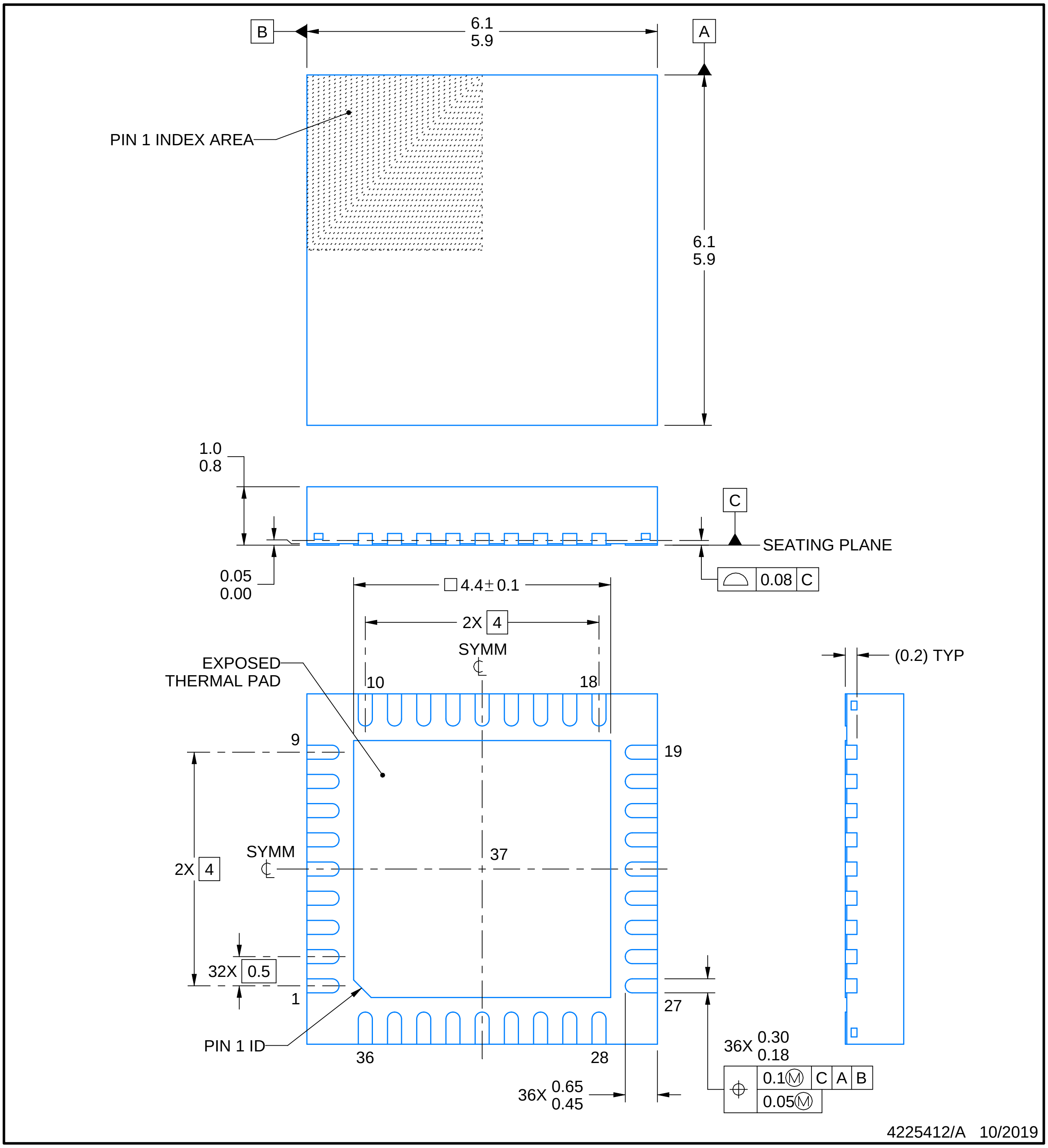
4223582/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

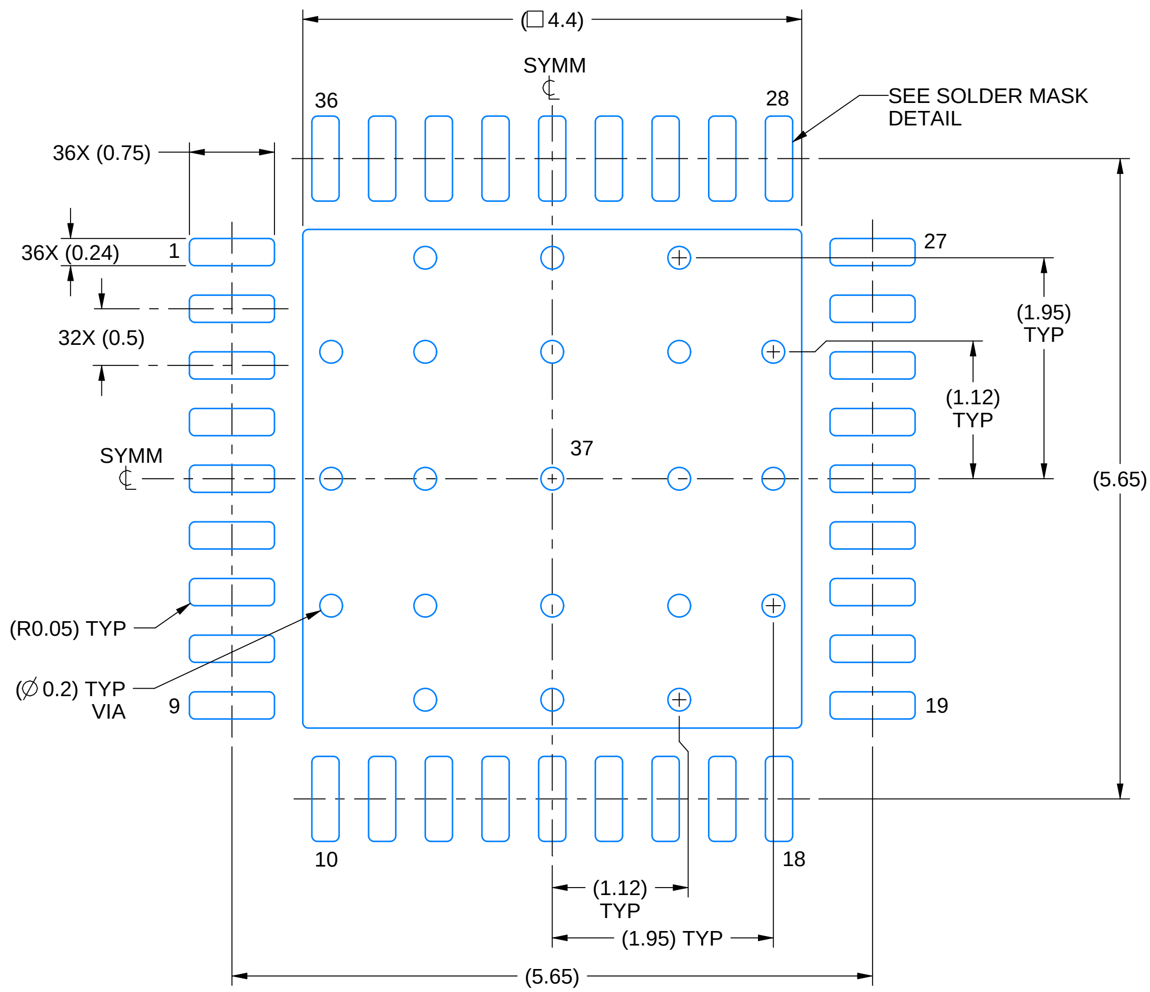
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



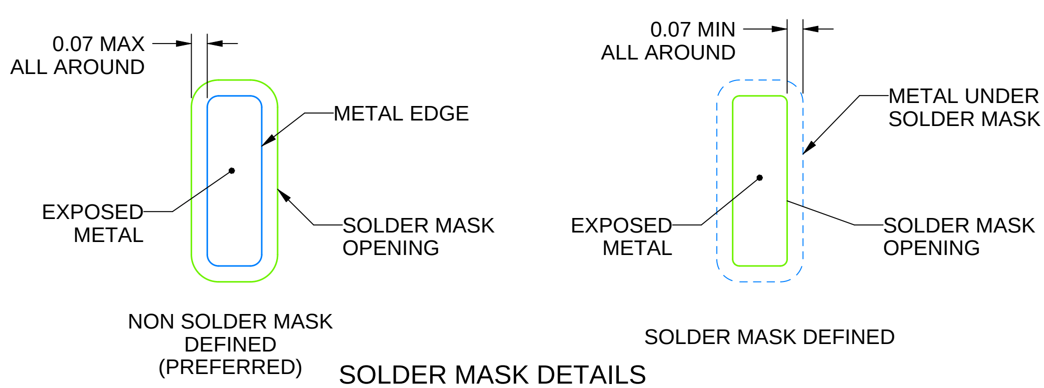


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

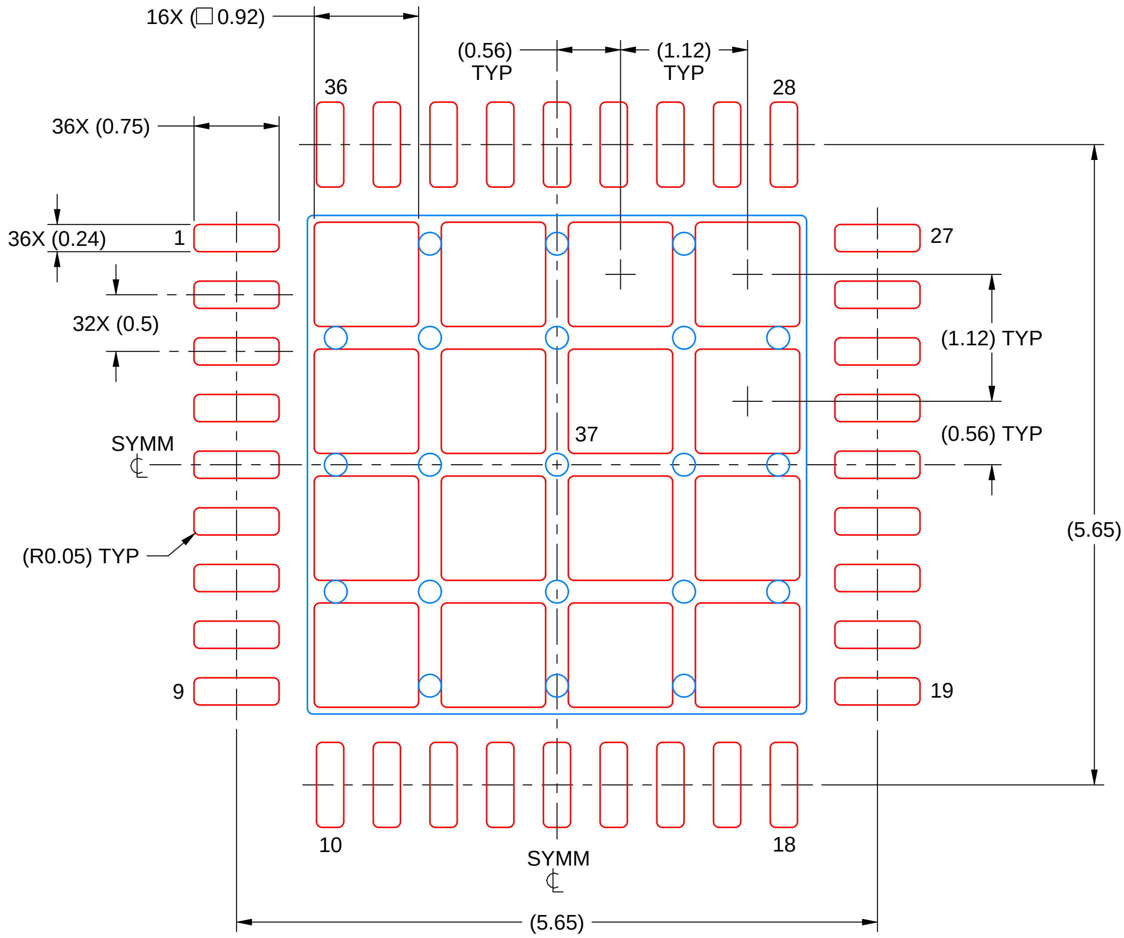


SOLDER MASK DETAILS

4225412/A 10/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
70% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225412/A 10/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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