DAC101C08xx 10 位微功耗 数模转换器，具有 I^2C 兼容接口

1 特性

- 确保单调性达 10 位
- 低功耗运行：3.3V 时的最大电流为 156µA
- 扩展的电源范围（2.7V 至 5.5V）
- I^2C 兼容双线接口，支持标准 (100kHz)、快速 (400kHz) 和高速 (3.4MHz) 三种模式
- 轨到轨电压输出
- 超小型封装
- DAC101C081Q 采用汽车级流程制造，符合 AEC-Q100 1 级标准
- 分辨率：10 位
- 积分非线性 (INL)：±2 最低有效位 (LSB)（最大值）
- 差分非线性 (DNL)：+0.3/-0.2 最低有效位 (LSB)（最大值）
- 稳定时间：6µs（最大值）
- 零码误差：+10mV（最大值）
- 满量程误差：−0.7 %FS（最大值）
- 电源（正常工作）：380µW (3V)/730µW (5V)（典型值）
- 电源（省电模式）：0.5µW (3V)/0.9µW (5V)（典型值）

2 应用

- 工业过程控制
- 便携式仪器
- 数字增益和偏移调整
- 可编程电压源和电流源
- 测试设备
- 汽车

3 说明

DAC101C081 器件是一款 10 位、单通道、电压输出数模转换器 (DAC)，工作电源范围为 2.7V 至 5.5V。输出放大器支持轨到轨输出摆幅，并且具有 6µs 的稳定时间。DAC101C081 使用电源作为基准以提供最宽的动态输出范围，在 5.0V 电压下工作时通常仅消耗 132µA 电流。该器件采用 6 引脚小外形尺寸晶体管 (SOT) 和晶圆级小外形无引线 (WSON) 封装，并且提供三种地址选项（可通过引脚选择）。

DAC101C085 是一款替代产品，提供有 9 种 I^2C™寻址选项且使用外部基准。该器件采用 8 引脚超薄小外形尺寸封装 (VSSOP) 封装，并且与 DAC101C081 具有相同的性能和稳定时间。

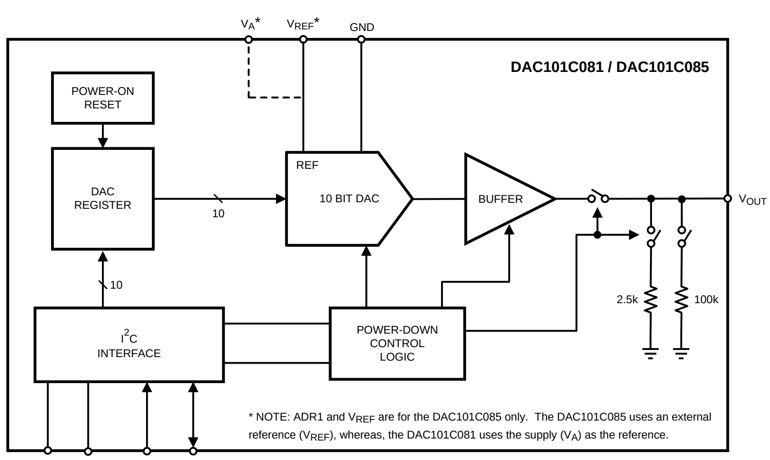
DAC101C081 和 DAC101C085 采用双线 I^2C 兼容串行接口，支持包括高速模式 (3.4MHz) 在内的全部三种速度模式。凭借外部地址选择引脚，每条双线总线上最多可连接 3 个 DAC101C081 或 9 个 DAC101C085 器件。此外，还提供有与 DAC101C081 引脚兼容的替代产品，可提供更多的地址选项。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC101C081	WSON (6)	2.20mm x 2.50mm
	SOT (6)	1.60mm x 2.90mm
DAC101C085	VSSOP (8)	3.00mm × 3.00mm
DAC101C081Q	WSON (6)	2.20mm x 2.50mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (March 2013) to Revision B	**Page**
• *已添加 ESD 额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分。*	1
• Added addresses that the DAC responds to on the I2C bus.	19

Changes from Original (March 2013) to Revision A	**Page**
• Changed layout of National Data Sheet to TI format	28

5 说明 （续）

DAC101C081 和 DAC101C085 均具有一个 16 位寄存器，用于控制工作模式、省电条件和输出电压。上电复位电路可确保 DAC 输出电压在上电时达到 0V。省电特性可使器件功耗降至 1 微瓦以下。低功耗及小型封装特性使得这两款 DAC 成为了电池供电类设备的绝佳选择。每款 DAC 均在 −40°C 至 +125°C 的扩展工业级温度范围内运行。

DAC101C081 和 DAC101C085 所属系列均提供有 12 位和 8 位分辨率的引脚兼容 DAC。12 位 DAC 分别为 DAC121C081 和 DAC121C085。8 位 DAC 分别为 DAC081C081 和 DAC081C085。

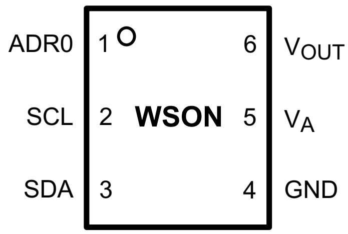
6 Device Comparison Table(1)

Resolution	SOT-6 and WSON-6 Packages	VSSOP-8 Package w/ External Reference
12-bit	DAC121C081	DAC121C085
10-bit	**DAC101C081**	**DAC101C085**
8-bit	DAC081C081	DAC081C085

(1) All devices are fully pin and function compatible.

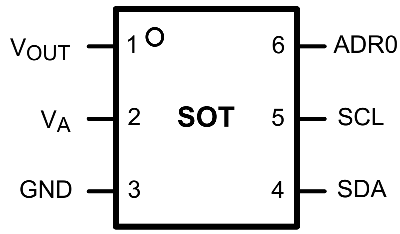
7 Pin Configuration and Functions

NGF Package
6-Pin WSON
Top View



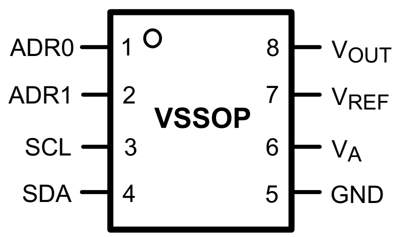
DAC101C081

DDC Package
6-Lead SOT
Top View



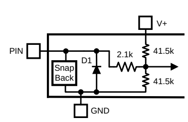
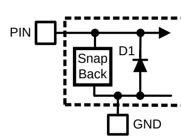
DAC101C081

DGK Package
8-Lead VSSOP
Top View



DAC101C085

Pin Functions

PIN				TYPE	EQUIVALENT CIRCUIT	DESCRIPTION
NAME	WSON	SOT	VSSOP			
ADR0	1	6	1	Digital Input, three levels		Tri-state Address Selection Input. Sets the two Least Significant Bits (A1 and A0) of the 7-bit slave address. (see Table 1)
ADR1	—	—	2	Digital Input, three levels		Tri-State Address Selection Input. Sets Bits A6 and A3 of the 7-bit slave address. (see Table 1)
GND	4	3	5	Ground		Ground for all on-chip circuitry
PAD	PAD	—	—	Ground		Exposed die attach pad can be connected to ground or left floating. Soldering the pad to the PCB offers optimal thermal performance and enhances package self-alignment during reflow.
SCL	2	5	3	Digital Input		Serial Clock Input. SCL is used together with SDA to control the transfer of data in and out of the device.
SDA	3	4	4	Digital Input/Output		Serial Data bi-directional connection. Data is clocked into or out of the internal 16-bit register relative to the clock edges of SCL. This is an open drain data line that must be pulled to the supply (V_A) by an external pullup resistor.
V_A	5	2	6	Supply		Power supply input. For the SOT and WSON versions, this supply is used as the reference. Must be decoupled to GND.
V_{OUT}	6	1	8	Analog Output		Analog Output Voltage
V_{REF}	—	—	7	Supply		Unbufferred reference voltage. For the VSSOP-8, this supply is used as the reference. V_{REF} must be free of noise and decoupled to GND.

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)(3)

	MIN	MAX	UNIT
Supply voltage, V_A	−0.3	6.5	V
Voltage on any input pin	−0.3	6.5	V
Input current at any pin (4)		±10	mA
Package input current (4)		±20	mA
Power consumption at T_A = 25°C	See (5)		
Operating junction temperature		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds 5.5 V or is less than GND, the current at that pin should be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A) / θ_{JA}. The values for maximum power dissipation will be reached only when the device is operated in a severe fault condition (e.g., when input or output pins are driven beyond the operating ratings, or the power supply polarity is reversed).

8.2 ESD Ratings

				VALUE	UNIT
DAC081C081 in NGF Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except 2 and 3	±2500	V
			Pins 2 and 3	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins except 2 and 3	±1000	
			Pins 2 and 3	±1000	
		Machine model (MM)	All pins except 2 and 3	±250	
			Pins 2 and 3	±350	
DAC081C081 in DDC Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except 4 and 5	±2500	V
			Pins 4 and 5	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins except 4 and 5	±1000	
			Pins 4 and 5	±1000	
		Machine model (MM)	All pins except 4 and 5	±250	
			Pins 4 and 5	±350	
DAC081C085 in DGK Package					
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins except 3 and 4	±2500	V
			Pins 3 and 4	±5000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101	All pins except 3 and 4	±1000	
			Pins 3 and 4	±1000	
		Machine model (MM)	All pins except 3 and 4	±250	
			Pins 3 and 4	±350	

8.3 Recommended Operating Conditions

See (1)

	MIN	NOM	MAX	UNIT
Operating temperature range	−40	T_A	125	°C
Supply voltage, V_A	2.7		5.5	V
Reference voltage, V_{REFIN}	1		V_A	V
Digital input voltage(2)(3)	0		5.5	V
Output load	0		1500	pF

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(2) The inputs are protected as shown below. Input voltage magnitudes up to 5.5 V, regardless of V_A, will not cause errors in the conversion result. For example, if V_A is 3 V, the digital input pins can be driven with a 5 V logic device.
(3) To ensure accuracy, it is required that V_A and V_{REF} be well bypassed.

8.4 Thermal Information

THERMAL METRIC(1)(2)(3)		DAC101C081	DAC101C081, DAC101C081Q	DAC101C085	UNIT
		DDC (SOT)	NGF (WSON)	DGK (VSSOP)	
		6 PINS	6 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	250	190	240	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Soldering process must comply with Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.
(3) Reflow temperature profiles are different for lead-free packages.

8.5 Electrical Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 12 to 1011. All Maximum and Minimum limits apply for $T_{MIN} \leq T_A \leq T_{MAX}$ and all Typical limits are at T_A = 25°C (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(1)	UNIT
STATIC PERFORMANCE						
	Resolution		10			Bits
	Monotonicity		10			Bits
INL	Integral non-linearity			+0.6	+2	LSB
			−2	−0.4		LSB
DNL	Differential non-linearity			+0.12	+0.3	LSB
			−0.2	−0.04		LSB
ZE	Zero code error	I_{OUT} = 0		+1.1	+10	mV
FSE	Full-scale error	I_{OUT} = 0		−0.1	−0.7	%FSR
GE	Gain error	All ones loaded to DAC register		−0.2	−0.7	%FSR
ZCED	Zero code error drift			−20		µV/°C
TC GE	Gain error tempco	V_A = 3 V		−0.7		ppm FSR/°C
		V_A = 5 V		−1		ppm FSR/°C
ANALOG OUTPUT CHARACTERISTICS (V_{OUT})						
	Output voltage range(2)	DAC101C085	0		V_{REF}	V
		DAC101C081	0		V_A	V
ZCO	Zero code output	V_A = 3 V, I_{OUT} = 200 µA		1.3		mV
		V_A = 5 V, I_{OUT} = 200 µA		7.0		mV
FSO	Full scale output	V_A = 3 V, I_{OUT} = 200 µA		2.984		V
		V_A = 5 V, I_{OUT} = 200 µA		4.989		V

(1) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(2) This parameter is ensured by design and/or characterization and is not tested in production.

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 12 to 1011. All Maximum and Minimum limits apply for $T_{MIN} \le T_A \le T_{MAX}$ and all Typical limits are at T_A = 25°C (unless otherwise specified).

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX (1)	UNIT
I_{OS}	Output short circuit current (I_{SOURCE})	V_A = 3 V, V_{OUT} = 0 V, Input code = FFFh.		56		mA
		V_A = 5 V, V_{OUT} = 0 V, Input code = FFFh.		69		mA
I_{OS}	Output short circuit current (I_{SINK})	V_A = 3 V, V_{OUT} = 3 V, Input code = 000h.		−52		mA
		V_A = 5 V, V_{OUT} = 5 V, Input code = 000h.		−75		mA
I_O	Continuous output current (2)	Available on the DAC output			11	mA
C_L	Maximum load capacitance	R_L = ∞		1500		pF
		R_L = 2 kΩ		1500		pF
Z_{OUT}	DC output impedance			7.5		Ω
REFERENCE INPUT CHARACTERISTICS- (DAC101C085 only)						
V_{REF}	Input range inimum		1	0.2		V
	Input range maximum				V_A	V
	Input impedance			120		kΩ
LOGIC INPUT CHARACTERISTICS (SCL, SDA)						
V_{IH}	Input high voltage		0.7 × V_A			V
V_{IL}	Input low voltage				0.3 × V_A	V
I_{IN}	Input current				±1	µA
C_{IN}	Input pin capacitance (2)				3	pF
V_{HYST}	Input hysteresis		0.1 × V_A			V
LOGIC INPUT CHARACTERISTICS (ADR0, ADR1)						
V_{IH}	Input high voltage		V_A– 0.5			V
V_{IL}	Input low voltage				0.5	V
I_{IN}	Input current				±1	µA
LOGIC OUTPUT CHARACTERISTICS (SDA)						
V_{OL}	Output low voltage	I_{SINK} = 3 mA			0.4	V
		I_{SINK} = 6 mA			0.6	V
I_{OZ}	High-impedence output leakage current				±1	µA
POWER REQUIREMENTS						
V_A	Supply voltage minimum		2.7			V
	Supply voltage maximum				5.5	V
Normal -- V_{OUT} set to midscale. 2-wire interface quiet (SCL = SDA = V_A). (output unloaded)						
I_{ST_VA-1}	V_A**DAC101C081** supply current	V_A = 2.7 V to 3.6 V		105	156	µA
		V_A = 4.5 V to 5.5 V		132	214	µA
I_{ST_VA-5}	V_A**DAC101C085** supply current	V_A = 2.7 V to 3.6 V		86	118	µA
		V_A = 4.5 V to 5.5 V		98	152	µA
I_{ST_VREF}	V_{REF} supply current (DAC101C085 only)	V_A = 2.7 V to 3.6 V		37	43	µA
		V_A = 4.5 V to 5.5 V		53	61	µA
P_{ST}	Power consumption (V_A & V_{REF} for DAC101C085)	V_A = 3 V		380		µW
		V_A = 5 V		730		µW
Continuous Operation -- 2-wire interface actively addressing the DAC and writing to the DAC register. (output unloaded)						

Electrical Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, C_L = 200 pF to GND, input code range 12 to 1011. All Maximum and Minimum limits apply for T_{MIN} ≤ T_A ≤ T_{MAX} and all Typical limits are at T_A = 25°C (unless otherwise specified).

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX(1)	UNIT
I_{CO_VA-1}	V_A **DAC101C081** supply current	f_{SCL} = 400 kHz	V_A = 2.7 V to 3.6 V		134	220	µA
			V_A = 4.5 V to 5.5 V		192	300	µA
		f_{SCL} = 3.4 MHz	V_A = 2.7 V to 3.6 V		225	320	µA
			V_A = 4.5 V to 5.5 V		374	500	µA
I_{CO_VA-5}	V_A **DAC101C085** supply current	f_{SCL} = 400 kHz	V_A = 2.7 V to 3.6 V		101	155	µA
			V_A = 4.5 V to 5.5 V		142	220	µA
		f_{SCL} = 3.4 MHz	V_A = 2.7 V to 3.6 V		193	235	µA
			V_A = 4.5 V to 5.5 V		325	410	µA
I_{CO_VREF}	V_{REF} supply current (DAC101C085 only)		V_A = 2.7 V to 3.6 V		33.5	55	µA
			V_A = 4.5 V to 5.5 V		49.5	71.4	µA
P_{CO}	Power consumption (V_A & V_{REF} for DAC101C085)	f_{SCL} = 400 kHz	V_A = 3 V		480		µW
			V_A = 5 V		1.06		mW
		f_{SCL} = 3.4 MHz	V_A = 3 V		810		µW
			V_A = 5 V		2.06		mW
Power Down -- 2-wire interface quiet (SCL = SDA = V_A) after PD mode written to DAC register. (output unloaded)							
I_{PD}	Supply current (V_A & V_{REF} for DAC101C085)	All power-down modes	V_A = 2.7 V to 3.6 V		0.13	1.52	µA
			V_A = 4.5 V to 5.5 V		0.15	3.25	µA
P_{PD}	Power consumption (V_A & V_{REF} for DAC101C085)	All power-down modes	V_A = 3 V		0.5		µW
			V_A = 5 V		0.9		µW

8.6 AC and Timing Characteristics

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, R_L = Infinity, C_L = 200 pF to GND. All Maximum and Minimum limits apply for T_{MIN} ≤ T_A ≤ T_{MAX} and all Typical limits are at T_A = 25°C (unless otherwise specified).

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX(1)(3)	UNIT
t_s	Output voltage settling time(4)	100h to 300h code change R_L = 2 kΩ, C_L = 200 pF		4.5	6	µs
SR	Output slew rate			1		V/µs
	Glitch impulse	Code change from 200h to 1FFh		12		nV-sec
	Digital feedthrough			0.5		nV-sec
	Multiplying bandwidth(5)	V_{REF} = 2.5 V ± 0.1 Vpp		160		kHz
	Total harmonic distortion(5)	V_{REF} = 2.5 V ± 0.1 Vpp input frequency = 10 kHz		70		dB

(1) C_b refers to the capacitance of one bus line. C_b is expressed in pF units.
(2) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(3) Typical figures are at T_J = 25°C, and represent most likely parametric norms. Test limits are specified to AOQL (Average Outgoing Quality Level).
(4) This parameter is ensured by design and/or characterization and is not tested in production.
(5) Applies to the Multiplying DAC configuration. In this configuration, the reference is used as the analog input. The value loaded in the DAC Register will digitally attenuate the signal at Vout.

AC and Timing Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, R_L = Infinity, C_L = 200 pF to GND. All Maximum and Minimum limits apply for $T_{MIN} \le T_A \le T_{MAX}$ and all Typical limits are at T_A = 25°C (unless otherwise specified).

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX(1)(3)	UNIT
t_{WU}	Wake-up time	V_A = 3 V		0.8		µsec
		V_A = 5 V		0.5		µsec
DIGITAL TIMING SPECS (SCL, SDA)						
f_{SCL}	Serial clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
		High speed mode, C_b = 100 pF			3.4	MHz
		High speed mode, C_b = 400 pF			1.7	MHz
t_{LOW}	SCL low time	Standard mode	4.7			µs
		Fast mode	1.3			µs
		High speed mode, C_b = 100 pF	160			ns
		High speed mode, C_b = 400 pF	320			ns
t_{HIGH}	SCL high time	Standard mode	4			µs
		Fast mode	0.6			µs
		High speed mode, C_b = 100 pF	60			ns
		High speed mode, C_b = 400 pF	120			ns
$t_{SU;DAT}$	Data set-up time	Standard mode	250			ns
		Fast mode	100			ns
		High speed mode	10			ns
$t_{HD;DAT}$	Data hold time	Standard mode	0		3.45	µs
		Fast mode	0		0.9	µs
		High speed mode, C_b = 100 pF	0		70	ns
		High speed mode, C_b = 400 pF	0		150	ns
$t_{SU;STA}$	Set-up time for a start or a repeated start condition	Standard mode	4.7			µs
		Fast mode	0.6			µs
		High speed mode	160			ns
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard mode	4			µs
		Fast mode	0.6			µs
		High speed mode	160			ns
t_{BUF}	Bus free time between a stop and start condition	Standard mode	4.7			µs
		Fast mode	1.3			µs
$t_{SU;STO}$	Set-up time for a stop condition	Standard mode	4			µs
		Fast mode	0.6			µs
		High speed mode	160			ns
t_{rDA}	Rise time of SDA signal	Standard mode			1000	ns
		Fast mode	20 + 0.1C_b		300	ns
		High speed mode, C_b = 100 pF	10		80	ns
		High speed mode, C_b = 400 pF	20		160	ns
t_{fDA}	Fall time of SDA signal	Standard mode			250	ns
		Fast mode	20 + 0.1C_b		250	ns
		High speed mode, C_b = 100 pF	10		80	ns
		High speed mode, C_b = 400 pF	20		160	ns
t_{rCL}	Rise time of SCL signal	Standard mode			1000	ns
		Fast mode	20 + 0.1C_b		300	ns
		High speed mode, C_b = 100 pF	10		40	ns
		High speed mode, C_b = 400 pF	20		80	ns

AC and Timing Characteristics (continued)

The following specifications apply for V_A = 2.7 V to 5.5 V, V_{REF} = V_A, R_L = Infinity, C_L = 200 pF to GND. All Maximum and Minimum limits apply for $T_{MIN} \le T_A \le T_{MAX}$ and all Typical limits are at T_A = 25°C (unless otherwise specified).

PARAMETER		TEST CONDITIONS(1)	MIN	TYP(2)	MAX(1)(3)	UNIT
t_{rCL1}	Rise time of SCL signal after a repeated start condition and after an acknowledge bit.	Standard mode			1000	ns
		Fast mode	20 + 0.1C_b		300	ns
		High speed mode, C_b = 100 pF	10		80	ns
		High speed mode, C_b = 400 pF	20		160	ns
t_{fCL}	Fall time of a SCL signal	Standard mode			300	ns
		Fast mode	20 + 0.1C_b		300	ns
		High speed mode, C_b = 100 pF	10		40	ns
		High speed mode, C_b = 400 pF	20		80	ns
C_b	Capacitive load for each bus line (SCL and SDA)				400	pF
t_{SP}	Pulse width of spike suppressed(6)(4)	Fast mode			50	ns
		High speed mode			10	
t_{outz}	SDA output delay (see Section 1.9)	Fast mode		87	270	ns
		High speed mode		38	60	

(6) Spike suppression filtering on SCL and SDA will supress spikes that are less than 50ns for standard-fast mode and less than 10ns for hs-mode.

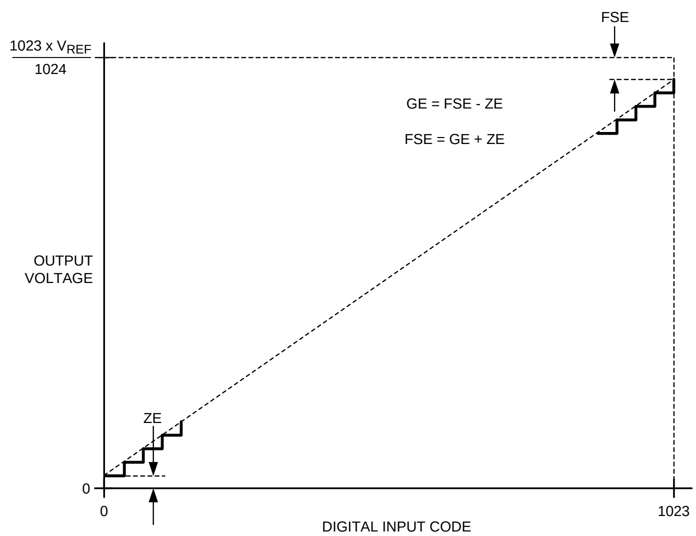


Figure 1. Input / Output Transfer Characteristic

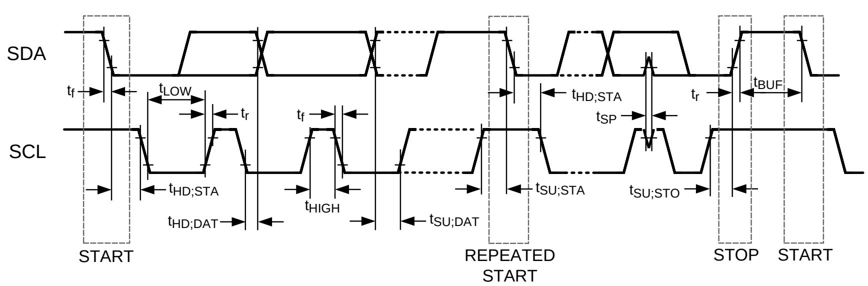


Figure 2. Serial Timing Diagram

8.7 Typical Characteristics

$V_{REF} = V_A$, f_{SCL} = 3.4 MHz, T_A = 25°C, input code range 12 to 1011 (unless otherwise stated).

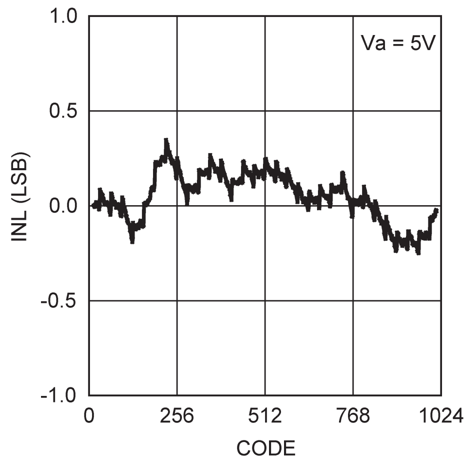


Figure 3. Define (INL)

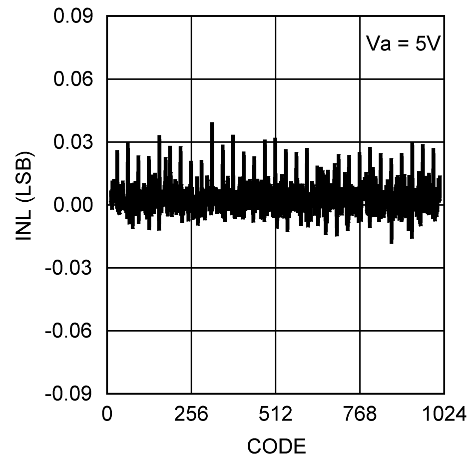


Figure 4. Define (DNL)

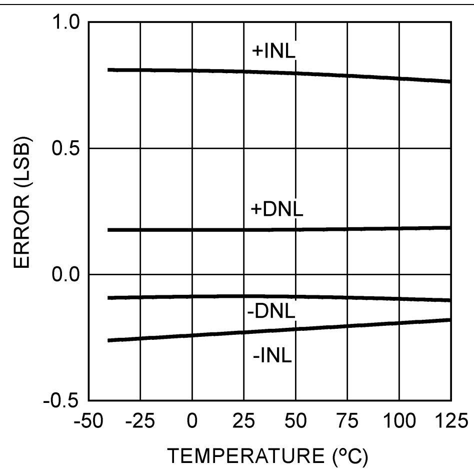


Figure 5. INL/DNL vs Temperature at V_A = 3.0 V

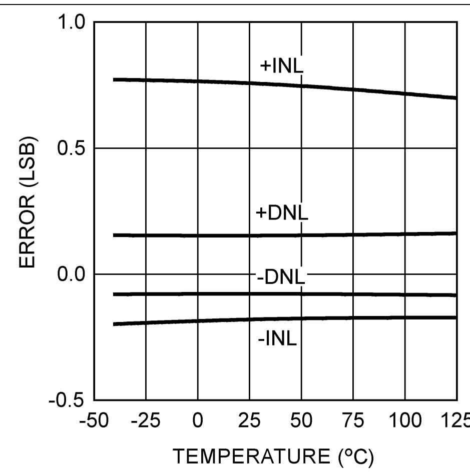


Figure 6. INL/DNL vs Temperature at V_A = 5 V

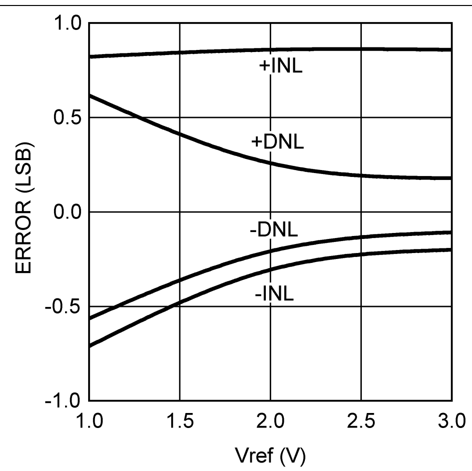


Figure 7. INL/DNL vs V_{REFIN} at V_A = 3 V

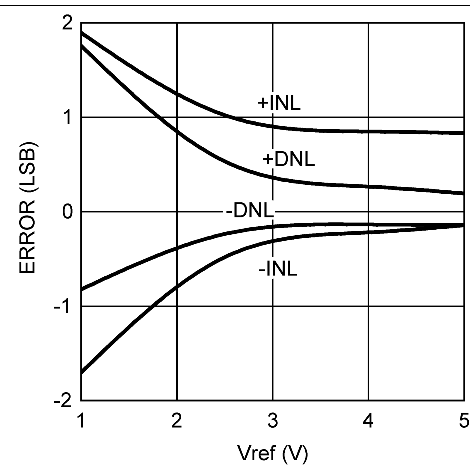


Figure 8. INL/DNL vs V_{REFIN} at V_A = 5 V

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCL} = 3.4 MHz, T_A = 25°C, input code range 12 to 1011 (unless otherwise stated).

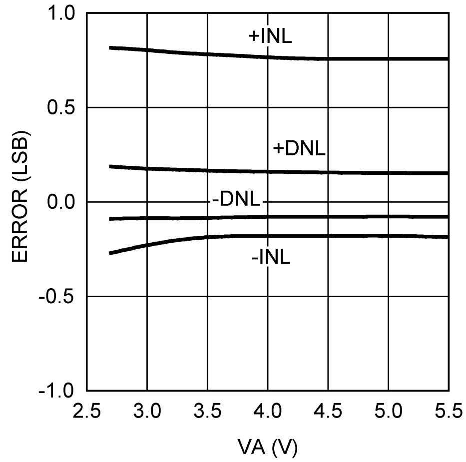


Figure 9. INL/DNL vs V_A

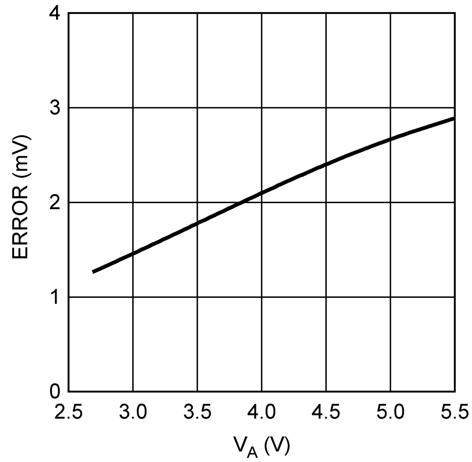


Figure 10. Zero Code Error vs V_A

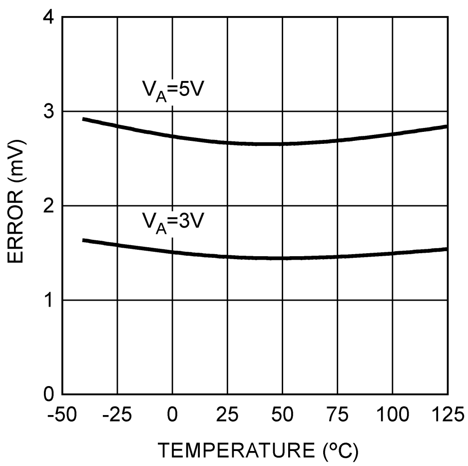


Figure 11. Zero Code Error vs Temperature

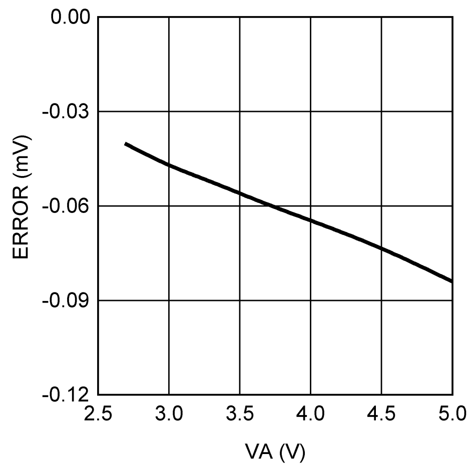


Figure 12. Full Scale Error vs V_A

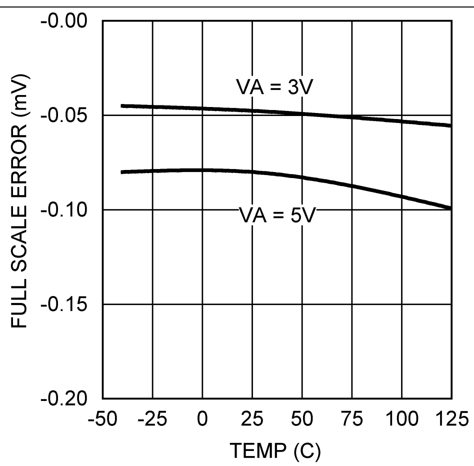


Figure 13. Full Scale Error vs Temperature

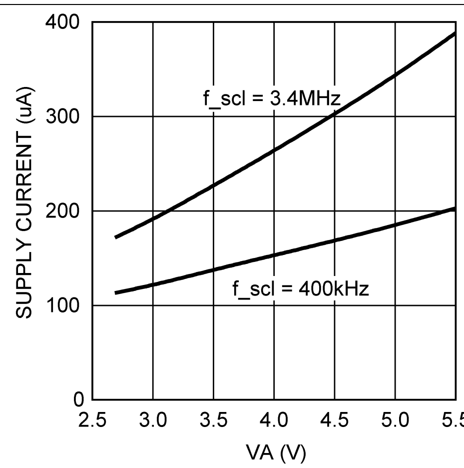


Figure 14. Total Supply Current vs V_A

Typical Characteristics (continued)

$V_{REF} = V_A$, f_{SCL} = 3.4 MHz, T_A = 25°C, input code range 12 to 1011 (unless otherwise stated).

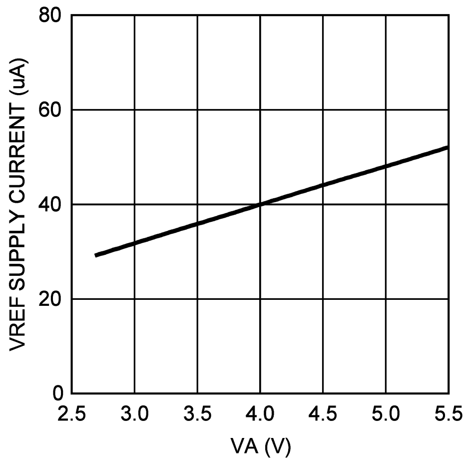


Figure 15. V_{REF} Supply Current vs V_A

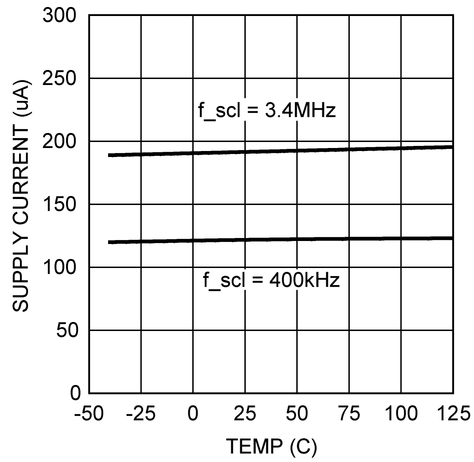


Figure 16. Total Supply Current vs Temperature at V_A = 3 V

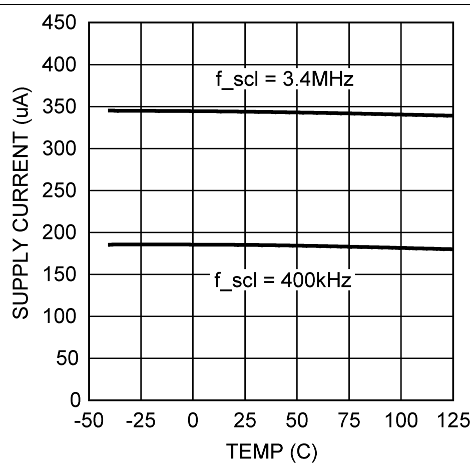


Figure 17. Total Supply Current vs Temperature at V_A = 5 V

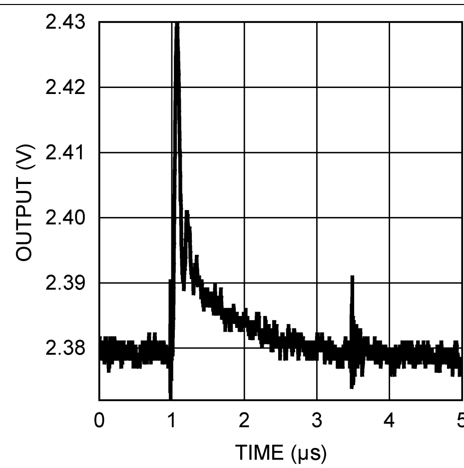


Figure 18. 5 V Glitch Response

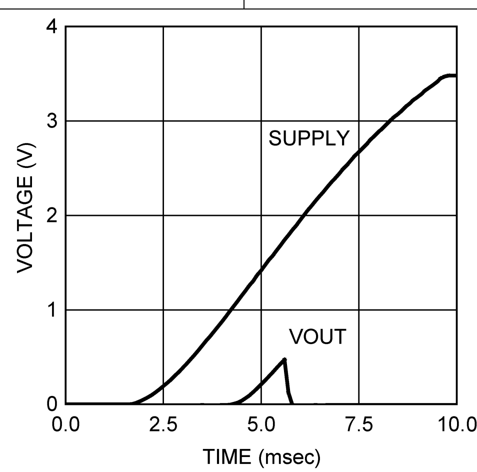


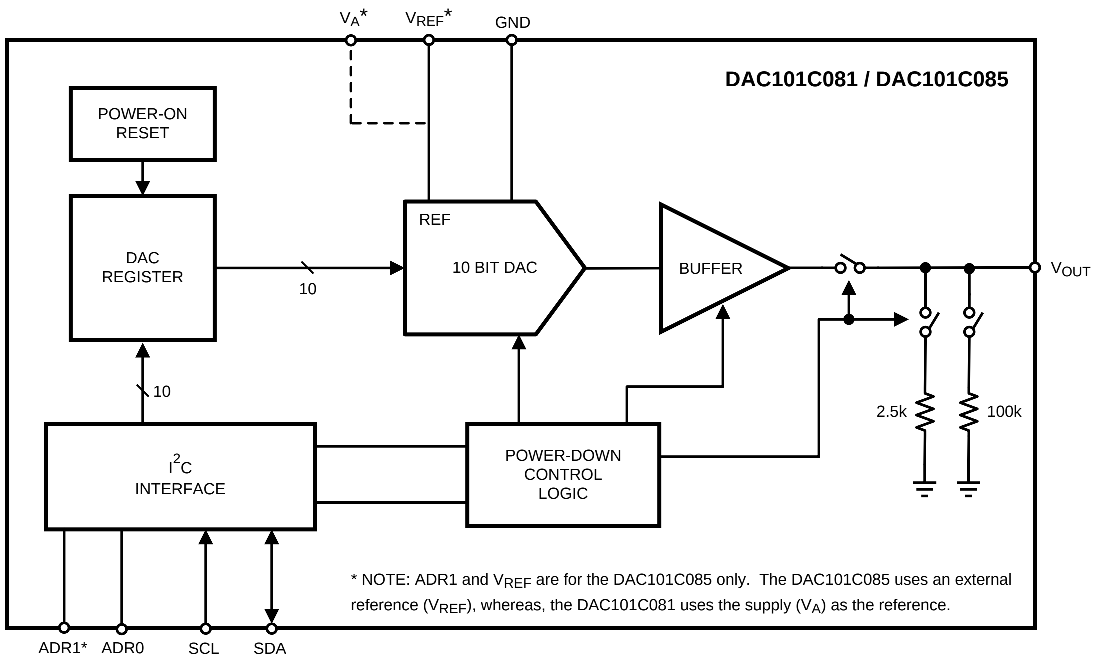
Figure 19. Power-On Reset

9 Detailed Description

9.1 Overview

The DAC101C081 is fabricated on a CMOS process with an architecture that consists of switches and resistor strings that are followed by an output buffer.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 DAC Section

For simplicity, a single resistor string is shown in Figure 20. This string consists of 1024 equal valued resistors with a switch at each junction of two resistors, plus a switch to ground. The code loaded into the DAC register determines which switch is closed, connecting the proper node to the amplifier. The input coding is straight binary with an ideal output voltage of:

$$V_{OUT} = V_{REF} \times (D / 1024) \quad (1)$$

where *D* is the decimal equivalent of the binary code that is loaded into the DAC register. D can take on any integer value between 0 and1023. This configuration ensures that the DAC is monotonic.

Feature Description (continued)

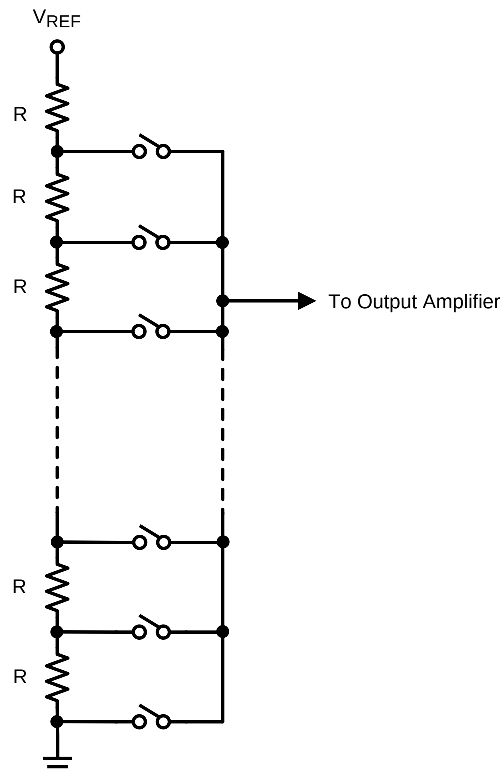


Figure 20. DAC Resistor String

9.3.2 Output Amplifier

The output amplifier is rail-to-rail, providing an output voltage range of 0 V to V_A when the reference is V_A. All amplifiers, even rail-to-rail types, exhibit a loss of linearity as the output approaches the supply rails (0 V and V_A, in this case). For this reason, linearity is specified over less than the full output range of the DAC. However, if the reference is less than V_A, there is only a loss in linearity in the lowest codes. The output capabilities of the amplifier are described in the *Electrical Characteristics* table.

The output amplifiers are capable of driving a load of 2-kΩ in parallel with 1500 pF to ground or to V_A. The zero-code and full-scale outputs for given load currents are available in the *Electrical Characteristics* table.

9.3.3 Reference Voltage

The DAC101C081 uses the supply (V_A) as the reference. With that said, V_A must be treated as a reference. The Analog output will only be as clean as the reference (V_A). It is recommended that the reference be driven by a voltage source with low output impedance.

The DAC101C085 comes with an external reference supply pin (V_{REF}). For the DAC101C085, it is important that V_{REF} be kept as clean as possible.

The *Applications Information* section describes a handful of ways to drive the reference appropriately. Refer to *Using References as Power Supplies* for details.

9.3.4 Power-On Reset

The power-on reset circuit controls the output voltage of the DAC during power-up. Upon application of power, the DAC register is filled with zeros and the output voltage is 0 Volts. The output remains at 0 V until a valid write sequence is made to the DAC.

Feature Description (continued)

When resetting the device, it is crutial that the V_A supply be lowered to a maximum of 200mV before the supply is raised again to power-up the device. Dropping the supply to within 200mV of GND during a reset will ensure the ADC performs as specified.

9.3.5 Simultaneous Reset

The broadcast address allows the I^2C™ master to write a single word to multiple DACs simultaneously. Provided that all of the DACs exist on a singleI^2C™ bus, every DAC will update when the broadcast address is used to address the bus. This feature allows the master to reset all of the DACs on a shared I^2C™ bus to a specific digital code. For instance, if the master writes a power-down code to the bus with the broadcast address, all of the DACs will power-down simultaneously.

9.3.6 Additional Timing Information: t_{outz}

The t_{outz} specification is provided to aid the design of the I^2C bus. After the SCL bus is driven low by the I^2C™ master, the SDA bus will be held for a short time by the DAC101C081. This time is referred to as t_{outz}. The following figure illustrates the relationship between the fall of SCL, at the 30% threshold, to the time when the DAC begins to transition the SDA bus. The t_{outz} specification only applies when the DAC is in control of the SDA bus. The DAC is only in control of the bus during an ACK by the DAC101C081 or a data byte read from the DAC (see Figure 25).

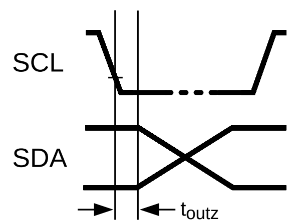


Figure 21. Data Output Timing

The t_{outz} specification is typically 87nsec in Standard-Fast Mode and 38nsec in Hs-Mode.

9.4 Device Functional Modes

9.4.1 Power-Down Modes

The DAC101C081 has three power-down modes. In power-down mode, the supply current drops to 0.13µA at 3 V and 0.15µA at 5 V (typ). The DAC101C081 is put into power-down mode by writing a one to PD1 and/or PD0. The outputs can be set to high impedance, terminated by 2.5 kΩ to GND, or terminated by 100 kΩ to GND (see Figure 26).

The bias generator, output amplifier, resistor string, and other linear circuitry are all shut down in any of the power-down modes. When the DAC101C081 is powered down, the value written to the DAC register, including the power-down bits, is saved. While the DAC is in power-down, the saved DAC register contents can be read back. When the DAC is brought out of power-down mode, the DAC register contents will be overwritten and V_{OUT} will be updated with the new 10-bit data value.

The time to exit power-down (Wake-Up Time) is typically 0.8µsec at 3 V and 0.5µsec at 5 V.

9.5 Programming

9.5.1 Serial Interface

The I²C™-compatible interface operates in all three speed modes. Standard mode (100kHz) and Fast mode (400 kHz) are functionally the same and will be referred to as Standard-Fast mode in this document. High-Speed mode (3.4 MHz) is an extension of Standard-Fast mode and will be referred to as Hs-mode in this document. The following diagrams describe the timing relationships of the clock (SCL) and data (SDA) signals. Pullup resistors or current sources are required on the SCL and SDA busses to pull them high when they are not being driven low. A logic zero is transmitted by driving the output low. A logic high is transmitted by releasing the output and allowing it to be pulled-up externally. The appropriate pullup resistor values will depend upon the total bus capacitance and operating speed.

9.5.2 Basic I²C™ Protocol

The I²C™ interface is bi-directional and allows multiple devices to operate on the same bus. To facilitate this bus configuration, each device has a unique hardware address which is referred to as the "slave address." To communicate with a particular device on the bus, the controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit. If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled high. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a Stop condition on the bus.

All communication on the bus begins with either a Start condition or a Repeated Start condition. The protocol for starting the bus varies between Standard-Fast mode and Hs-mode. In Standard-Fast mode, the master generates a Start condition by driving SDA from high to low while SCL is high. In Hs-mode, starting the bus is more complicated. Please refer to *High-Speed (Hs) Mode* for the full details of a Hs-mode Start condition. A Repeated Start is generated to either address a different device, or switch between read and write modes. The master generates a Repeated Start condition by driving SDA low while SCL is high. Following the Repeated Start, the master sends out the slave address and a read/write bit as shown in Figure 22. The bus continues to operate in the same speed mode as before the Repeated Start condition.

All communication on the bus ends with a Stop condition. In either Standard-Fast mode or Hs-Mode, a Stop condition occurs when SDA is pulled from low to high while SCL is high. After a Stop condition, the bus remains idle until a master generates a Start condition.

Please refer to the PhilipsI²C™ Specification (Version 2.1 Jan, 2000) for a detailed description of the serial interface.

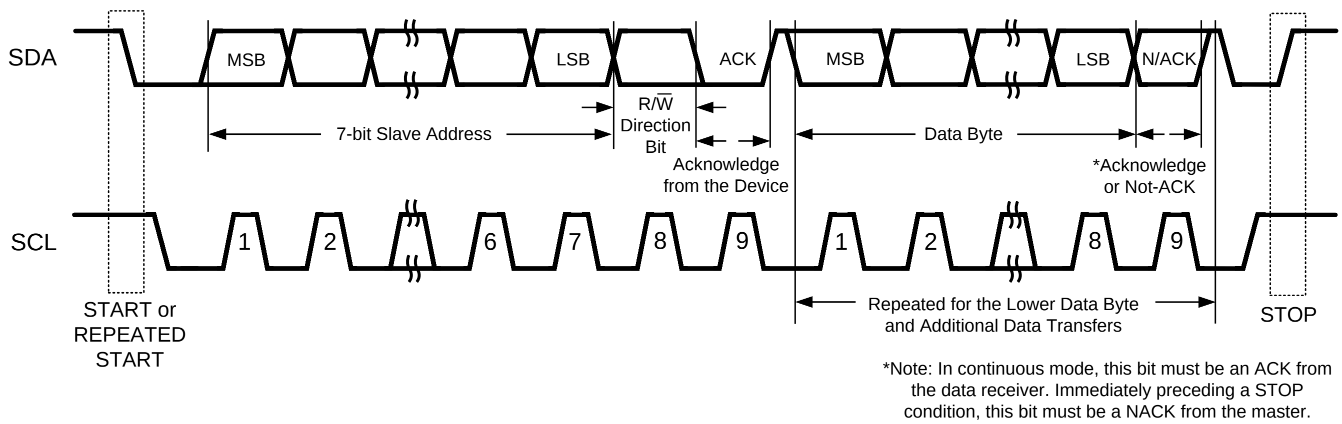


Figure 22. Basic Operation

Programming (continued)

9.5.3 Standard-Fast Mode

In Standard-Fast mode, the master generates a start condition by driving SDA from high to low while SCL is high. The Start condition is always followed by a 7-bit slave address and a Read/Write bit. After these eight bits have been transmitted by the master, SDA is released by the master and the DAC101C081 either ACKs or NACKs the address. If the slave address matches, the DAC101C081 ACKs the master. If the address doesn't match, the DAC101C081 NACKs the master.

For a **write** operation, the master follows the ACK by sending the upper eight data bits to the DAC101C081. Then the DAC101C081 ACKs the transfer by driving SDA low. Next, the lower eight data bits are sent by the master. The DAC101C081 then ACKs the transfer. At this point, the DAC output updates to reflect the contents of the 16-bit DAC register. Next, the master either sends another pair of data bytes, generates a Stop condition to end communication, or generates a Repeated Start condition to communicate with another device on the bus.

For a **read** operation, the DAC101C081 sends out the upper eight data bits of the DAC register. This is followed by an ACK by the master. Next, the lower eight data bits of the DAC register are sent to the master. The master then produces a NACK by letting SDA be pulled high. The NACK is followed by a master-generated Stop condition to end communication on the bus, or a Repeated Start to communicate with another device on the bus.

9.5.4 High-Speed (Hs) Mode

For Hs-mode, the sequence of events to begin communication differ slightly from Standard-Fast mode. Figure 23 describes this in further detail. Initially, the bus begins running in Standard-Fast mode. The master generates a Start condition and sends the 8-bit Hs master code (00001XXX) to the DAC101C081. Next, the DAC101C081 responds with a NACK. Once the SCL line has been pulled to a high level, the master switches to Hs-mode by increasing the bus speed and generating a Repeated Start condition (driving SDA low while SCL is pulled high). At this point, the master sends the slave address to the DAC101C081, and communication continues as shown above in the "Basic Operation" Diagram (see Figure 22).

When the master generates a Repeated Start condition while in Hs-mode, the bus stays in Hs-mode awaiting the slave address from the master. The bus continues to run in Hs-mode until a Stop condition is generated by the master. When the master generates a Stop condition on the bus, the bus must be started in Standard-Fast mode again before increasing the bus speed and switching to Hs-mode.

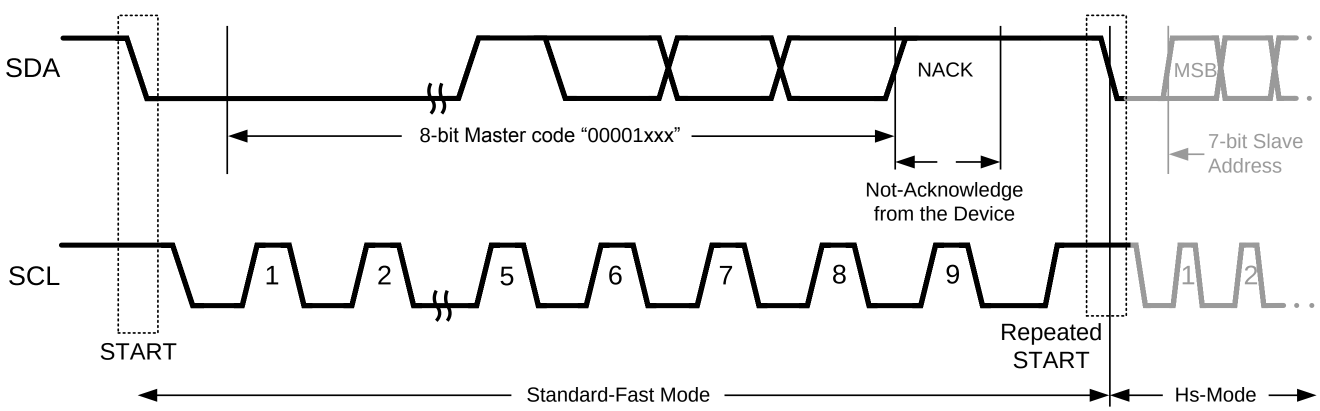


Figure 23. Beginning Hs-Mode Communication

Programming (continued)

9.5.5 I²C Slave (Hardware) Address

The DAC has a seven-bit I²C™ slave address. For the VSSOP-8 version of the DAC, this address is configured by the ADR0 and ADR1 address selection inputs. For the DAC101C081, the address is configured by the ADR0 address selection input. ADR0 and ADR1 can be grounded, left floating, or tied to V_A. If desired, the address selection inputs can be set to $V_A/2$ rather than left floating. The state of these inputs sets the address the DAC responds to on the I²C™ bus (see Table 1). In addition to the selectable slave address, there is also a broadcast address (1001000) for all DAC101C081's and DAC101C085's on the 2-wire bus. When the bus is addressed by the broadcast address, all the DAC101C081's and DAC101C085's will respond and update synchronously. Figure 24 and Figure 25 describe how the master device should address the DAC via the I²C™-Compatible interface.

Keep in mind that the address selection inputs (ADR0 and ADR1) are only sampled until the DAC is correctly addressed with a non-broadcast address. At this point, the ADR0 and ADR1 inputs Tri-State and the slave address is "locked". Changes to ADR0 and ADR1 will not update the selected slave address until the device is power-cycled.

Table 1. Slave Addresses

SLAVE ADDRESS [A6 - A0]	DAC101C085 (VSSOP-8)		DAC101C081 (SOT & WSON)(1)
	ADR1	ADR0	ADR0
0001100, 1000110	Floating	Floating	Floating
0001101, 1000110	Floating	GND	GND
0001110, 1000111	Floating	V_A	V_A
0001000, 1000100	GND	Floating	—
0001001, 1000100	GND	GND	—
0001010, 1000101	GND	V_A	—
1001100, 1100110	V_A	Floating	—
1001101, 1100110	V_A	GND	—
1001110, 1100111	V_A	V_A	—
1001000, 1100100	Broadcast Address		

(1) Pin-compatible alternatives to the DAC101C081 options are available with additional address options.

9.5.6 Writing to the DAC Register

To write to the DAC, the master addresses the part with the correct slave address (A6-A0) and writes a "zero" to the read/write bit. If addressed correctly, the DAC returns an ACK to the master. The master then sends out the upper data byte. The DAC responds by sending an ACK to the master. Next, the master sends the lower data byte to the DAC. The DAC responds by sending an ACK again. At this point, the master either sends the upper byte of the next data word to be converted by the DAC, generates a Stop condition to end communication, or generates a Repeated Start condition to begin communication with another device on the bus. Until generating a Stop condition, the master can continuously write the upper and lower data bytes to the DAC register. This allows for a maximum DAC conversion rate of 188.9 kilo-conversions per second in Hs-mode.

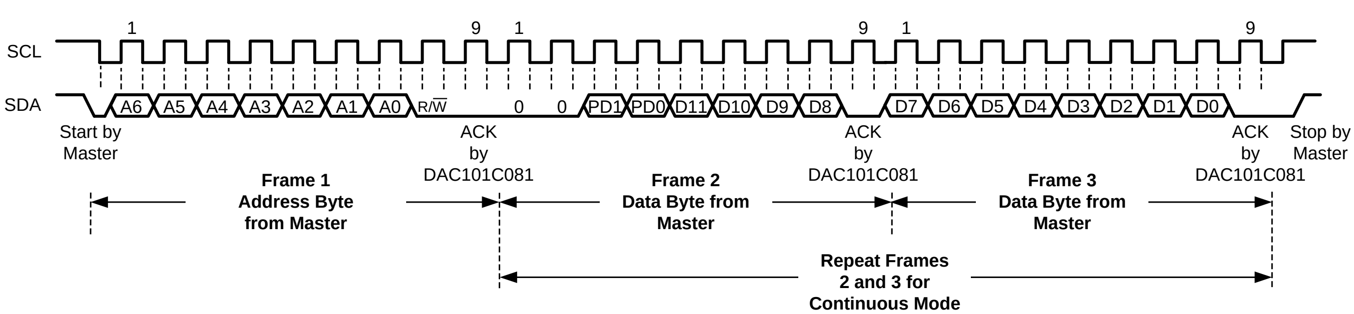


Figure 24. Typical Write to the DAC Register

9.5.7 Reading from the DAC Register

To read from the DAC register, the master addresses the part with the correct slave address (A6-A0) and writes a "one" to the read/write bit. If addressed correctly, the DAC returns an ACK to the master. Next, the DAC sends out the upper data byte. The master responds by sending an ACK to the DAC to indicate that it wants to receive another data byte. Then the DAC sends the lower data byte to the master. Assuming only one 16-bit data word is read, the master sends a NACK after receiving the lower data byte. At this point, the master either generates a Stop condition to end communication, or a Repeated Start condition to begin communication with another device on the bus.

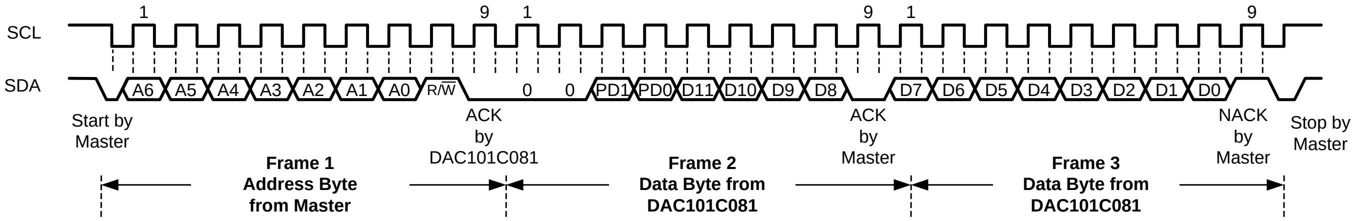


Figure 25. Typical Read from the DAC Register

9.6 Registers

9.6.1 DAC Register

The DAC register, Figure 26, has sixteen bits. The first two bits are always zero. The next two bits determine the mode of operation (normal mode or one of three power-down modes). The final twelve bits of the shift register are the data bits. The data format is straight binary (MSB first, LSB last), with twelve 0's corresponding to an output of 0 V and twelve 1's corresponding to a full-scale output of V_A - 1 LSB. When writing to the DAC Register, V_{OUT} will update on the rising edge of the ACK following the lower data byte.

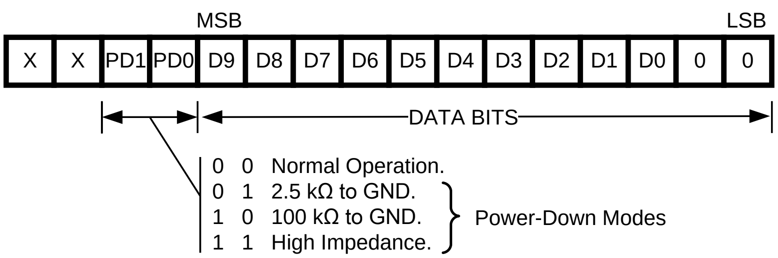


Figure 26. DAC Register Contents

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Bipolar Operation

The DAC101C081 is designed for single supply operation and thus has a unipolar output. However, a bipolar output may be obtained with the circuit in Figure 27. This circuit will provide an output voltage range of ±5 Volts. A rail-to-rail amplifier should be used if the amplifier supplies are limited to ±5 V.

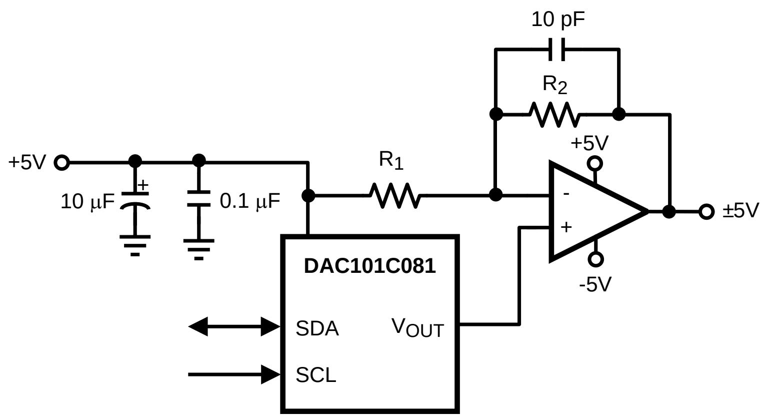


Figure 27. Bipolar Operation

The output voltage of this circuit for any code is found to be:

$$V_O = (V_A \times (D / 1024) \times ((R1 + R2) / R1) – V_A \times R2 / R1)$$

where *D* is the input code in decimal form. (2)

With V_A = 5 V and R1 = R2,

$$V_O = (10 \times D / 1024) – 5\ V \quad (3)$$

A list of rail-to-rail amplifiers suitable for this application are indicated in Table 2.

Table 2. Some Rail-to-Rail Amplifiers

AMP	PKGS	Typ V_{OS}	Typ I_{SUPPLY}
LMP7701	SOT-23-5	37 uV	0.79 mA
LMV841	SC70-5	50 uV	1 mA
LMC7111	SOT-23-5	0.9 mV	25 µA
LM7301	SO-8 SOT-23-5	0.03 mV	620 µA
LM8261	SOT-23-5	0.7 mV	1 mA

10.1.2 DSP/Microprocessor Interfacing

Interfacing the DAC101C081 to microprocessors and DSPs is quite simple. The following guidelines are offered to simplify the design process.

10.1.2.1 Interfacing to the 2-wire Bus

Figure 28 shows a microcontroller interfacing to the DAC101C081 via the 2-wire bus. Pullup resistors (Rp) should be chosen to create an appropriate bus rise time and to limit the current that will be sunk by the open-drain outputs of the devices on the bus. Please refer to the I^2C™ Specification for further details. Typical pullup values to use in Standard-Fast mode bus applications are 2kΩ to 10kΩ. SCL and SDA series resisters (R_S) near the DAC101C081 are optional. If high-voltage spikes are expected on the 2-wire bus, series resistors should be used to filter the voltage on SDA and SCL. The value of the series resistance must be picked to ensure the V_{IL} threshold can be achieved. If used, R_S is typically 51Ω.

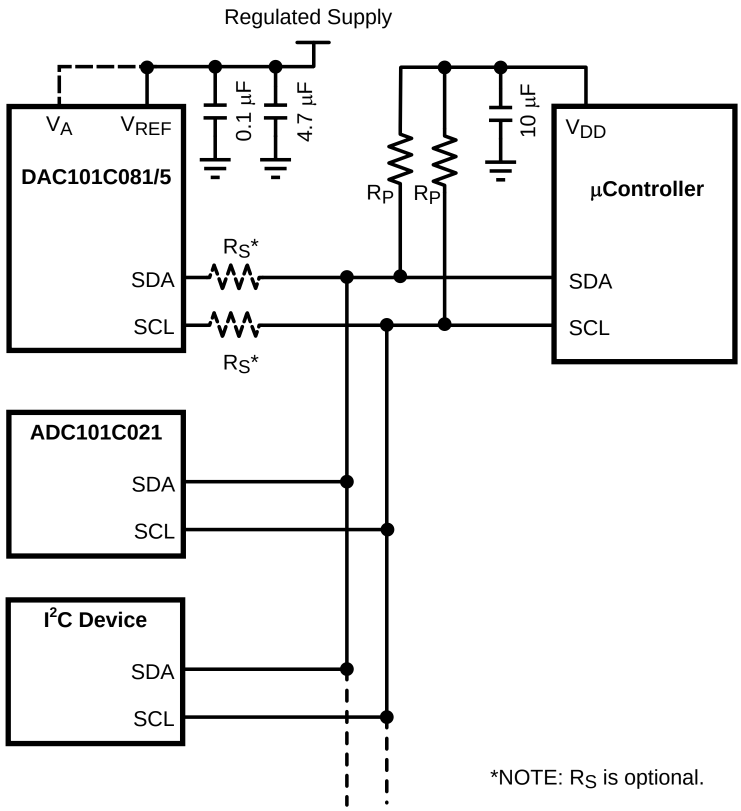


Figure 28. Serial Interface Connection Diagram

10.1.2.2 Interfacing to a Hs-mode Bus

Interfacing to a Hs-mode bus is very similar to interfacing to a standard-fast mode bus. In Hs-mode, the specified rise time of SCL is shortened. To create a faster rise time, the master device (microcontroller) can drive the SCL bus high and low. In other words, the microcontroller can drive the line high rather than leaving it to the pullup resistor. It is also possible to decrease the value of the pullup resistors or increase the pullup current to meet the tighter timing specs. Please refer to the I^2C Specification for further details.

10.2 Typical Application

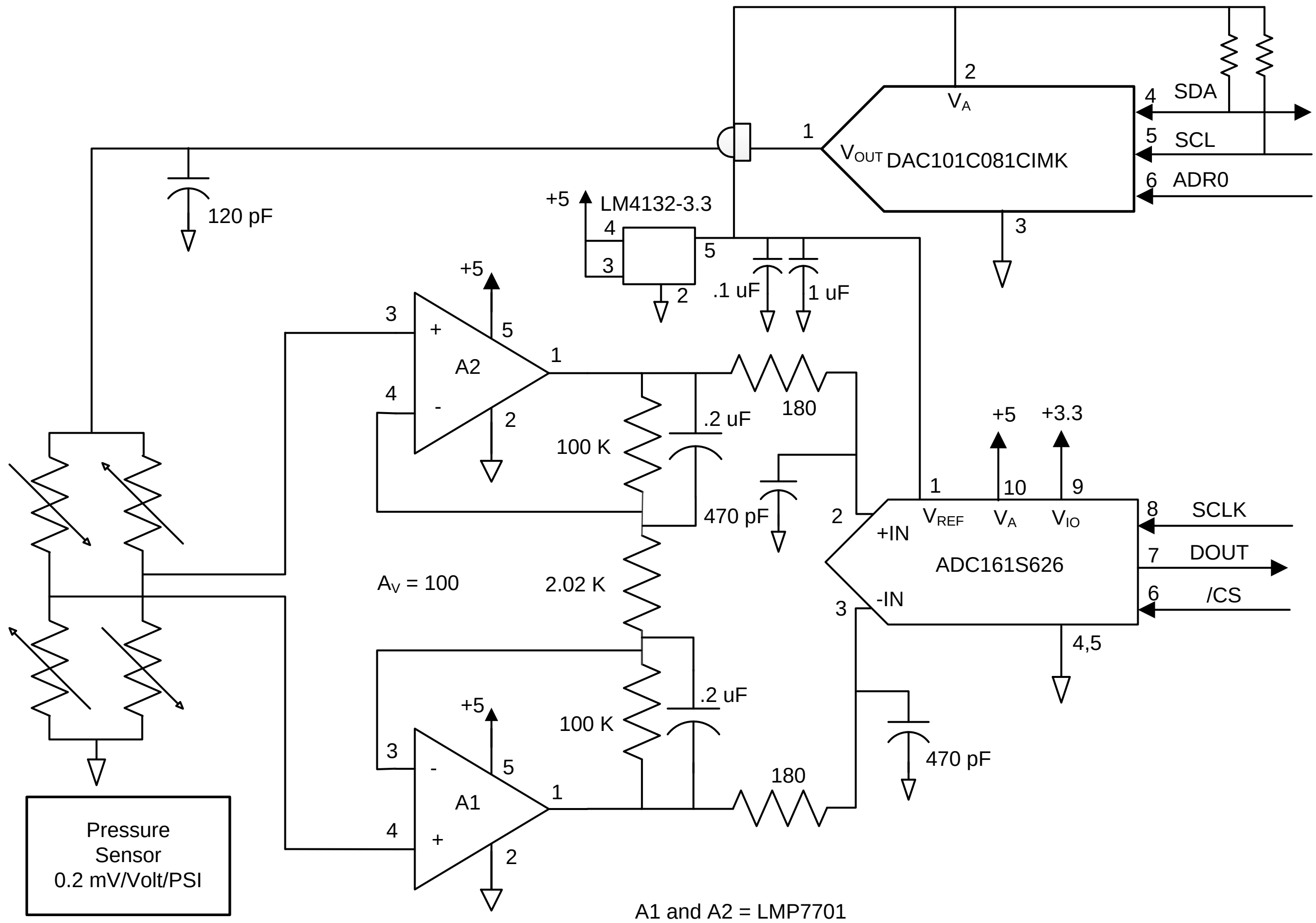


Figure 29. Pressure Sensor Gain Adjust

10.2.1 Design Requirements

A positive supply only data acquisition system capable of digitizing a pressure sensor output. In addition to digitizing the pressure sensor output, the system designer can use the DAC101C081 to correct for gain errors in the pressure sensor output by adjusting the bias voltage to the bridge pressure sensor.

10.2.2 Detailed Design Procedure

As shown in Equation 4, the output of the pressure sensor is relative to the imbalance of the resistive bridge times the output of the DAC101C081, thus providing the desired gain correction.

$$\text{Pressure Sensor Output} = (\text{DAC\_Output} \times [(R2 / (R1 + R2) – (R4 / (R3 + R4)] \quad (4)$$

Likewise for the ADC161S626, Equation 5 shows that the ADC output is function of the Pressure Sensor Output times relative to the ratio of the ADC input divided by the DAC101C081 output voltage.

$$\text{ADC161S626 Output} = (\text{Pressure Sensor Output} \times 100 /(2 \times \text{VREF})) \times 2^{16} \quad (5)$$

Typical Application (continued)

10.2.3 Application Curve

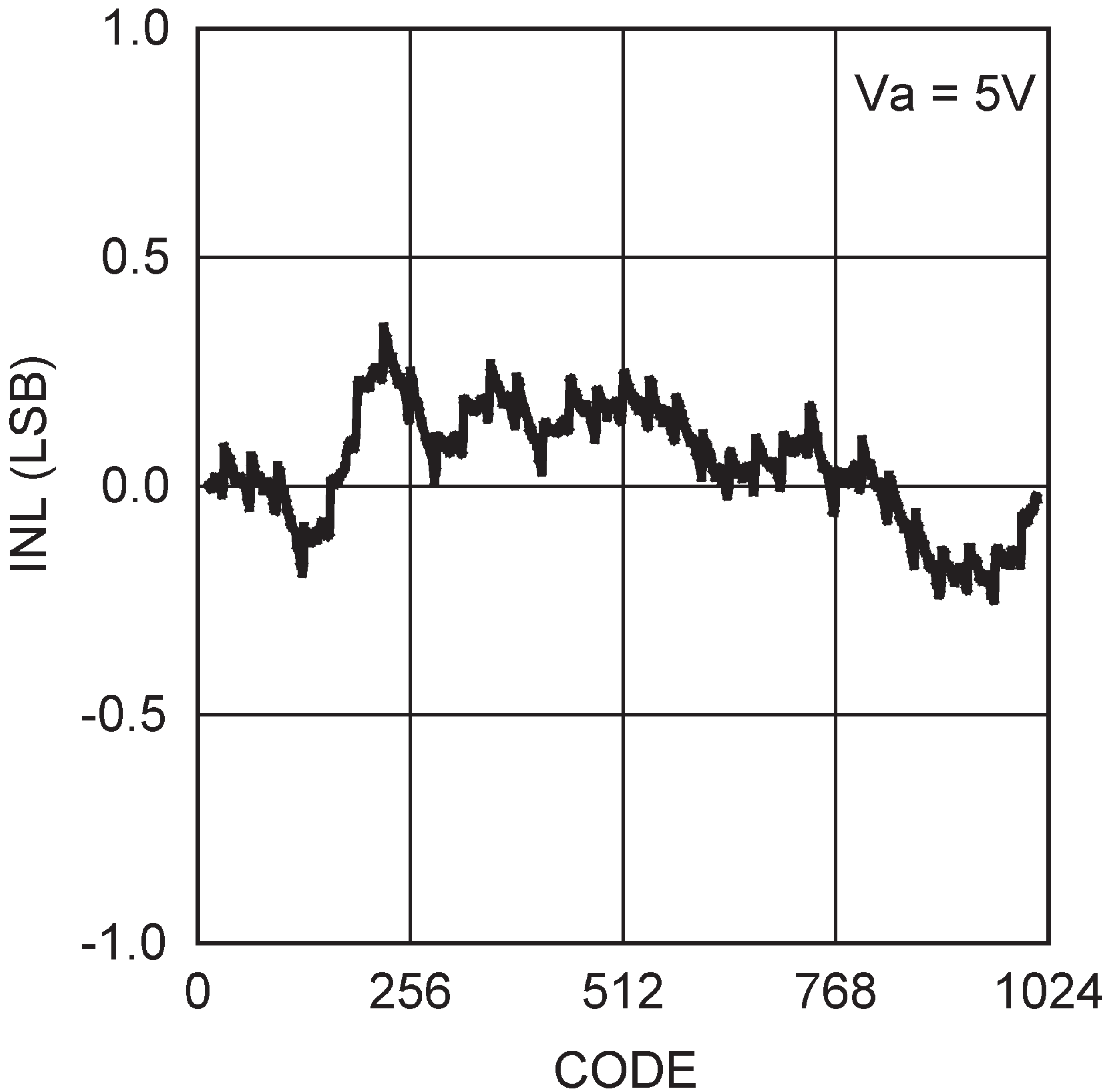


Figure 30. INL vs Input Code

11 Power Supply Recommendations

11.1 Using References as Power Supplies

While the simplicity of the DAC101C081 implies ease of use, it is important to recognize that the path from the reference input (V_A for the DAC101C081 and V_{REF} for the DAC101C085) to V_{OUT} will have essentially zero Power Supply Rejection Ratio (PSRR). Therefore, it is necessary to provide a noise-free supply voltage to the reference. In order to use the full dynamic range of the DAC101C085, the supply pin (V_A) and V_{REF} can be connected together and share the same supply voltage. Since the DAC101C081 consumes very little power, a reference source may be used as the supply voltage. To ensure accuracy, it is required that V_A and V_{REF} be well bypassed. The advantages of using a reference source over a voltage regulator are accuracy and stability. Some low noise regulators can also be used. Listed below are a few reference and power supply options for the DAC101C081. When using the DAC101C081, it is important to treat the analog supply (V_A) as the reference.

11.1.1 LM4132

The LM4132, with its 0.05% accuracy over temperature, is a good choice as a reference source for the DAC101C081. The 4.096-V version is useful if a 0 to 4.095-V output range is desirable or acceptable. Bypassing the LM4132 V_{IN} pin with a 0.1-μF capacitor and the V_{OUT} pin with a 2.2-μF capacitor will improve stability and reduce output noise. The LM4132 comes in a space-saving 5-pin SOT-23.

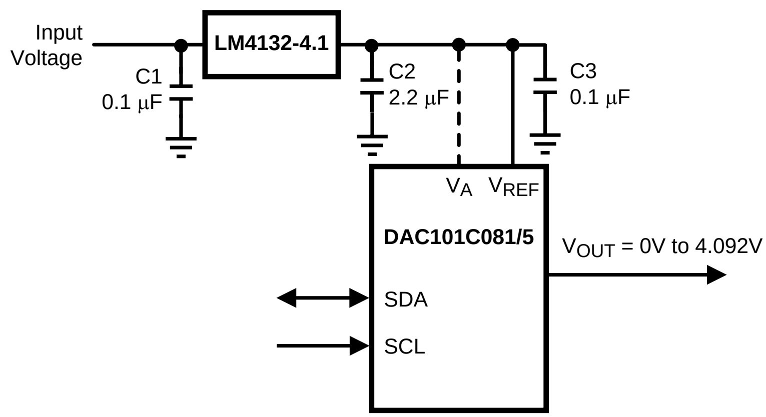


Figure 31. The LM4132 as a Power Supply

Using References as Power Supplies (continued)

11.1.2 LM4050

Available with accuracy of 0.44%, the LM4050 shunt reference is also a good choice as a reference for the DAC101C081. It is available in 4.096-V and 5-V versions and comes in a space-saving 3-pin SOT-23.

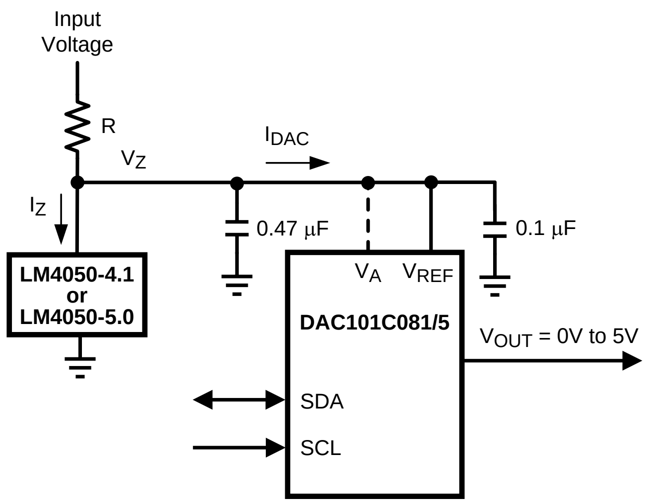


Figure 32. The LM4050 as a Power Supply

The minimum resistor value in the circuit of Figure 32 must be chosen such that the maximum current through the LM4050 does not exceed its 15-mA rating. The conditions for maximum current include the input voltage at its maximum, the LM4050 voltage at its minimum, and the DAC101C081 drawing zero current. The maximum resistor value must allow the LM4050 to draw more than its minimum current for regulation plus the maximum DAC101C081 current in full operation. The conditions for minimum current include the input voltage at its minimum, the LM4050 voltage at its maximum, the resistor value at its maximum due to tolerance, and the DAC101C081 draws its maximum current. These conditions can be summarized as:

$$R(min) = (V_{IN}(max) - V_Z(min)) / I_Z(max) \quad (6)$$

and

$$R(max) = (V_{IN}(min) - V_Z(max)) / ((I_{DAC}(max) + I_Z(min))$$

where

- V_Z(min) and V_Z(max) are the nominal LM4050 output voltages ± the LM4050 output tolerance over temperature
- I_Z(max) is the maximum allowable current through the LM4050
- I_Z(min) is the minimum current required by the LM4050 for proper regulation and
- I_{DAC}(max) is the maximum DAC101C081 supply current. (7)

Using References as Power Supplies (continued)

11.1.3 LP3985

The LP3985 is a low noise, ultra low dropout voltage regulator with a 3% accuracy over temperature. It is a good choice for applications that do not require a precision reference for the DAC101C081. It comes in 3.0-V, 3.3-V and 5-V versions, among others, and sports a low 30-µV noise specification at low frequencies. Because low frequency noise is relatively difficult to filter, this specification could be important for some applications. The LP3985 comes in a space-saving 5-pin SOT-23 and 5-bump DSBGA packages.

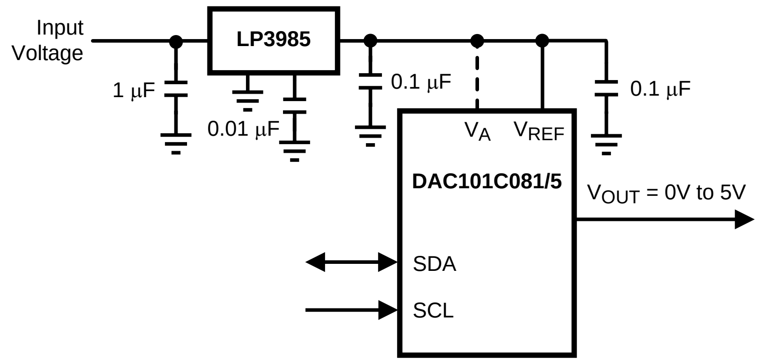


Figure 33. Using the LP3985 Regulator

An input capacitance of 1.0 µF without any ESR requirement is required at the LP3985 input, while a 1.0-µF ceramic capacitor with an ESR requirement of 5 mΩ to 500 mΩ is required at the output. Careful interpretation and understanding of the capacitor specification is required to ensure correct device operation.

11.1.4 LP2980

The LP2980 is an ultra low dropout regulator with a 0.5% or 1.0% accuracy over temperature, depending upon grade. It is available in 3.0-V, 3.3-V and 5-V versions, among others.

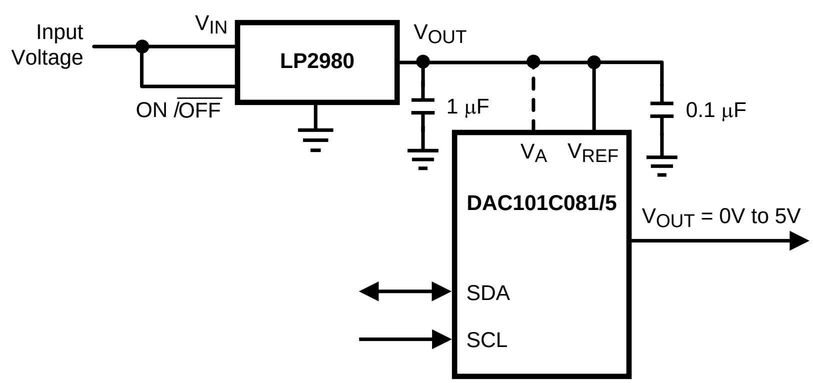


Figure 34. Using the LP2980 Regulator

Like any low dropout regulator, the LP2980 requires an output capacitor for loop stability. This output capacitor must be at least 1.0µF over temperature, but values of 2.2µF or more will provide even better performance. The ESR of this capacitor should be within the range specified in the LP2980 data sheet. Surface-mount solid tantalum capacitors offer a good combination of small size and ESR. Ceramic capacitors are attractive due to their small size but generally have ESR values that are too low for use with the LP2980. Aluminum electrolytic capacitors are typically not a good choice due to their large size and have ESR values that may be too high at low temperatures.

12 Layout

12.1 Layout Guidelines

For best accuracy and minimum noise, the printed circuit board containing the DAC101C081 requires separate analog and digital areas. The areas are defined by the locations of the analog and digital power planes. Both of these planes should be located on the same board layer. There should be a single ground plane. A single ground plane is preferred if digital return current does not flow through the analog ground area. Frequently a single ground plane design will use a *fencing* technique to prevent the mixing of analog and digital ground current. Separate ground planes should only be utilized when the fencing technique is inadequate. The separate ground planes must be connected in one place, preferably near the DAC101C081. Special care is required to ensure that digital signals with fast edge rates do not pass over split ground planes. They must always have a continuous return path below their traces.

The DAC101C081 power supply should be bypassed with a 4.7-µF and a 0.1-µF capacitor as close as possible to the device with the 0.1 µF right at the device supply pin. The 4.7-µF capacitor should be a tantalum type and the 0.1-µF capacitor should be a low ESL, low ESR type. The power supply for the DAC101C081 should only be used for analog circuits.

Avoid crossover of analog and digital signals and keep the clock and data lines on the component side of the board. These clock and data lines require controlled impedances.

12.2 Layout Example

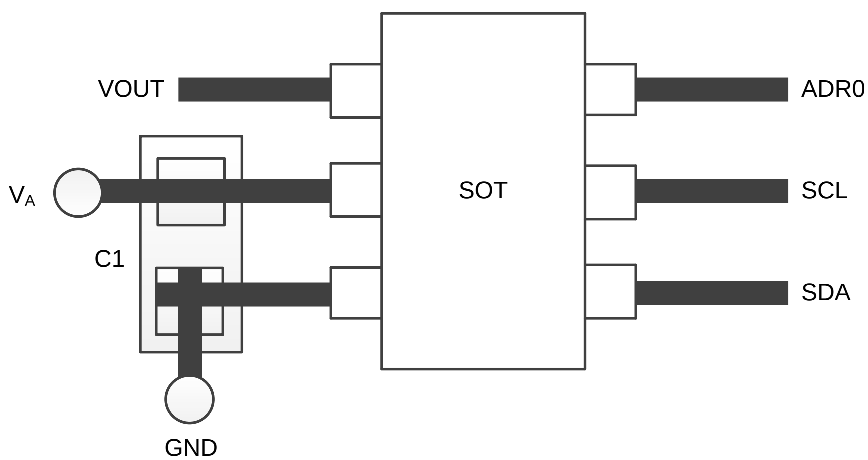


Figure 35. Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 器件命名规则

13.1.1.1 技术规格定义

微分非线性 **(DNL)** 是指与理想步长宽度 (1 LSB) 之间的最大偏差，即 V_{REF} / 1024 = V_A / 1024。

数字馈通是指 DAC 输出未更新时从数字输入注入 DAC 模拟输出的能量。测量时使用数据总线上的满量程编码变化。

满量程误差是指 DAC 中装载满量程编码 (FFFh) 时的实际输出电压与 V_A x 1023 / 1024 的值之差。

增益误差是指与传递函数理想斜率之间的偏差。增益误差可使用零码误差和满量程误差来计算，公式如下：

GE = FSE - ZE

其中

- GE 为增益误差
- FSE 为满量程误差
- ZE 为零码误差。 (8)

毛刺脉冲是指 DAC 寄存器的输入编码发生变化时注入模拟输出的能量。它表示为毛刺脉冲面积，以毫微伏秒为单位。

积分非线性 **(INL)** 是指每个独立代码与通过输入输出传递函数的直线之间的偏差。任意指定编码与这条直线的偏差都是从该编码值的中心测量的。测量时使用的是端点方法。根据*电气特性表*，该产品的 INL 规定在一个有限范围内。

最低有效位 **(LSB)** 是指一个字的所有位中具有最小值或最低权重的位。该值为

LSB = V_{REF} / 2^n

其中

- V_{REF} 是此产品的电源电压，“n”是 DAC 的分辨率（以位为单位，DAC101C081 为 10）。 (9)

最大负载电容是指在保持输出稳定性的前提下 DAC 可驱动的最大电容。

单调性是一种单调的状态。在这种状态下，当输入编码增加时，DAC 的输出从不减少。

最高有效位 **(LSB)** 是指一个字的所有位中具有最大值或最高权重的位。其值为 V_A 的 1/2。

增值带宽是指 DAC 中装载满量程编码后输出幅值降至 V_{REFIN} 上的输入正弦波的 3dB 以下时所处的频率。

功率效率是输出电流与总电源电流之比。输出电流来自电源。电源电流与输出电流之差为器件的无载功耗。

稳定时间是指输入编码更新后输出稳定在最终值的 1/2 LSB 以内所需的时间。

总谐波失真 **(THD)** 是指对 V_{REFIN} 施加理想正弦波时 DAC 的输出端存在的谐波。THD 以 dB 为单位。

唤醒时间是指输出退出省电模式所需的时间。该时间从较低数据字节的 ACK 位期间的 SCL 上升沿开始，到输出电压与省电电压的偏差为零时结束。

零码误差是指输入 000h 编码后 DAC 输出端存在的输出误差或电压。

13.2 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **3.** 相关链接

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
DAC101C081	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
DAC101C081Q	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

相关链接 (接下页)

表 **3.** 相关链接 **(**接下页**)**

器件	产品文件夹	样片与购买	技术文章	工具与软件	支持与社区
DAC101C085	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 商标

E2E is a trademark of Texas Instruments.
I²C is a trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

13.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC101C081CIMK/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X85C	Samples
DAC101C081CIMKX/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X85C	Samples
DAC101C081CISD/NOPB	ACTIVE	WSON	NGF	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM		X88	Samples
DAC101C081CISDX/NOPB	ACTIVE	WSON	NGF	6	4500	RoHS & Green	SN	Level-1-260C-UNLIM		X88	Samples
DAC101C081QISD/NOPB	ACTIVE	WSON	NGF	6	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	Q88	Samples
DAC101C081QISDX/NOPB	ACTIVE	WSON	NGF	6	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	Q88	Samples
DAC101C085CIMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		X91C	Samples
DAC101C085CIMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	X91C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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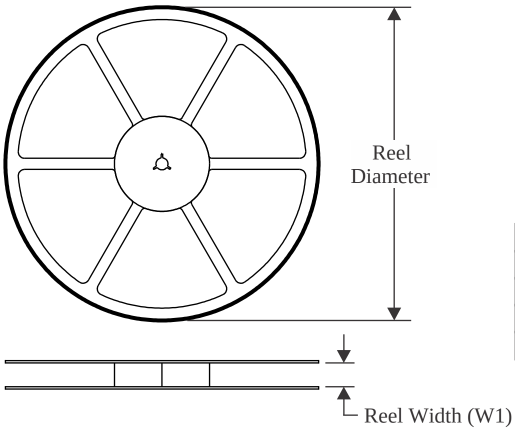
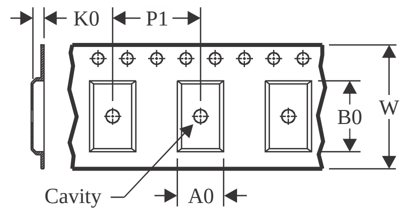
TAPE AND REEL INFORMATION

REEL DIMENSIONS

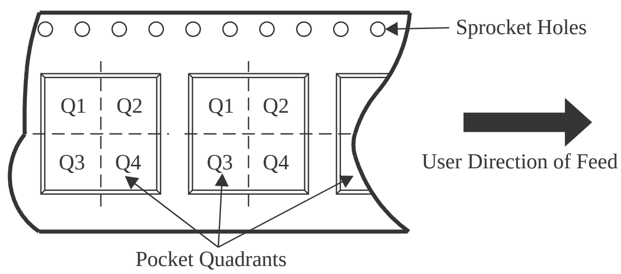


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

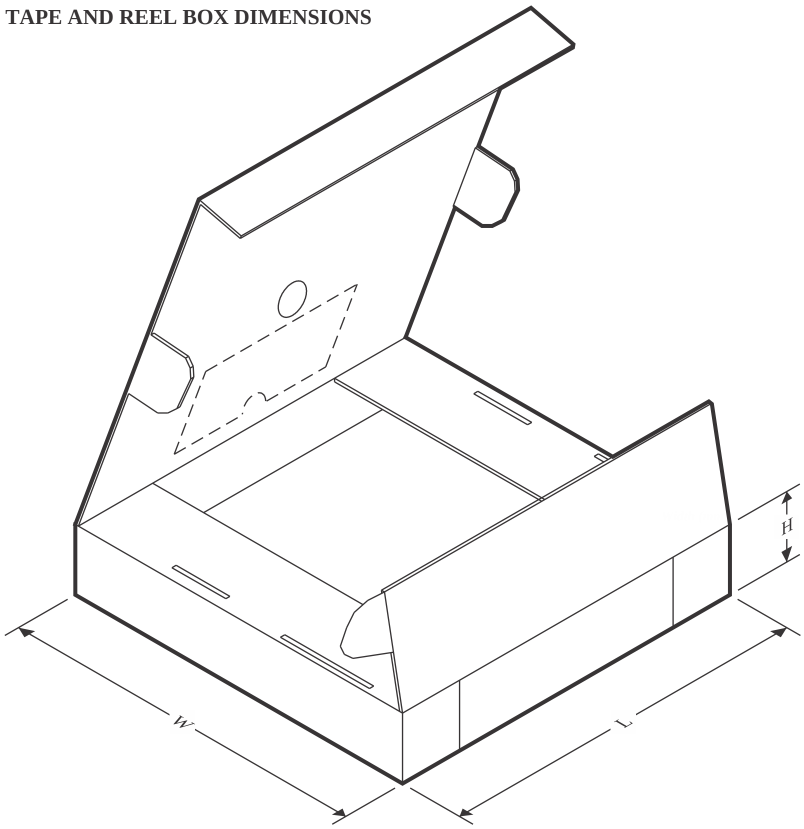
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

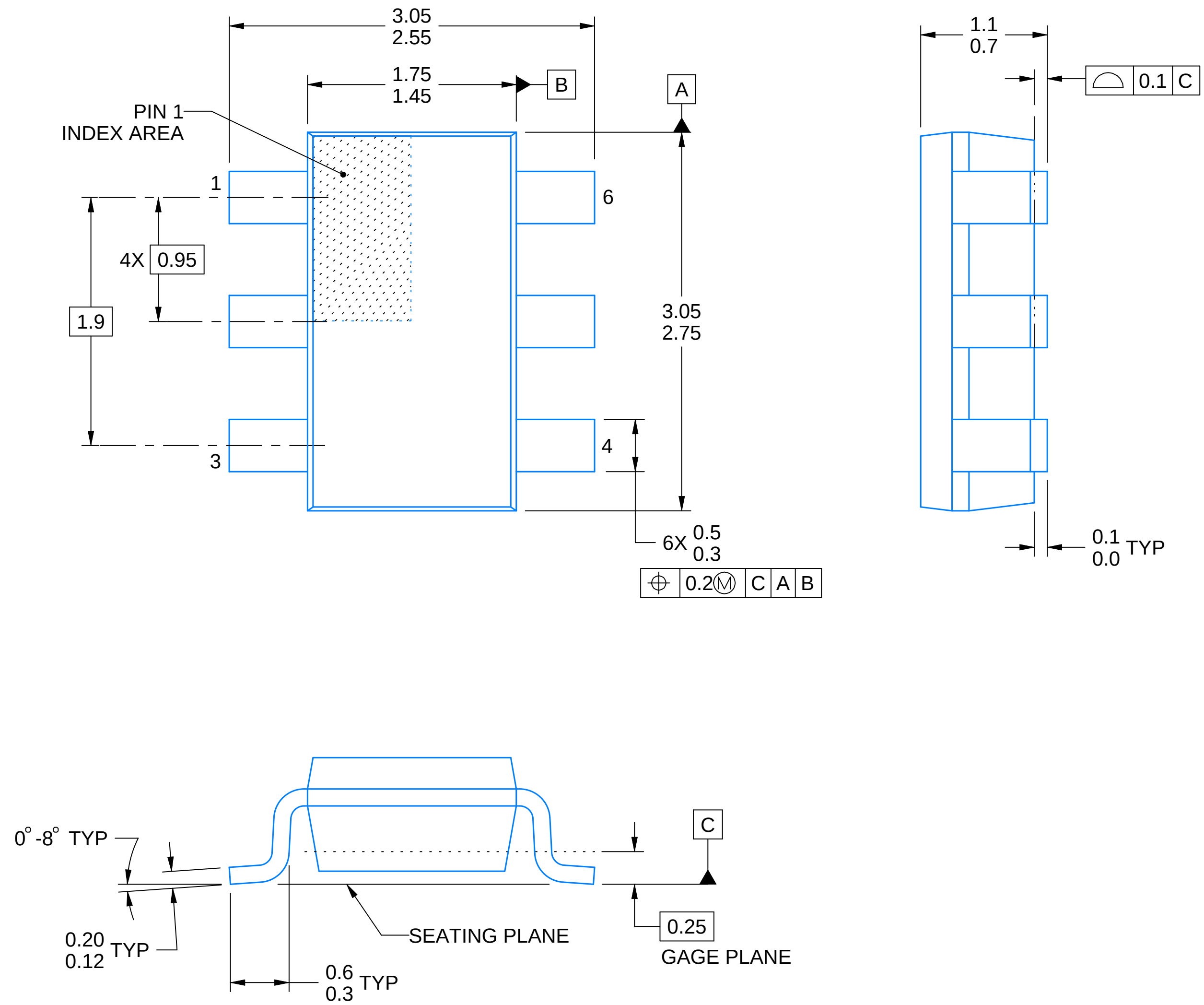
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC101C081CIMK/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC101C081CIMKX/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
DAC101C081CISD/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC101C081CISDX/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC101C081QISD/NOPB	WSON	NGF	6	1000	178.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC101C081QISDX/NOPB	WSON	NGF	6	4500	330.0	12.4	2.8	2.5	1.0	8.0	12.0	Q1
DAC101C085CIMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
DAC101C085CIMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC101C081CIMK/NOPB	SOT-23-THIN	DDC	6	1000	210.0	185.0	35.0
DAC101C081CIMKX/ NOPB	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
DAC101C081CISD/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
DAC101C081CISDX/ NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
DAC101C081QISD/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0
DAC101C081QISDX/ NOPB	WSON	NGF	6	4500	367.0	367.0	35.0
DAC101C085CIMM/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
DAC101C085CIMMX/ NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0



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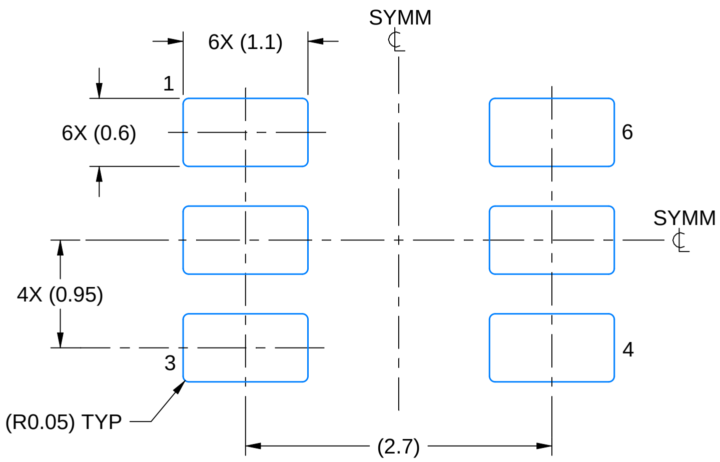
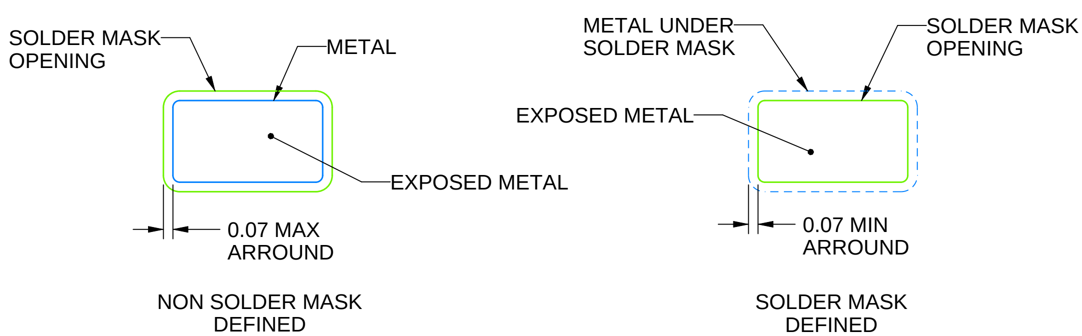
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

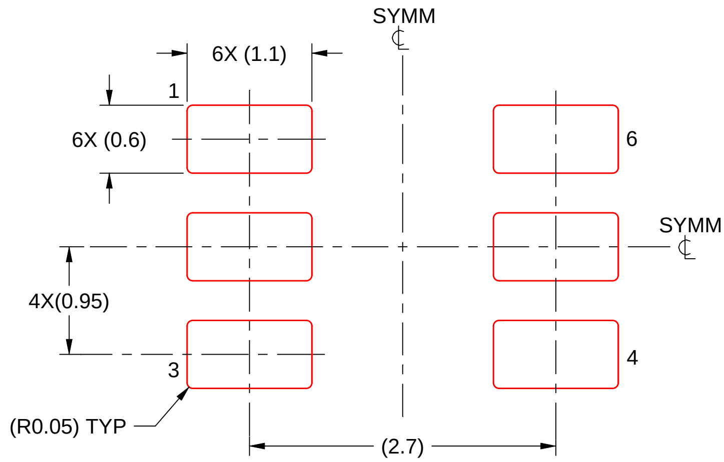


SOLDERMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

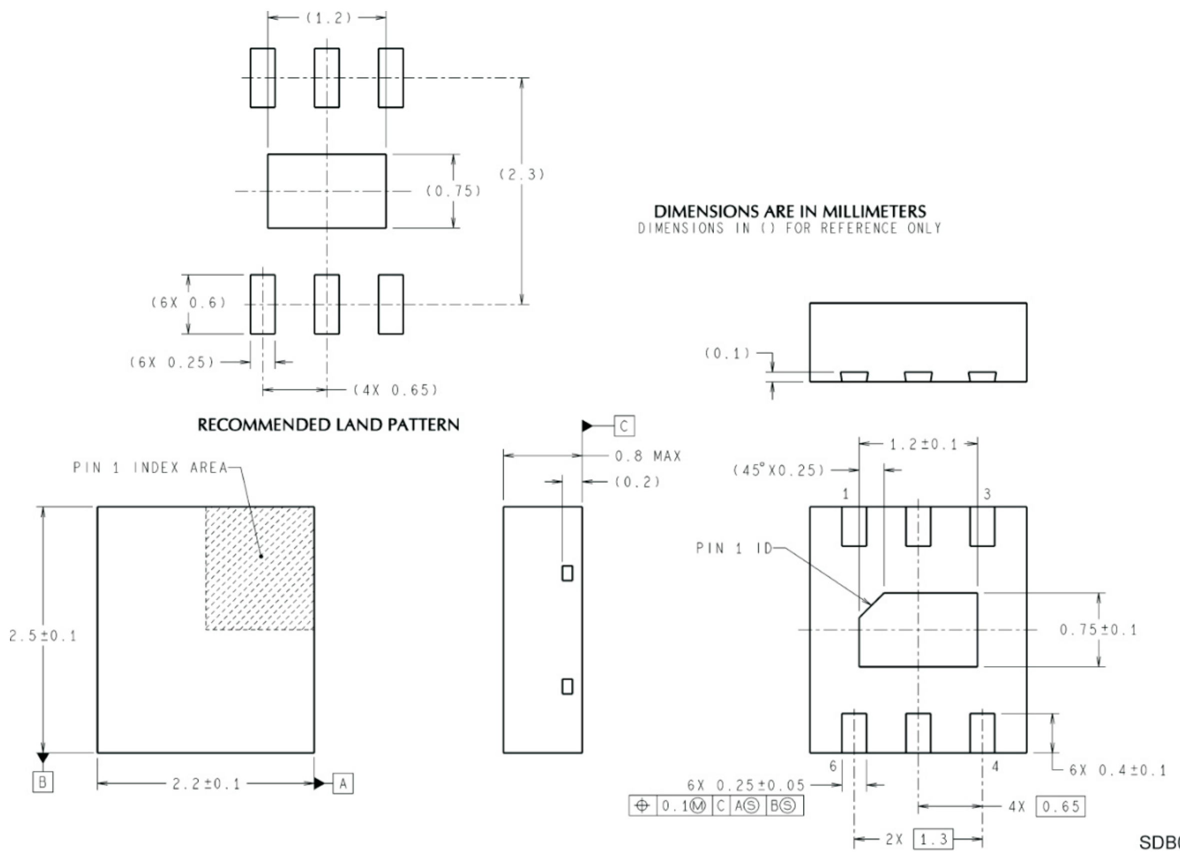


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

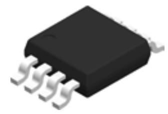
4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.


(1.2)
(2.3)
(0.75)
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(6X 0.6)
(6X 0.25)
(4X 0.65)
(0.1)
RECOMMENDED LAND PATTERN
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
PIN 1 INDEX AREA
1
3
PIN 1 ID
2.5±0.1
0.75±0.1
6
4
6X 0.4±0.1
B
2.2±0.1
A
6X 0.25±0.05
0.1 M C A S B S
4X 0.65
2X 1.3

SDB06A (Rev A)

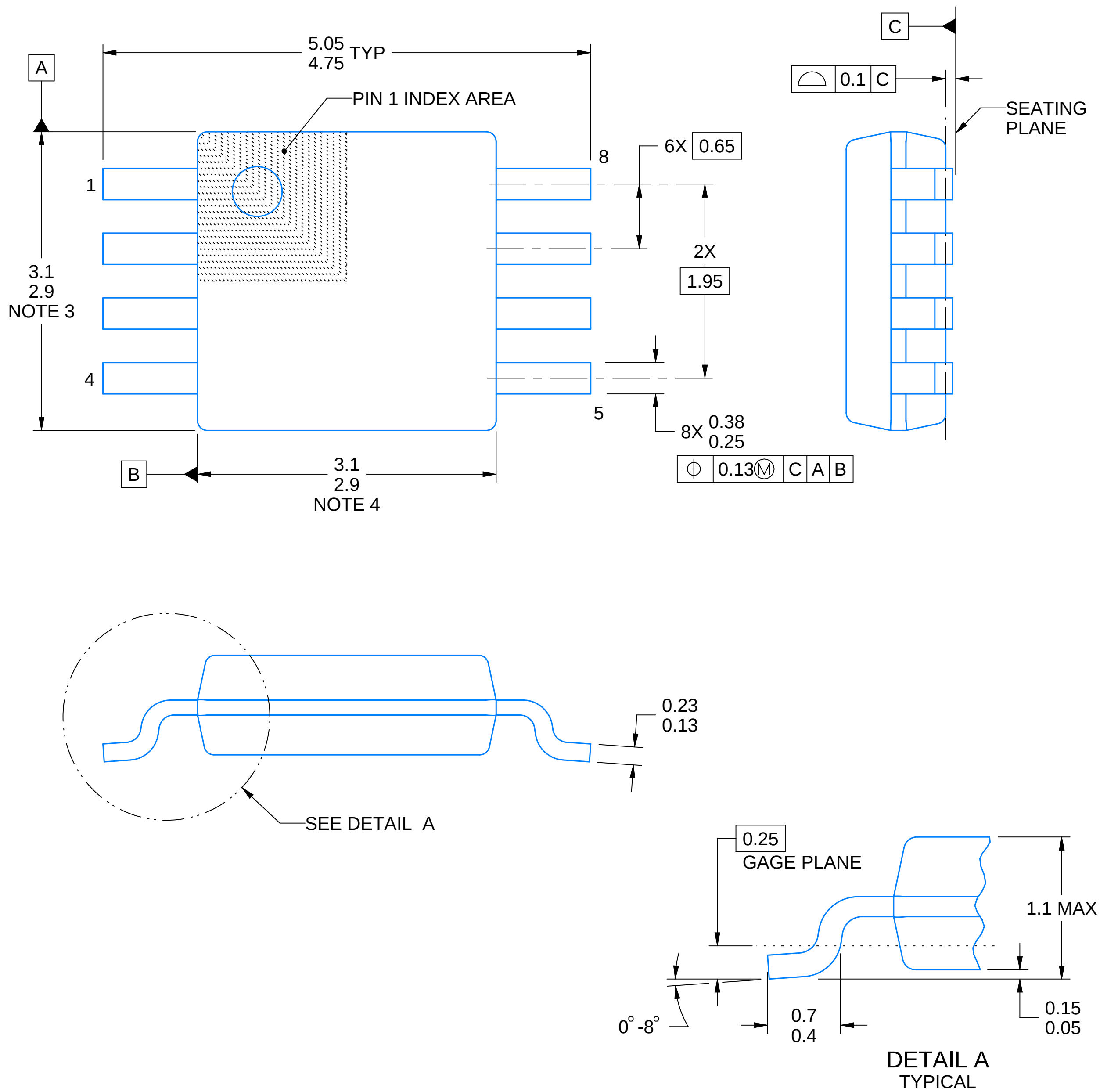


PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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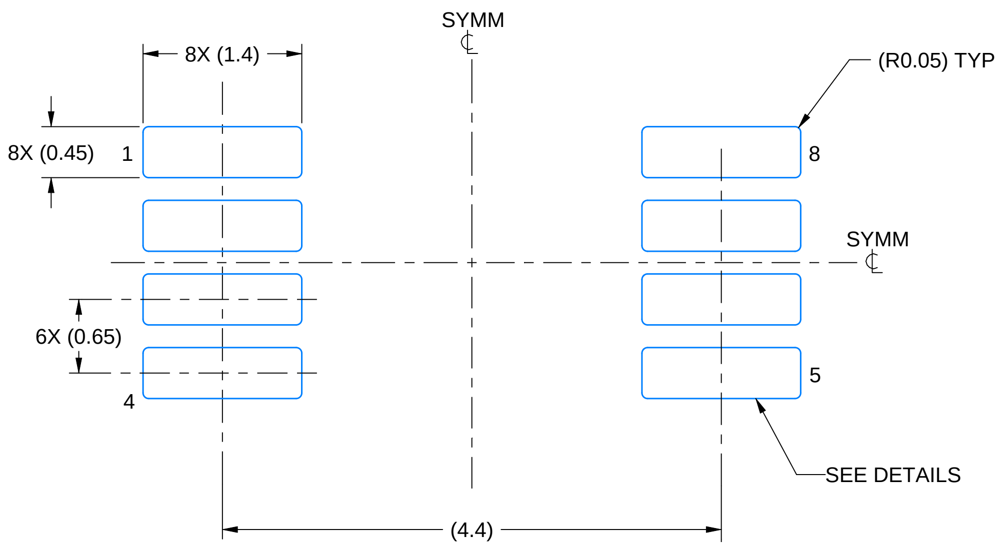
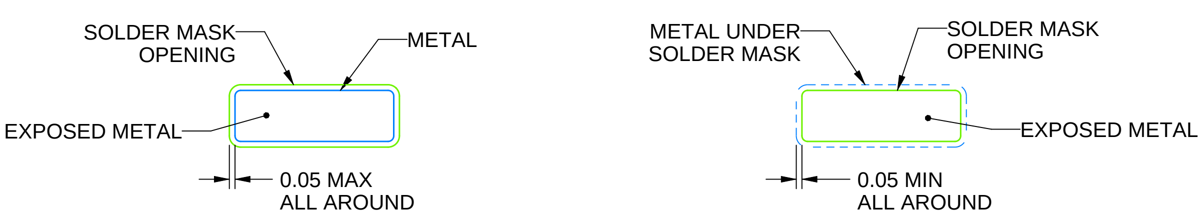
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK DEFINED (PREFERRED)

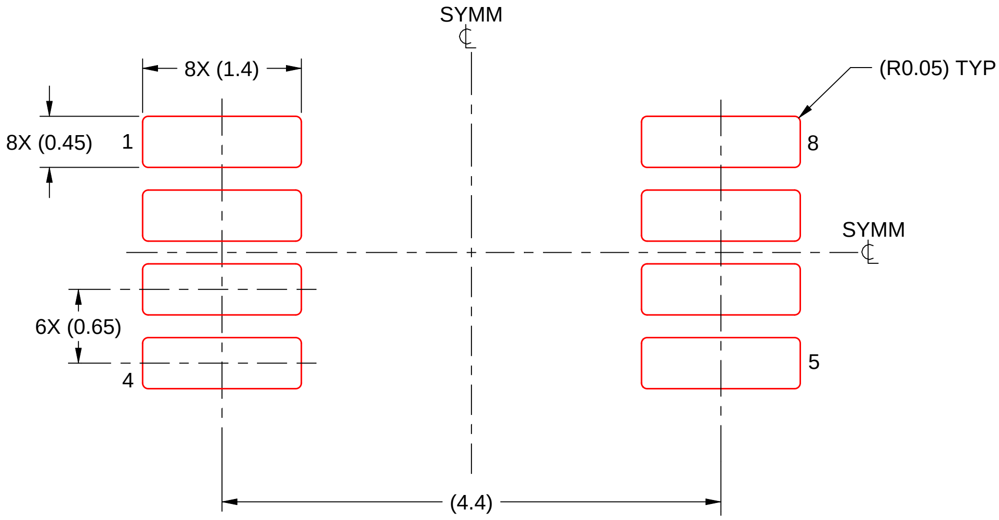
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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