TEXAS INSTRUMENTS
UCC27321, UCC27322, UCC37321, UCC37322
ZHCSTX9I – SEPTEMBER 2002 – REVISED NOVEMBER 2023

UCC2732x/UCC3732x 具有使能功能的单路 9A 高速低侧 MOSFET 驱动器

1 特性

- 业界通用引脚排列，具有额外使能功能
- 使用 TrueDrive 在米勒平坦区域提供 ±9A 的高峰值电流驱动能力
- 使用独特的双极和 CMOS 输出级实现高效恒流源
- 与电源电压无关的 TTL/CMOS 兼容输入
- 10nF 负载时的上升时间和下降时间典型值为 20ns
- 输入下降和上升时的典型传播延迟时间分别为 25ns 和 35ns
- 4V 至 15V 电源电压
- 采用热增强型 MSOP PowerPAD™ 封装，具有 4.7°C/W θjc
- 额定温度为 -40°C 至 +105°C
- 8 引脚 SOIC 和 PDIP 封装上的无铅表面处理 (CU NIPDAU)

2 应用

- 开关模式电源
- 直流/直流转换器
- 电机控制器
- D 类开关放大器
- 线路驱动器
- 脉冲变压器驱动器

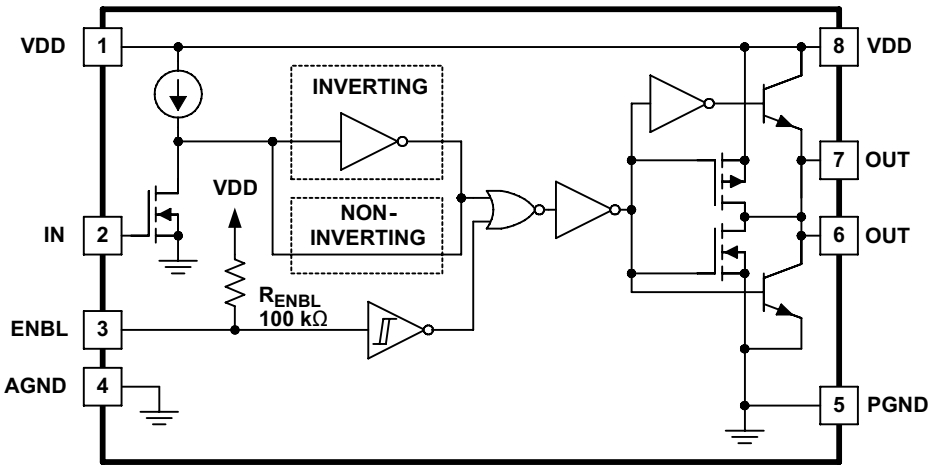
3 说明

UCC2732x/UCC3732x 系列高速驱动器在业界通用引脚排列中提供 9A 峰值驱动电流。这些驱动器可以为由于高 dV/dt 转换而需要极端米勒电流的系统驱动最大 MOSFET。这样无需额外的外部电路，并且可以替换多个元件，以减少空间，降低设计复杂性和组装成本。提供两种标准逻辑选项：反相 (UCC37321) 和同相 (UCC37322)。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
UCC2732x UCC3732x	MSOP-PowerPAD (8)	3.00mm × 3.00mm
	SOIC (8)	3.91mm × 4.90mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



方框图

Table of Contents

4 说明（续）

通过使用本身能够更大限度减少击穿电流的设计，这些器件的输出可以在 MOSFET 开关切换期间，在米勒平坦区域最需要的地方提供高栅极驱动电流。独特的混合输出级并联双极和 MOSFET 晶体管 (TrueDrive)，可在低电源电压下高效输送电流。通过此驱动架构，UCC3732x 可用于业界通用 6A、9A 和许多 12A 驱动器应用。还包括闩锁和 ESD 保护电路。最后，UCC3732x 提供了使能 (ENBL) 功能，以更好地控制驱动器应用的运行。ENBL 在引脚 3 上实现，该引脚之前在业界通用引脚排列中未使用。它内部上拉至 V_{DD} 电源以实现高电平有效逻辑运行，并且可保持断开连接状态以实现标准运行。

除了 8 引脚 SOIC (D) 封装产品外，UCC3732x 还采用热增强型微型 8 引脚 MSOP PowerPAD™ (DGN) 封装。PowerPAD 封装大幅降低了热阻，从而扩大了工作温度范围并提高了长期可靠性。

5 Related Products

PRODUCT	DESCRIPTION	PACKAGES
UCC37323/4/5	Dual 4-A Low-Side Drivers	MSOP – 8 PowerPAD, SOIC – 8, PDIP – 8
UCC27423/4/5	Dual 4-A Low-Side Drivers with Enable	MSOP – 8 PowerPAD, SOIC – 8, PDIP – 8
TPS2811/12/13	Dual 2-A Low-Side Drivers with Internal Regulator	TSSOP – 8, SOIC – 8, PDIP – 8
TPS2814/15	Dual 2-A Low-Side Drivers with Two Inputs per Channel	TSSOP – 8, SOIC – 8, PDIP – 8
TPS2816/17/18/19	Single 2-A Low-Side Driver with Internal Regulator	5-Pin SOT – 23
TPS2828/29	Single 2-A Low-Side Driver	5-Pin SOT – 23

6 Pin Configuration and Functions

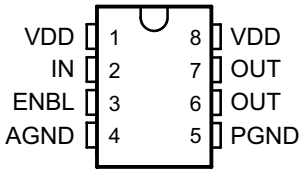


图 6-1. D, and DGN Packages 8-Pin SOIC, and MSOP With PowerPAD Top View

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	4	—	The AGND and the PGND must be connected by a single thick trace directly under the device. There must be a low ESR, low ESL capacitor of 0.1 µF between VDD (pin 8) and PGND and a separate 0.1-µF capacitor between VDD (pin 1) and AGND. The power MOSFETs must be located on the PGND side of the device while the control circuit must be on the AGND side of the device. The control circuit ground must be common with the AGND while the PGND must be common with the source of the power FETs.
ENBL	3	I	Enable input for the driver with logic compatible threshold and hysteresis. The driver output can be enabled and disabled with this pin. It is internally pulled up to V_{DD} with 100-kΩ resistor for active high operation. When the device is disabled, the output state is, low regardless of the input state.
IN	2	I	Input signal of the driver which has logic compatible threshold and hysteresis.
OUT	6, 7	O	Driver outputs that must be connected together externally. The output stage is capable of providing 9-A peak drive current to the gate of a power MOSFET.
PGND	5	—	Common ground for output stage. This ground must be connected very closely to the source of the power MOSFET which the driver is driving. Grounds are separated to minimize ringing affects due to output switching di/dt which can affect the input threshold.
VDD	1, 8	I	Supply voltage and the power input connections for this device. Two pins must be connected together externally.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Supply voltage, V_{DD}		– 0.3	16	V
Output current (OUT) DC, I_{OUT_DC}			0.6	A
Input voltage (IN), V_{IN}		– 0.3	6 V or V_{DD} + 0.3 (3)	V
Enable voltage (ENBL)		– 0.3	6 V or V_{DD} + 0.3 (3)	V
Power dissipation at T_A = 25°C	D package		650	mW
	DGN package		3	W
	P package		350	mW
Lead temperature (soldering, 10 s)			300	°C
Junction operating temperature, T_J		– 55	150	°C
Storage temperature, T_{stg}		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *节 7.3Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
(3) Whichever is larger

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, VDD	4.5		15	V

7.4 Thermal Information

THERMAL METRIC (1)		UCC27322	UCC27321		UNIT
		D (SOIC)	P (PDIP)	DGN (MSOP-PowerPAD)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.6	55.9	56.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	45.3	52.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.6	32.6	32.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	23.0	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	32.3	32.5	32.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.9	—	5.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{DD} = 4.5 V to 15 V, T_A = – 40°C to +105°C for UCC2732x, T_A = 0°C to 70°C for UCC3732x, $T_A = T_J$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT (IN)						
V_{IN_H}, logic 1 input threshold			1.6	2.2	2.5	V
V_{IN_L}, logic 0 input threshold			0.8	1.2	1.5	V
Input current		0 V ≤ V_{IN} ≤ V_{DD}	– 10	0	10	µA
OUTPUT (OUT)						
Peak output current(1)		V_{DD} = 14 V,		9		A
Output resistance high(2)		I_{OUT} = – 10 mA		0.6	1.5	Ω
Output resistance low(2)		I_{OUT} = 10 mA		0.4	1	Ω
OVERALL						
I_{DD}, static operating current	UCC37321 UCC27321	IN = LOW, EN = LOW, V_{DD} = 15 V		150	225	µA
		IN = HIGH, EN = LOW, V_{DD} = 15 V		440	650	
		IN = LOW, EN = HIGH, V_{DD} = 15 V		370	550	
		IN = HIGH, EN = HIGH, V_{DD} = 15 V		370	550	
	UCC37322 UCC27322	IN = LOW, EN = LOW, V_{DD} = 15 V		150	225	
		IN = HIGH, EN = LOW, V_{DD} = 15 V		450	650	
		IN = LOW, EN = HIGH, V_{DD} = 15 V		75	125	
		IN = HIGH, EN = HIGH, V_{DD} = 15 V		675	1000	
ENABLE (ENBL)						
V_{EN_H}, high-level enable voltage		LOW to HIGH transition	1.7	2.2	2.7	V
V_{EN_L}, low-level enable voltage		HIGH to LOW transition	1.1	1.6	2	V
Hysteresis			0.25	0.55	0.90	
R_{ENBL}, enable impedance		V_{DD} = 14 V, ENBL = GND	75	100	135	kΩ

(1) Not tested in production.
(2) Output pullup resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure.

7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

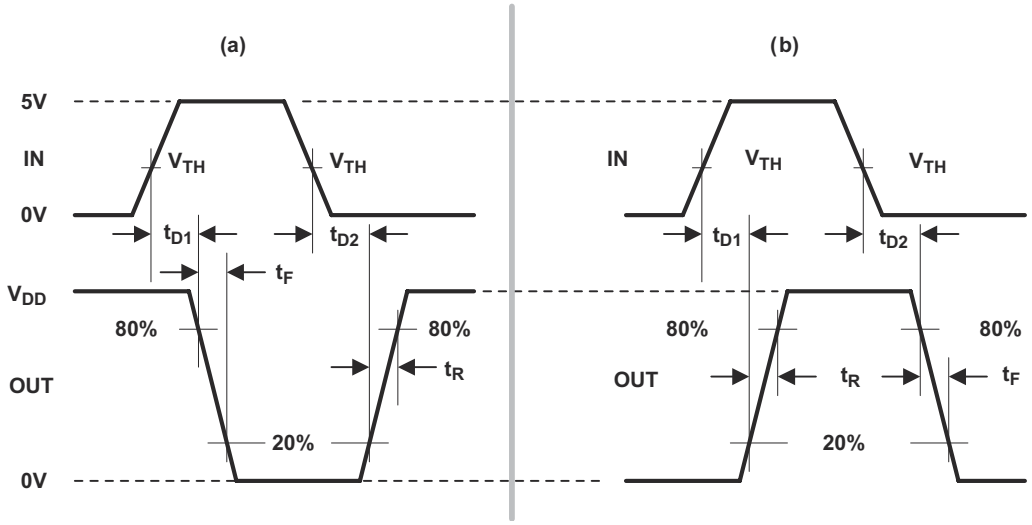
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE (ENBL)					
t_{D3}, propagation delay time(1)	C_{LOAD} = 10 nF		60	90	ns
t_{D4}, propagation delay time(1)	C_{LOAD} = 10 nF		60	90	ns
SWITCHING TIME(2)					
t_R, rise time (OUT)	C_{LOAD} = 10 nF		20	70	ns
t_F, fall time (OUT)	C_{LOAD} = 10 nF		20	30	ns
t_{D1}, propagation delay, IN rising (IN to OUT)	C_{LOAD} = 10 nF		25	70	ns
t_{D2}, propagation delay, IN falling (IN to OUT)	C_{LOAD} = 10 nF		35	70	ns

(1) See 图 7-2.
(2) See 图 7-1 for switching waveforms.

7.7 Power Dissipation Ratings

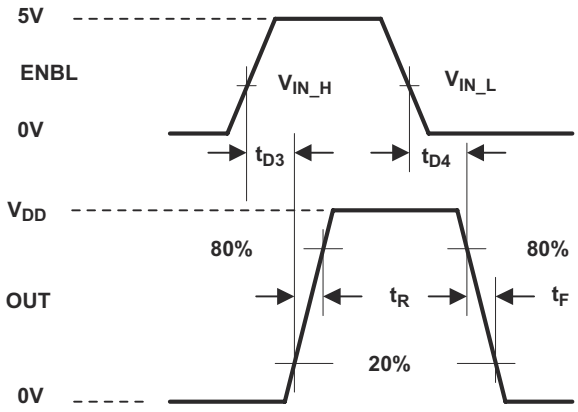
PACKAGE	SUFFIX	θ jc (°C/W)	θ ja (°C/W)	Power Rating (mW) T_A = 70°C(1)	Derating Factor Above 70°C (mW/°C)(1)
SOIC-8	D	42	84 to 160(2)	344 to 655(2)	6.25 to 11.9(2)
MSOP PowerPAD-8	DGN	4.7	50 to 59	1370	17.1

(1) 125°C operating junction temperature is used for power rating calculations
(2) The range of values indicates the effect of the printed-circuit-board. These values are intended to give the system designer an indication of the best and worst case conditions. In general, the system designer should attempt to use larger traces on the printed-circuit-board where possible to spread the heat away form the device more effectively. For additional information on device temperature management, see the *Packaging Information* section of the *Power Supply Control Products Data Book*, (SLUD003).



The 20% and 80% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

图 7-1. Switching Waveforms for (a) Inverting Input to (b) Output Times



The 20% and 80% thresholds depict the dynamics of the BiPolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

图 7-2. Switching Waveform for Enable to Output

7.8 Typical Characteristics

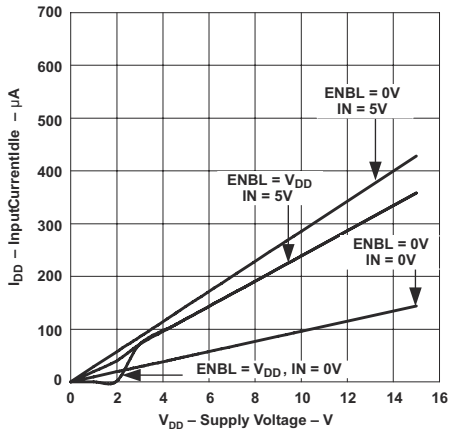


图 7-3. Input Current Idle vs Supply Voltage (UCCx7321)

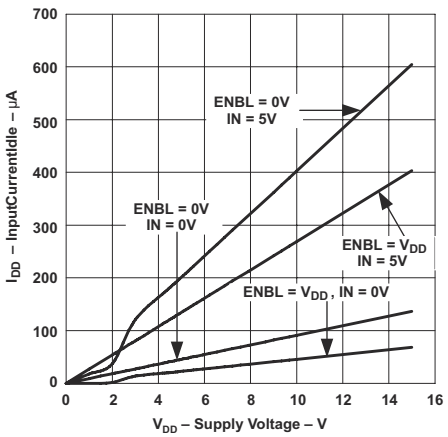


图 7-4. Input Current Idle vs Supply Voltage (UCCx7322)

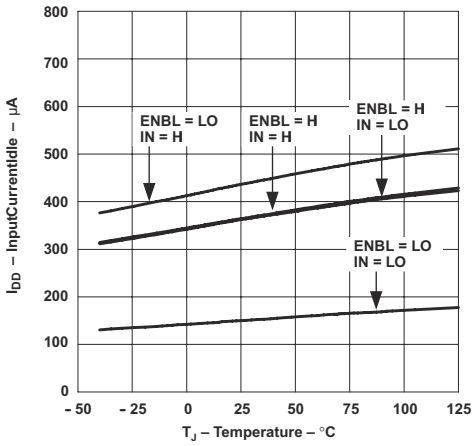


图 7-5. Input Current Idle vs Temperature (UCCx7321)

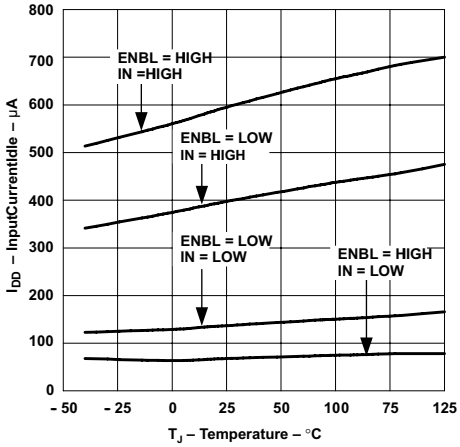


图 7-6. Input Current Idle vs Temperature (UCCx7322)

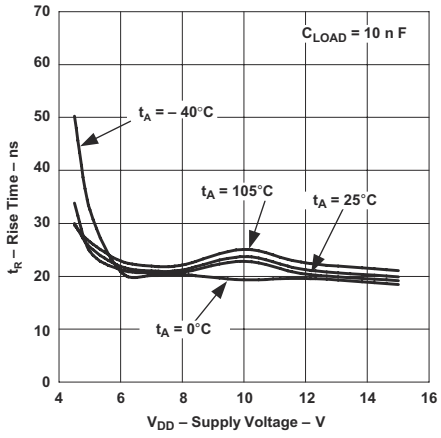


图 7-7. Rise Time vs Supply Voltage

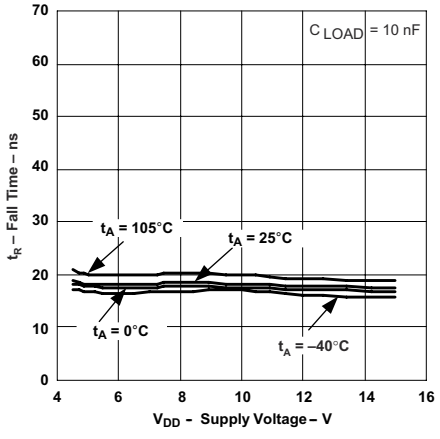


图 7-8. Fall Time vs Supply Voltage

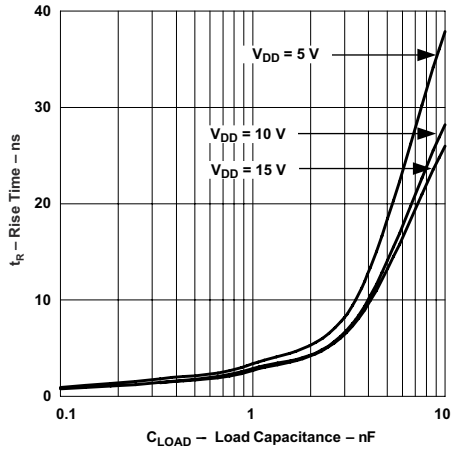


图 7-9. Rise Time vs Load Capacitance

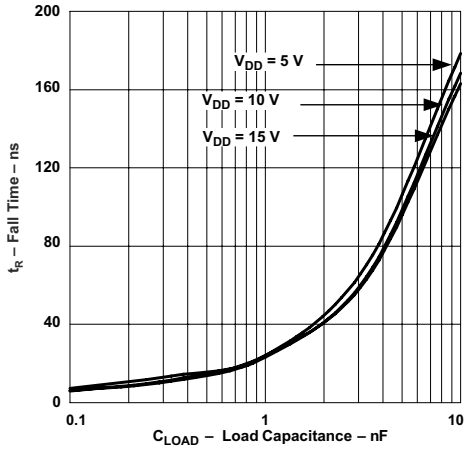


图 7-10. Fall Time vs Output Capacitance

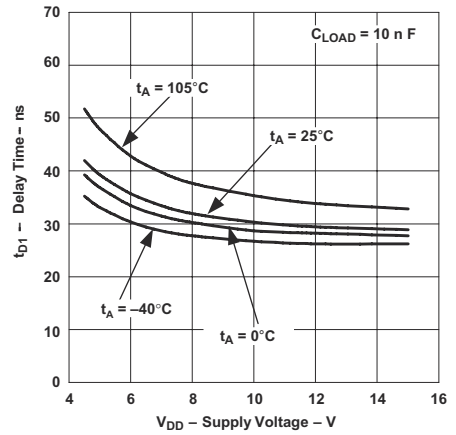


图 7-11. t_{D1} Delay Time vs Supply Voltage

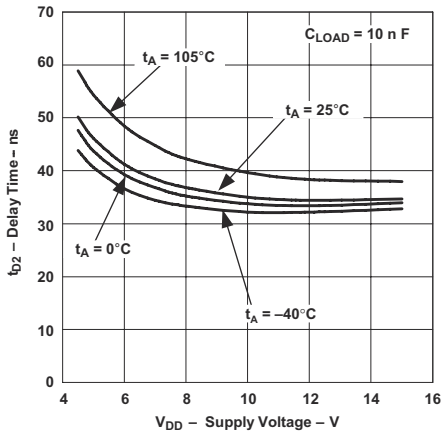


图 7-12. t_{D2} Delay Time vs Supply Voltage

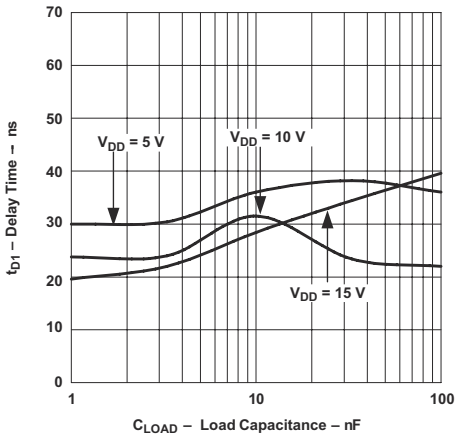


图 7-13. t_{D1} Delay Time vs Load Capacitance

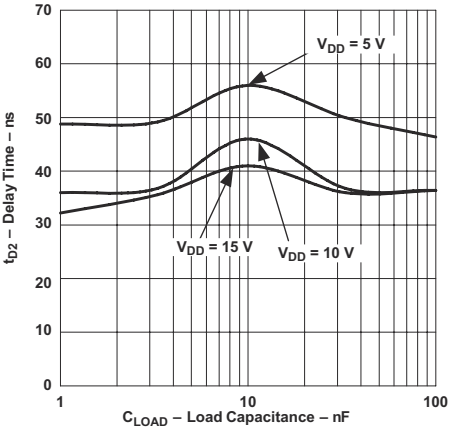


图 7-14. t_{D2} Delay Time vs Load Capacitance

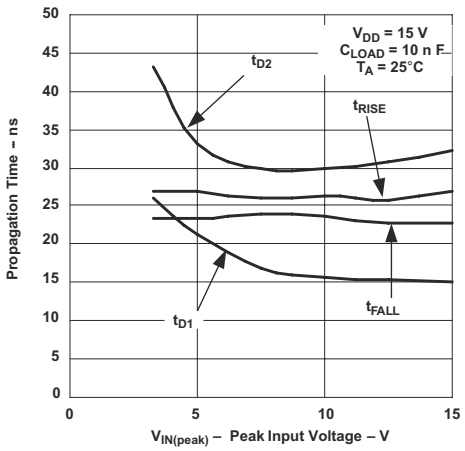


图 7-15. Propagation Times vs Peak Input Voltage

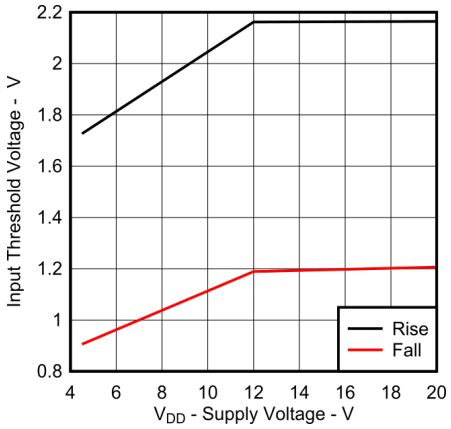


图 7-16. Input Threshold vs Supply Voltage

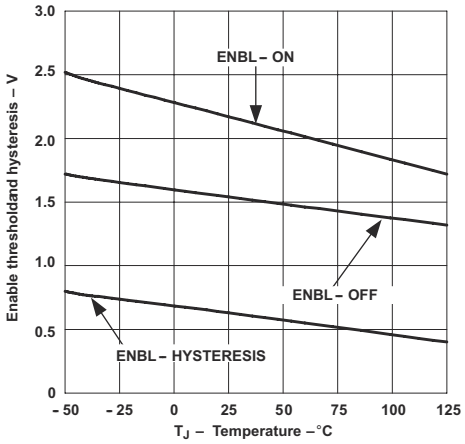


图 7-17. Enable Threshold and Hysteresis vs Temperature

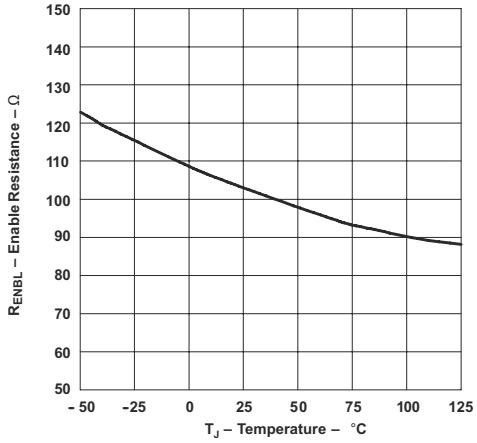


图 7-18. Enable Resistance vs Temperature

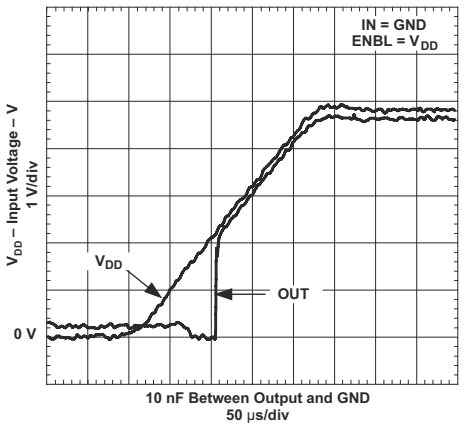


图 7-19. Output Behavior vs V_{DD} (UCC37321)

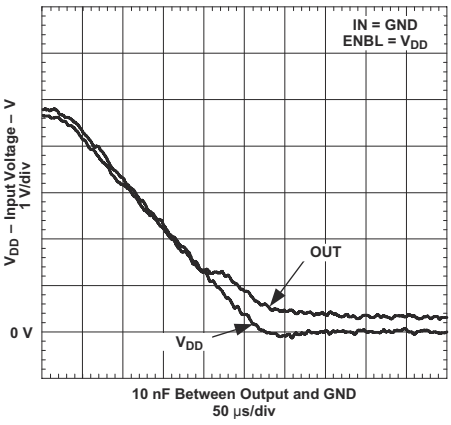


图 7-20. Output Behavior vs V_{DD} (UCC37321)

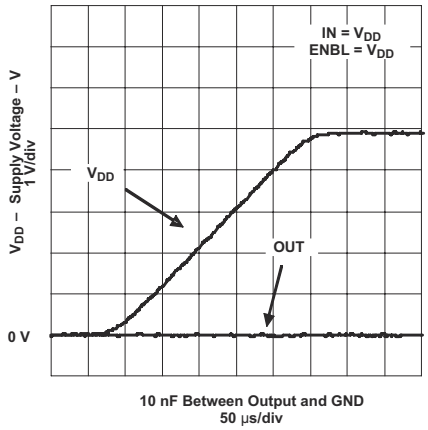


图 7-21. Output Behavior vs VDD (Inverting)

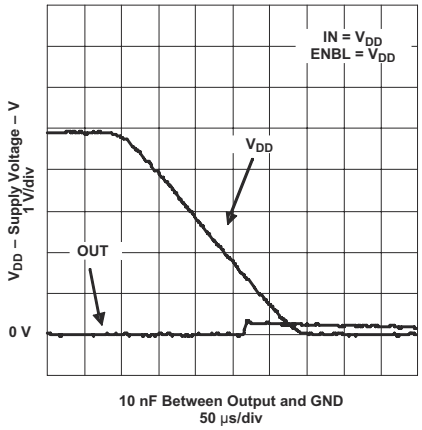


图 7-22. Output Behavior vs VDD (Inverting)

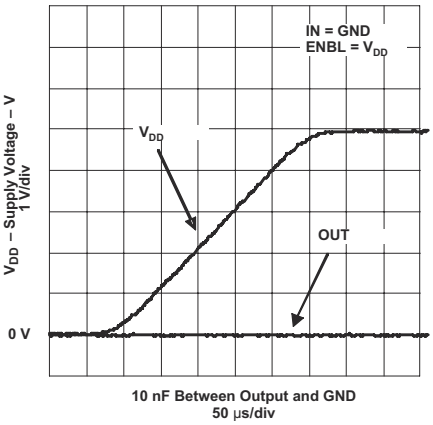


图 7-23. Output Behavior vs VDD (Noninverting)

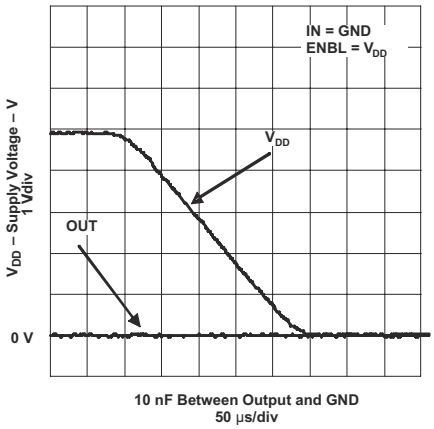


图 7-24. Output Behavior vs VDD (Noninverting)

8 Detailed Description

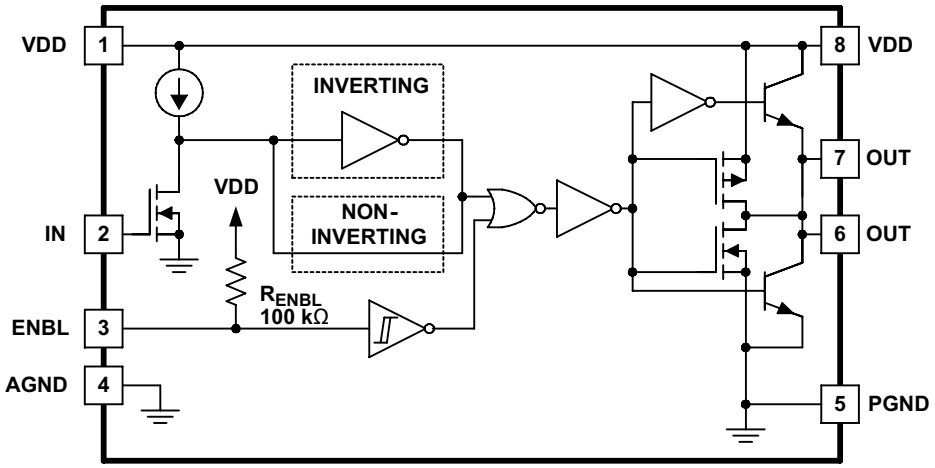
8.1 Overview

The UCC37321 and UCC37322 drivers serve as an interface between low-power controllers and power MOSFETs. They can also be used as an interface between DSPs and power MOSFETs. High-frequency power supplies often require high-speed, high-current drivers such as the UCC3732x family. A leading application is the need to provide a high power buffer stage between the PWM output of the control device and the gates of the primary power MOSFET or IGBT switching devices. In other cases, the device drives the power device gates through a drive transformer. Synchronous rectification supplies must simultaneously drive multiple devices which can present an extremely large load to the control circuitry.

The inverting driver (UCC37321) is useful for generating inverted gate drive signals from controllers that have only outputs of the opposite polarity. For example, this driver can provide a gate signal for ground referenced, N-channel synchronous rectifier MOSFETs in buck derived converters. This driver can also be used for generating a gate drive signal for a P-channel MOSFET from a controller that is designed for N-channel applications.

MOSFET gate drivers are generally used when it is not feasible to have the primary PWM regulator device directly drive the switching devices for one or more reasons. The PWM device may not have the brute drive capability required for the intended switching MOSFET, limiting the switching performance in the application. In other cases there may be a desire to minimize the effect of high-frequency switching noise by placing the high current driver physically close to the load. Also, newer devices that target the highest operating frequencies may not incorporate onboard gate drivers at all. Their PWM outputs are only intended to drive the high impedance input to a driver such as the UCC3732x. Finally, the control device may be under thermal stress due to power dissipation, and an external driver can help by moving the heat from the controller to an external package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Stage

The IN threshold has a 3.3-V logic sensitivity over the full range of VDD voltages; yet, it is equally compatible with 0 V to VDD signals. The inputs of UCC3732x family of drivers are designed to withstand 500-mA reverse current without either damage to the device or logic upset. In addition, the input threshold turnoff of the UCC3732x has been slightly raised for improved noise immunity. The input stage of each driver must be driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (< 200 ns). The IN input of the driver functions as a digital gate, and it is not intended for applications where a slow changing input voltage is used to generate a switching output when the logic threshold of the input section is reached. While this may not be harmful to the driver, the output of the driver may switch repeatedly at a high frequency.

Users should not attempt to shape the input signals to the driver in an attempt to slow down (or delay) the signal at the output. If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the device package, as discussed in 节 11.3.

8.3.2 Output Stage

The TrueDrive output stage is capable of supplying ±9-A peak current pulses; it swings to both VDD and GND and can encourage even the most stubborn MOSFETs to switch. The pullup and pulldown circuits of the driver are constructed of bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(ON)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the internal MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

This unique BiPolar and MOSFET hybrid output architecture (TrueDrive) allows efficient current sourcing at low supply voltages. The UCC3732x family delivers 9 A of gate drive where it is most needed during the MOSFET switching transition – at the Miller plateau region – providing improved efficiency gains.

8.3.3 Source and Sink Capabilities during Miller Plateau

Large power MOSFETs present a significant load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCC3732x drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging or discharging of the drain-gate capacitance with current supplied or removed by the driver device.

Two circuits are used to test the current capabilities of the UCC3732x driver (see Reference 1) . In each case external circuitry is added to clamp the output near 5 V while the device is sinking or sourcing current. An input pulse of 250 ns is applied at a frequency of 1 kHz in the proper polarity for the respective test. In each test there is a transient period where the current peaked up and then settled down to a steady-state value. The noted current measurements are made at a time of 200 ns after the input pulse is applied, after the initial transient.

The circuit in 图 8-1 is used to verify the current sink capability when the output of the driver is clamped around 5 V, a typical value of gate-source voltage during the Miller plateau region. The UCC37321 is found to sink 9 A at V_{DD} = 15 V.

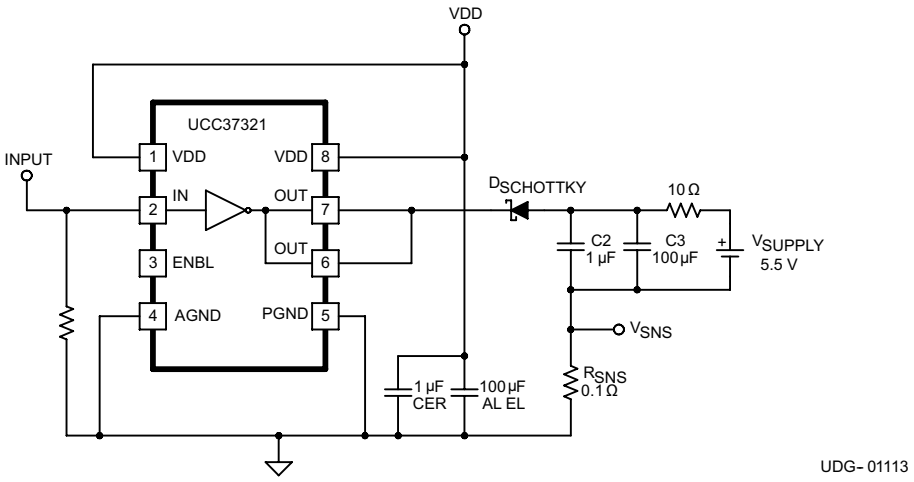


图 8-1. Sink Current Test Circuit

The circuit in 图 8-2 is used to test the current source capability with the output clamped to around 5 V with a string of Zener diodes. The UCC37321 is found to source 9 A at V_{DD} = 15 V.

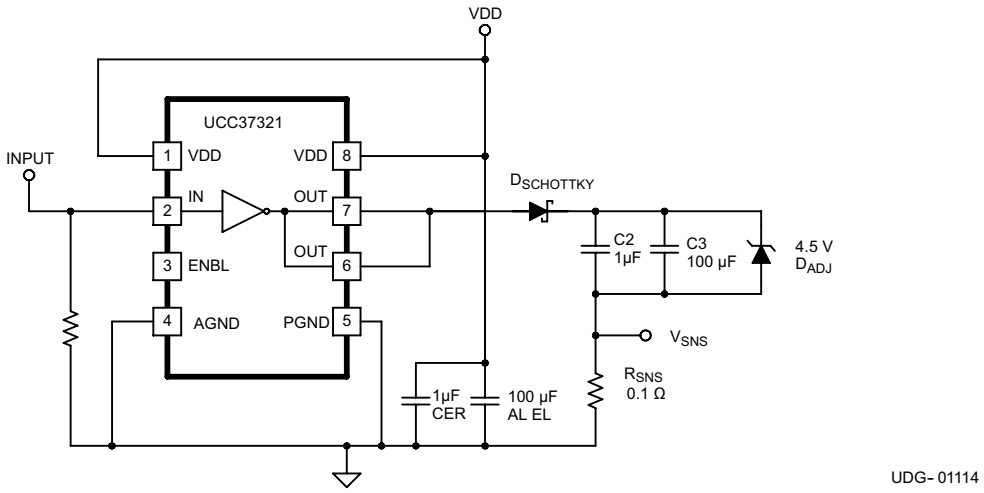


图 8-2. Source Current Test Circuit

Note that the current sink capability is slightly stronger than the current source capability at lower VDD. This is due to the differences in the structure of the bipolar-MOSFET power output section, where the current source is a P-channel MOSFET and the current sink has an N-channel MOSFET.

In most it is advantageous that the turnoff capability of a driver is stronger than the turnon capability. This helps to ensure that the MOSFET is held OFF during common power supply transients which may turn the device back ON.

8.3.4 Enable

The UCC37321/2 provides an enable input for improved control of the driver operation. This input also incorporates logic compatible thresholds with hysteresis. It is internally pulled up to VDD with 100-kΩ resistor for active high operation. When ENBL is high, the device is enabled and when ENBL is low, the device is disabled. The default state of the ENBL pin is to enable the device and therefore it can be left open for standard operation. The output state when the device is disabled is low regardless of the input state. See 表 8-1 for the operation using enable logic.

ENBL input is compatible with both logic signals and slow changing analog signals. It can be directly driven or a power-up delay can be programmed with a capacitor between ENBL and AGND.

8.4 Device Functional Modes

表 8-1 lists the logic of this device.

表 8-1. Device Logic Table

	ENBL	IN	OUT
INVERTING UCC37321	0	0	0
	0	1	0
	1	0	1
	1	1	0
NON-- INVERTING UCC37322	0	0	0
	0	1	0
	1	0	0
	1	1	1

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. To enable fast switching of power devices and reduce associated power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation may be encountered because the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or P- N- channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this because they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting and buffer drive functions. Gate drivers may also minimize the effect of switching noise by locating the high-current driver physically close to the power switch, drive gate-driver transformers and control floating power device gates, reducing power dissipation and thermal stress in controllers by absorbing gate-charge power losses.

In summary gate drivers are extremely important components in switching power combining benefits of high-performance, low-cost, low component count, board-space reduction, and simplified system design.

9.2 Typical Application

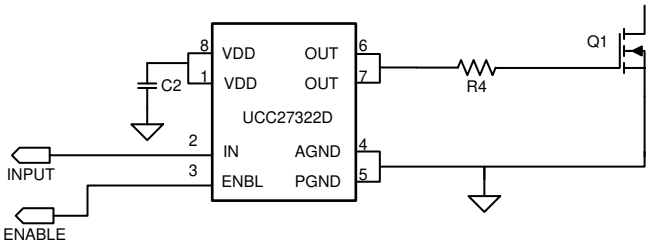


图 9-1. Typical Application Diagram of UCC27322 and UCC37322

9.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. The following design parameters should be used when selecting the proper gate driver device for an end application: input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, availability of independent enable and disable functions, propagation delay, power dissipation, and package type. See the example design parameters and requirements in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-output configuration	Noninverting
Input threshold type	CMOS
Bias supply voltage levels	12 V
dVDS/dt(1)	20 V/ns
Enable function	Yes
Propagation delay	< 50 ns
Power dissipation	< 0.45 W
Package type	SOIC (8)

(1) dVDS/dt is a typical requirement for a given design. This value can be used to find the peak source/sink currents needed as shown in 节 9.2.2.4.

9.2.2 Detailed Design Procedure

9.2.2.1 Input-to-Output Configuration

The design should specify which type of input-to-out configuration should be used. If turning on the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the noninverting configuration must be selected. If turning off the power MOSFET or IGBT when the input signal is in high state is preferred, then a device capable of the inverting configuration must be chosen. Based on this noninverting requirement of this application, the proper device out of the UCC27322 or UCC37322 should be selected.

9.2.2.2 Input Threshold Type

The type of input voltage threshold determines the type of controller that can be used with the gate driver device. The UCC2732x and UCC3732x devices feature a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See 节 7.5 for the actual input threshold voltage levels and hysteresis specifications for the UCC2732x and UCC3732x devices.

9.2.2.3 VDD Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pins of the device must never exceed the values listed in 节 7.3. However, different power switches require different voltage levels to be applied at the gate. With a wide operating range from 4.5 V to 15 V, the UCC2732x and UCC3732x can be used to drive a variety of power switches, such as Si MOSFETs (for example, Vgs = 4.5 V, 10 V, 12 V), IGBTs (V_{GE}=15 V), and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

9.2.2.4 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff must be as fast as possible to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dvDS/dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned on with a Dvds/dt of 20 V/ns or higher under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power loss is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to $V_{DS(on)}$ in ON state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (Q_{gd} parameter in SPP20N60C3 power MOSFET data sheet is 33 nC typically) is supplied by the peak current of gate driver.

According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, $V_{GS(th)}$).

To achieve the targeted Dvds/dt, the gate driver must be capable of providing the Q_{gd} charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC) / 20 ns) or higher must be provided by the gate driver. The UCC2732x and UCC3732x devices can provide 9-A peak sourcing/sinking current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. This 9-A peak sourcing/sinking current provides an extra margin against part-to-part variations in the Q_{gd} parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace in the gate driver circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effort of this trace inductance is to limit the di/dt of the output current pulse of the gate driver. To illustrate this effect, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (0.5 × IPEAK × time) would equal the total gate charge of the power MOSFET (Q_g parameter in SPP20N60C3 power MOSFET data sheet= 87 nC typically). If the parasitic trace inductance limits the di/dt then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the Q_g required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the IPEAK value of the current pulse would be much less than the true peak current capability of the device, while the required Q_g is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver can achieve the targeted witching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

9.2.2.5 Enable and Disable Function

Certain applications demand independent control of the output state of the driver without involving the input signal. A pin which offers enable and disable functions achieves the requirements. For these applications, the UCC2732x and UCC3732x are suitable as they feature an input pin and an Enable pin.

9.2.2.6 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC2732x and UCC3732x devices feature 25-ns turnon propagation delay and 35-ns turnoff propagation delay (typical), which ensure very little distortion and allow operation at higher frequencies. See 节 7.5 for the propagation and 节 7.6 of the UCC2732x and UCC3732x devices.

9.2.2.7 Power Dissipation

The UCC3732x family of drivers are capable of delivering 9-A of current to a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn an N-channel device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. An N-channel MOSFET is used in this discussion because it is the most common type of switching device used in high-frequency power conversion equipment.

References 1 and 2 contain detailed discussions of the drive current required to drive a power MOSFET and other capacitive-input switching devices. Much information is provided in tabular form to give a range of the current required for various devices at various frequencies. The information pertinent to calculating gate drive current requirements will be summarized here; the original document is available from the TI website.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by 方程式 1.

$$E = \frac{1}{2}CV^2 \tag{1}$$

where

- C is the load capacitor
- V is the bias voltage feeding the driver

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by 方程式 2.

$$P = 2 \times \frac{1}{2} CV^2 f \tag{2}$$

where

- f is the switching frequency

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An example using the conditions of the previous gate-drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as shown in 方程式 4.

$$P = 10\ nF \times (12)^2 \times (300\ kHz) = 0.432\ W \tag{3}$$

With a 12-V supply, this would equate, as shown in 方程式 4, to a current of:

$$I = \frac{P}{V} = \frac{0.432\ W}{12\ V} = 0.036A \tag{4}$$

The switching load presented by a power MOSFETcan be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence Qg = CeffV to provide 方程式 5 for power.

$$P = C \times V^2 \times f = Qg \times V \times f \tag{5}$$

方程式 5 allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

9.2.3 Application Curves

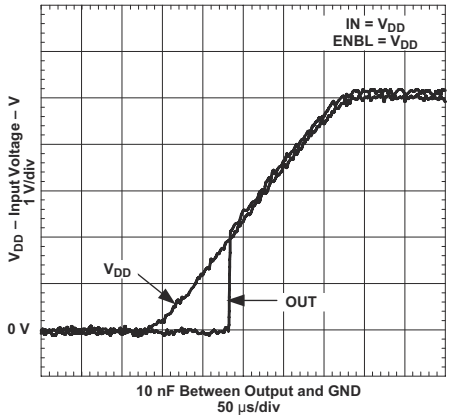


图 9-2. Output Behavior vs VDD (UCC37322)

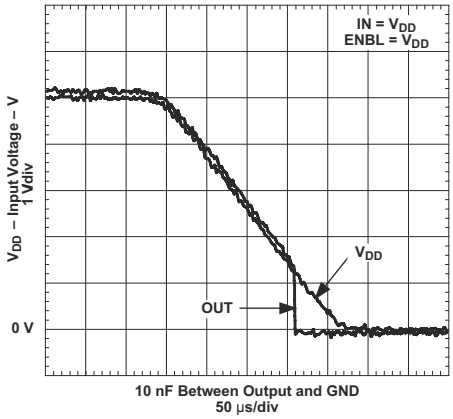


图 9-3. Output Behavior vs VDD (UCC37322)

10 Power Supply Recommendations

Although quiescent VDD current is very low, total supply current is higher, depending on OUTA and OUTB current and the operating frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated using 方程式 6.

$$I_{OUT} = Qg \times f \quad (6)$$

where

- f is frequency

For the best high-speed circuit performance, TI recommends two V_{DD} bypass capacitors to prevent noise problems. TI also highly recommends using surface mount components. A 0.1-µF ceramic capacitor must be placed closest to the VDD to ground connection. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel to help deliver the high current peaks to the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels in the driver application.

11 Layout

11.1 Layout Guidelines

It can be a significant challenge to avoid the overshoot, undershoot, and ringing issues that can arise from circuit layout. The low impedance of these drivers and their high di/dt can induce ringing between parasitic inductances and capacitances in the circuit. Utmost care must be used in the circuit layout.

In general, position the driver physically as close to its load as possible. Place a 1-µF bypass capacitor as close to the output side of the driver as possible, connecting it to pins 1 and 8. Connect a single trace between the two VDD pins (pin 1 and pin 8); connect a single trace between PGND and AGND (pin 5 and pin 4). If a ground plane is used, it may be connected to AGND; do not extend the plane beneath the output side of the package (pins 5 – 8). Connect the load to both OUT pins (pins 7 and 6) with a single trace on the adjacent layer to the component layer; route the return current path for the output on the component side, directly over the output path.

Extreme conditions may require decoupling the input power and ground connections from the output power and ground connections. The UCCx732x has a feature that allows the user to take these extreme measures, if necessary. There is a small amount of internal impedance of about 15 Ω between the AGND and PGND pins; there is also a small amount of impedance (approximately 30 Ω) between the two VDD pins. To take advantage of this feature, connect a 1-µF bypass capacitor between VDD and PGND (pins 5 and 8) and connect a 0.1-µF bypass capacitor between VDD and AGND (pins 1 and 4). Further decoupling can be achieved by connecting between the two VDD pins with a jumper that passes through a 40-MHz ferrite bead and connect bias power only to pin 8. Even more decoupling can be achieved by connecting between AGND and PGND with a pair of anti-parallel diodes (anode connected to cathode and cathode connected to anode).

11.2 Layout Example

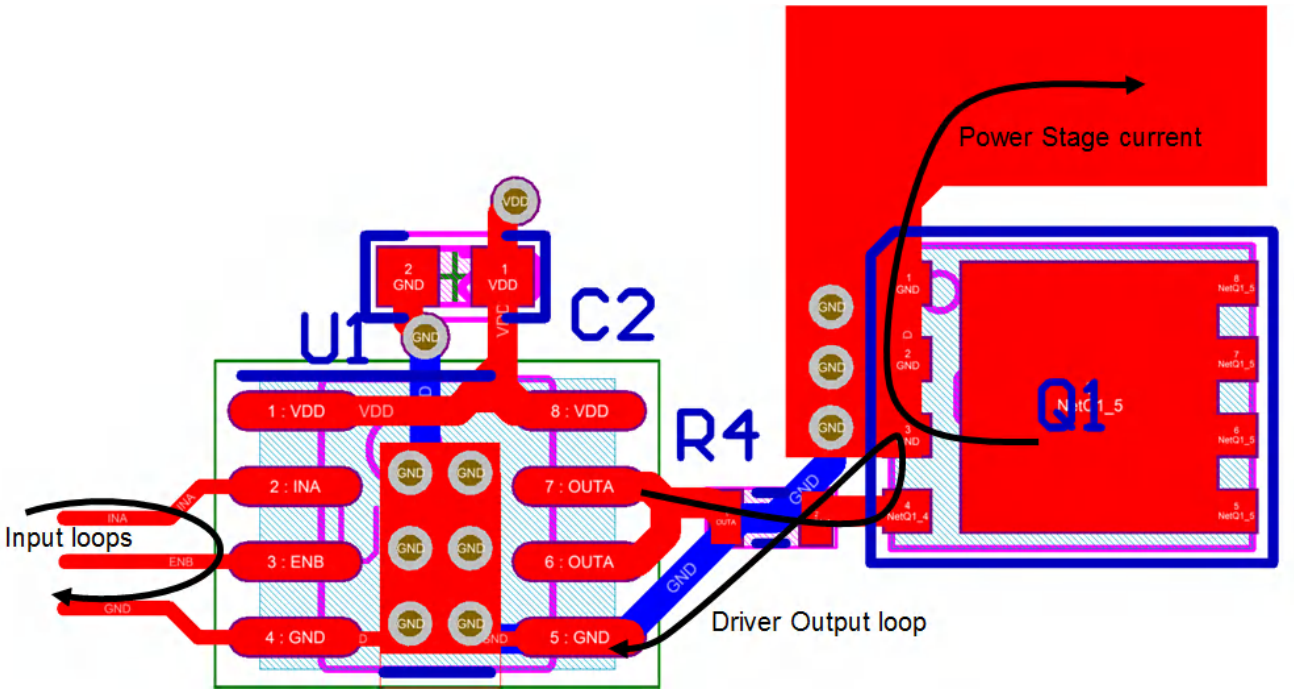


图 11-1. Layout Recommendation

11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. For a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCC3732x family of drivers is available in three different packages to cover a range of application requirements.

As shown in the power dissipation rating table, the 8-pin SOIC (D) and 8-pin PDIP (P) packages each have a power rating of around 0.5 W with T_A = 70°C. This limit is imposed in conjunction with the power derating factor also given in the table. The power dissipation in our earlier example is 0.432 W with a 10-nF load, 12 VDD, switched at 300 kHz. Thus, only one load of this size could be driven using the D or P package. The difficulties with heat removal limit the drive available in the D or P packages.

The 8-pin MSOP PowerPAD (DGN) package significantly relieves this concern by offering an effective means of removing the heat from the semiconductor junction. As illustrated in Reference 3, the PowerPAD packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board directly underneath the device package, reducing the θjc down to 4.7°C/W. Data is presented in Reference 3 to show that the power dissipation can be quadrupled in the PowerPAD configuration when compared to the standard packages. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference 4 .This allows a significant improvement in heatsinking over that available in theDor P packages, and is shown to more than double the power capability of the D and P packages.

The PowerPAD is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

12 Device and Documentation Support

12.1 Device Support

12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

1. SEM-1400, Topic 2, *A Design and Application Guide for High Speed Power MOSFET Gate Drive Circuits*
2. U-137, *Practical Considerations in High PerformanceMOSFET, IGBT andMCTGateDrive Circuits*, by Bill Andreycak (SLUA105)
3. Technical Brief, *PowerPad Thermally Enhanced Package* (SLMA002)
4. Application Brief, *PowerPAD Made Easy* (SLMA004)
5. Data Book, *Power Supply Control Products*, (SLUD003)

12.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

12.5 Trademarks

PowerPAD™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (January 2016) to Revision I (November 2023) **Page**

- 删除了“器件信息”表中的 P 封装....1
- 删除了说明（续）部分中的 P 封装....3
- Deleted P package from Pin Configuration and Functions section....5
- Changed ESD Ratings from ±2500 V and ±1500 V to ±2000 V and ±1000 V....6
- Changed input threshold voltage values, deleted V_{OH} output high level and V_{OL} output low level, changed output resistance high and output resistance low values and deleted Latch-up protection from Electrical Characteristics....7
- Deleted P package data from Power Dissipations Ratings section....8
- Changed 图 7-16 10

Changes from Revision G (May 2013) to Revision H (January 2016) **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分....1

Changes from Revision F (March 2012) to Revision G (May 2013) **Page**

- Updated AGND pin description. 5
- Changed minimum value for input voltage from –5 to –0.3 V in the *Absolute Maximum Ratings* table....6
- Added C_{LOAD} = 10 nF to Fall Time vs Supply Voltage graph....10
- Changed Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Rise Time vs Load Capacitance graph....10
- Changed Changed x-axis values from 1, 10, 100 to 0.1, 1, 10 in Fall Time vs Output Capacitance graph....10

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27321D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 105	27321	
UCC27321DGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	-40 to 105	27321	
UCC27321DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 105	27321	Samples
UCC27321P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27321P	Samples
UCC27321PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27321P	Samples
UCC27322D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 105	27322	
UCC27322DGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	-40 to 105	27322	
UCC27322DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	27322	Samples
UCC27322P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27322P	Samples
UCC27322PE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	UCC27322P	Samples
UCC37321D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	37321	
UCC37321DGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	0 to 70	37321	
UCC37321DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	37321	Samples
UCC37321P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37321P	Samples
UCC37322D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	37322	
UCC37322DGN	OBSOLETE	HVSSOP	DGN	8		TBD	Call TI	Call TI	0 to 70	37322	
UCC37322DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322DGNRG4	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC37322DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-1-260C-UNLIM	0 to 70	37322	Samples
UCC37322P	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UCC37322P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27321, UCC27322 :

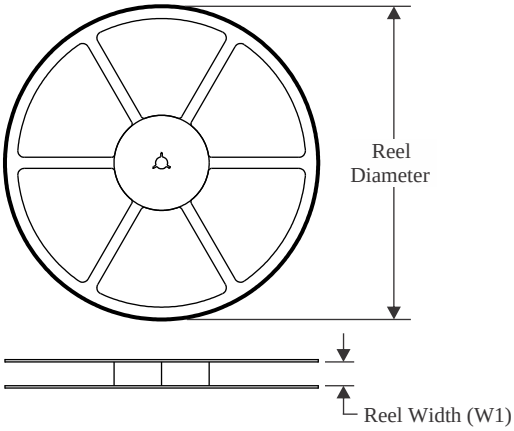
- Automotive : UCC27321-Q1, UCC27322-Q1
- Enhanced Product : UCC27322-EP

NOTE: Qualified Version Definitions:

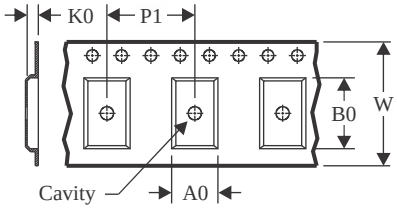
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

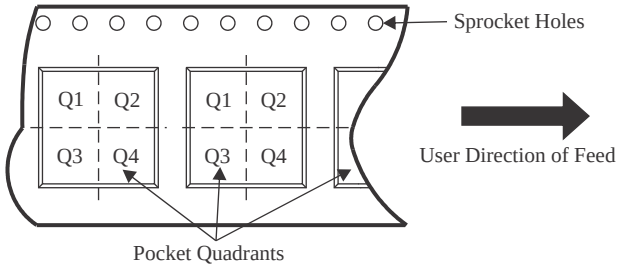


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

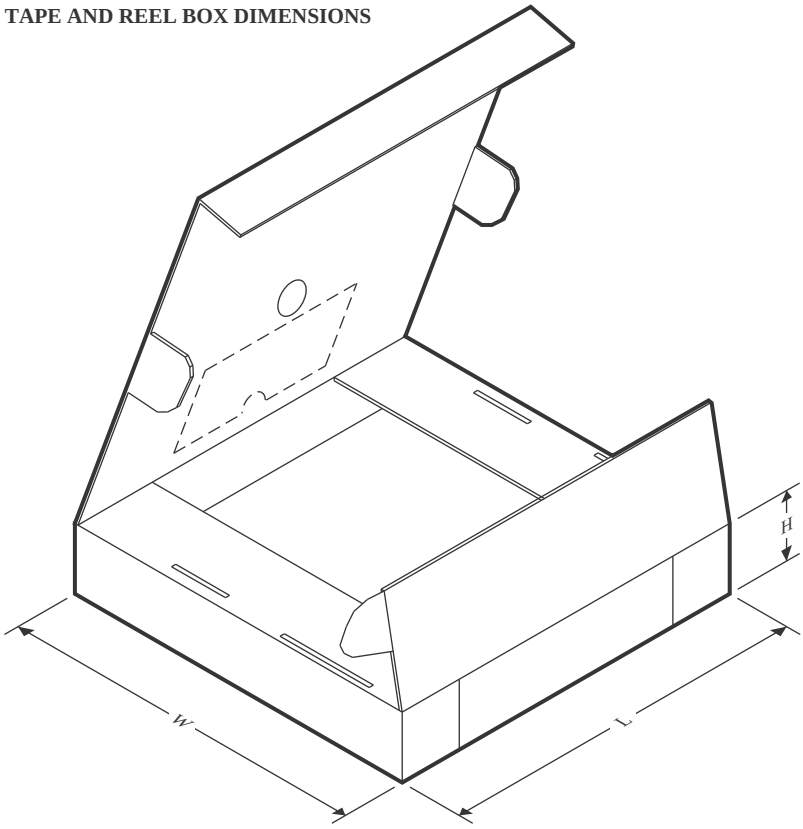
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC27322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37321DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37321DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37322DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37322DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
UCC37322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC37322DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

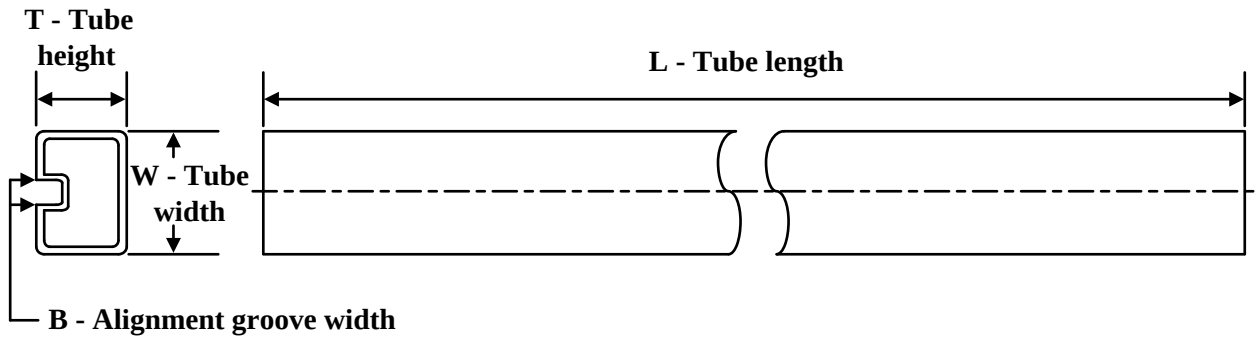
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27321DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC27321DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27321DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC27321DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC27322DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC27322DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC27322DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37321DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37321DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC37321DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37321DR	SOIC	D	8	2500	356.0	356.0	35.0
UCC37322DGNR	HVSSOP	DGN	8	2500	364.0	364.0	27.0
UCC37322DGNR	HVSSOP	DGN	8	2500	353.0	353.0	32.0
UCC37322DR	SOIC	D	8	2500	353.0	353.0	32.0
UCC37322DR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCC27321P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27321PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC27322P	P	PDIP	8	50	506	13.97	11230	4.32
UCC27322PE4	P	PDIP	8	50	506	13.97	11230	4.32
UCC37321P	P	PDIP	8	50	506	13.97	11230	4.32
UCC37322P	P	PDIP	8	50	506	13.97	11230	4.32

GENERIC PACKAGE VIEW

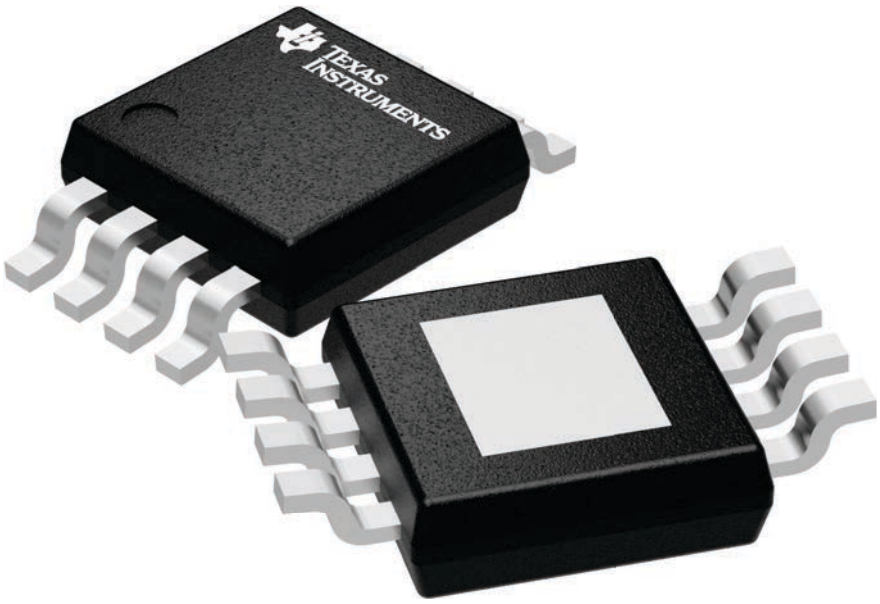
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

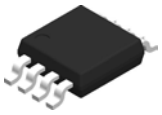
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

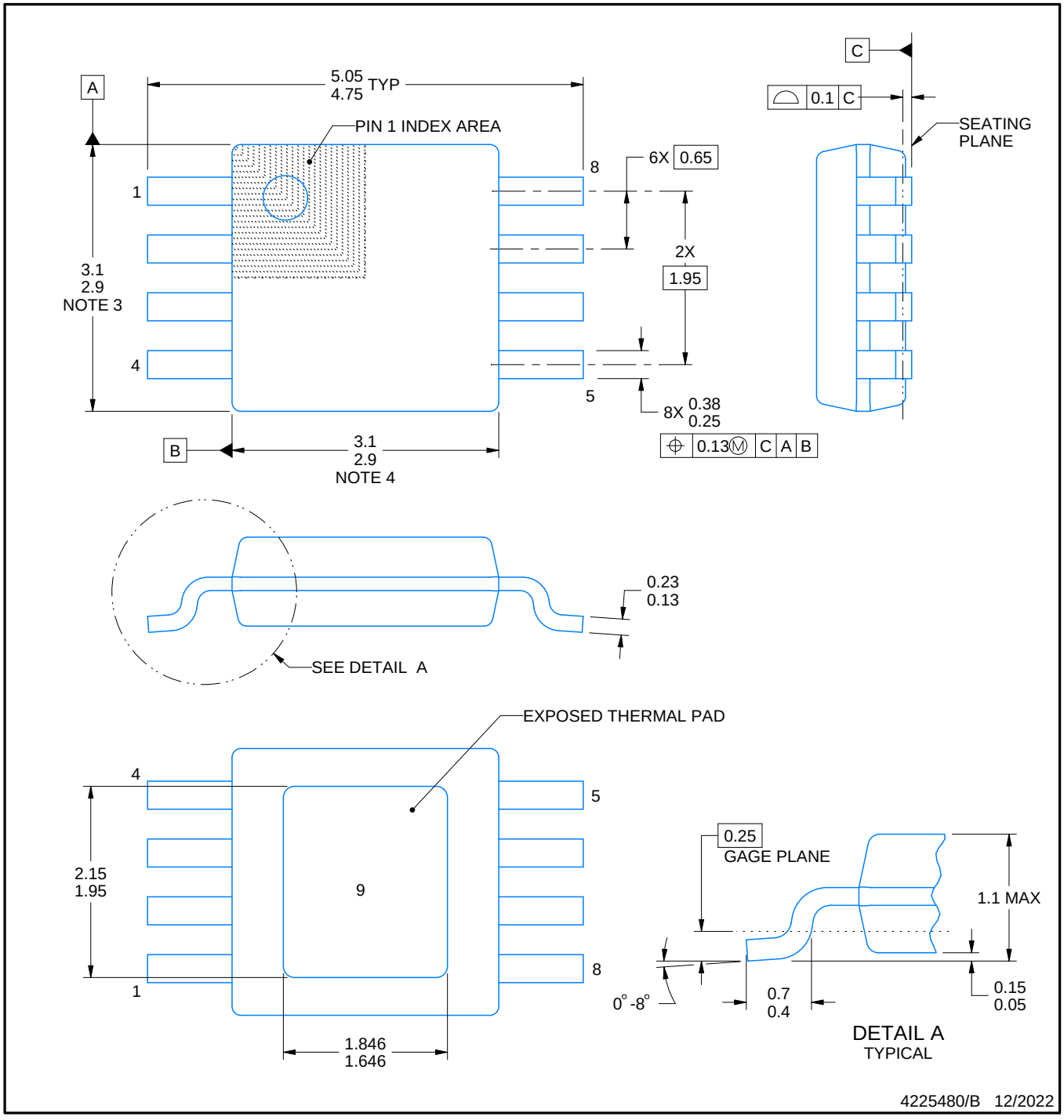
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

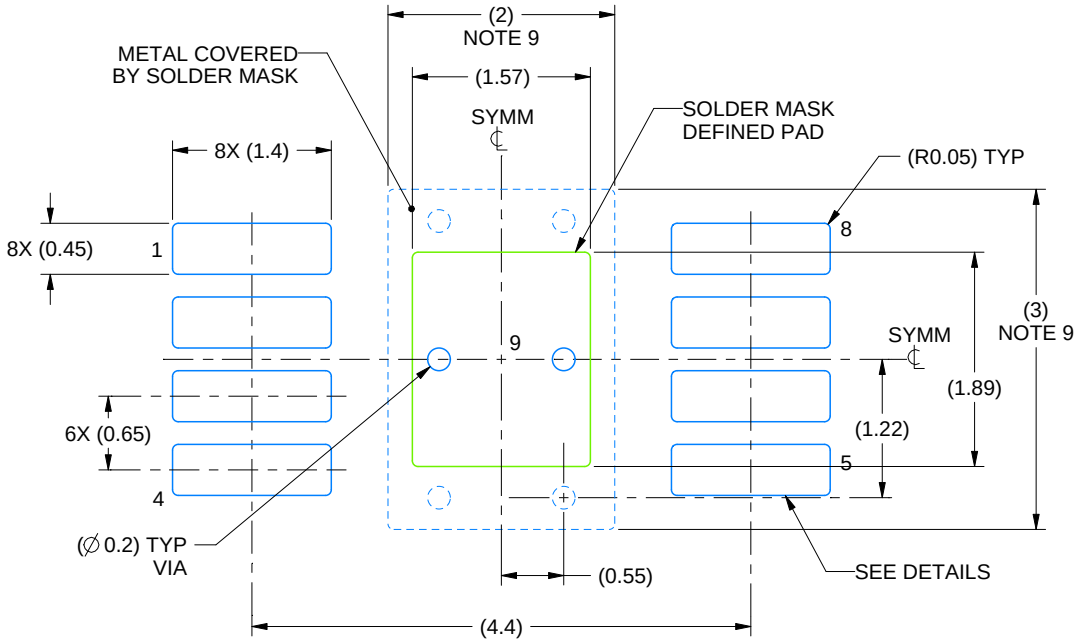
SMALL OUTLINE PACKAGE



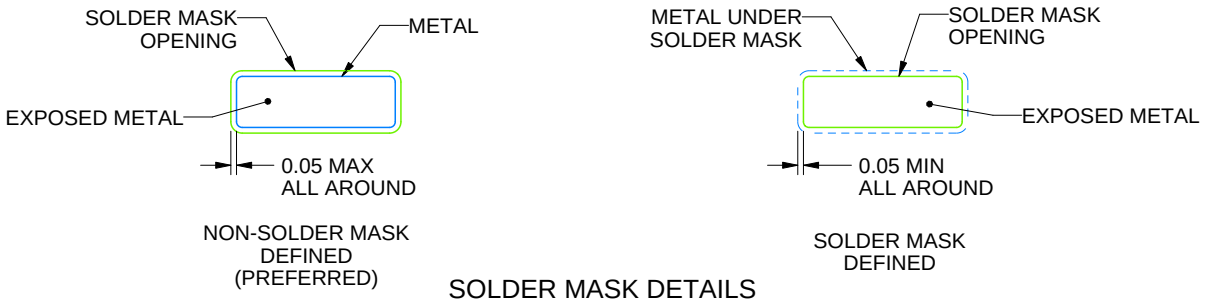
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

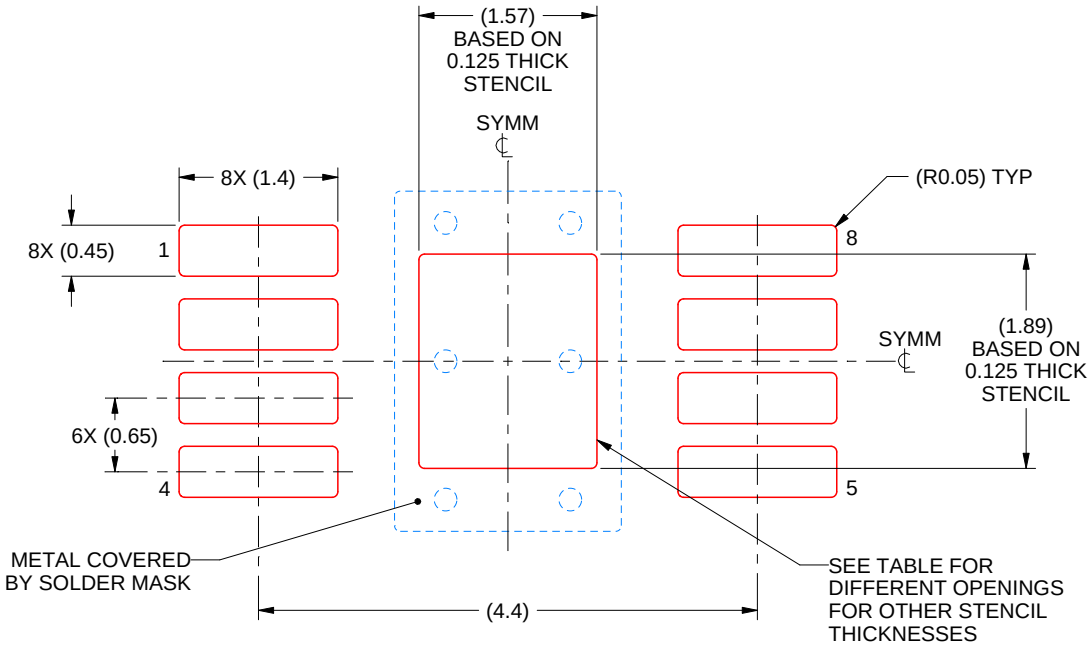


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

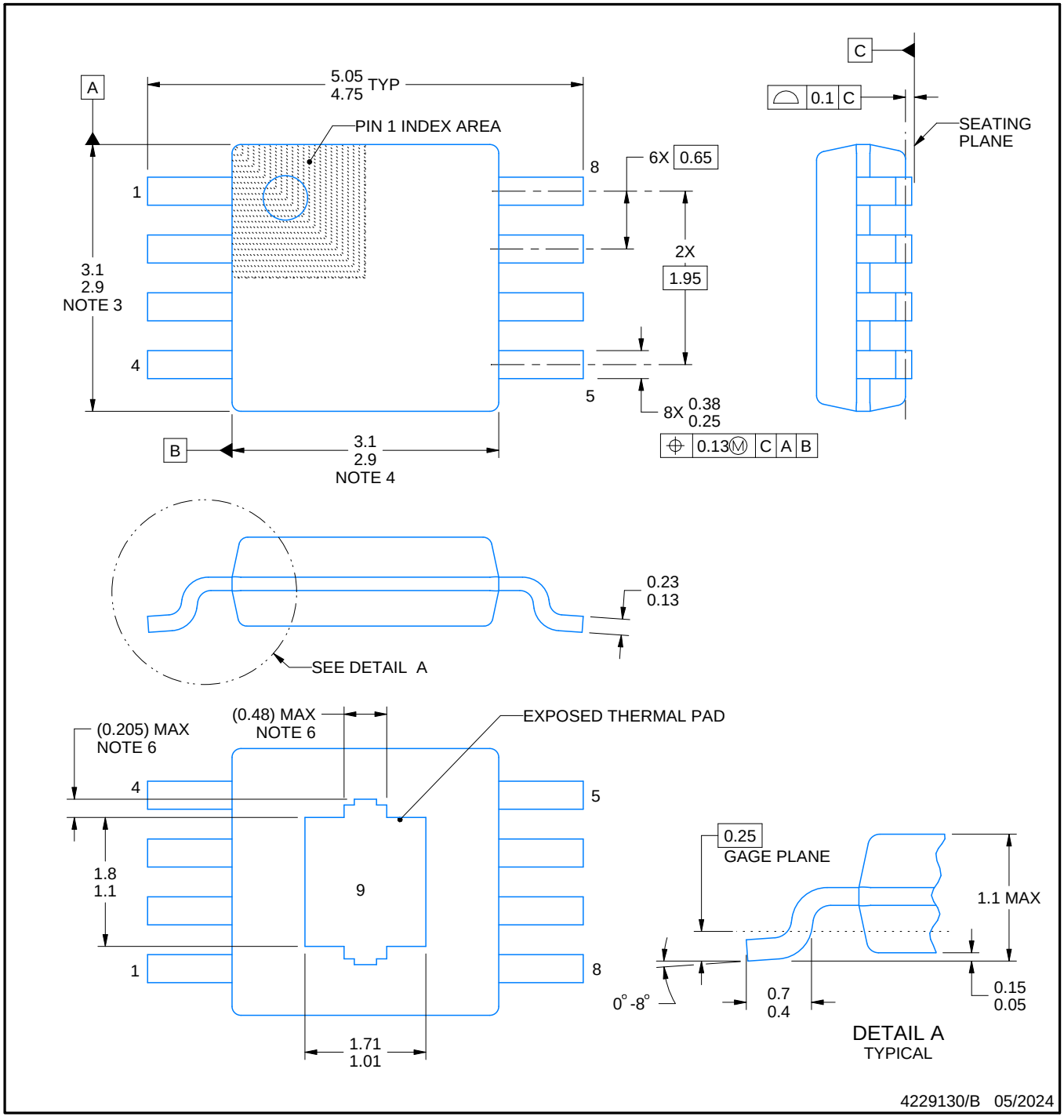
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

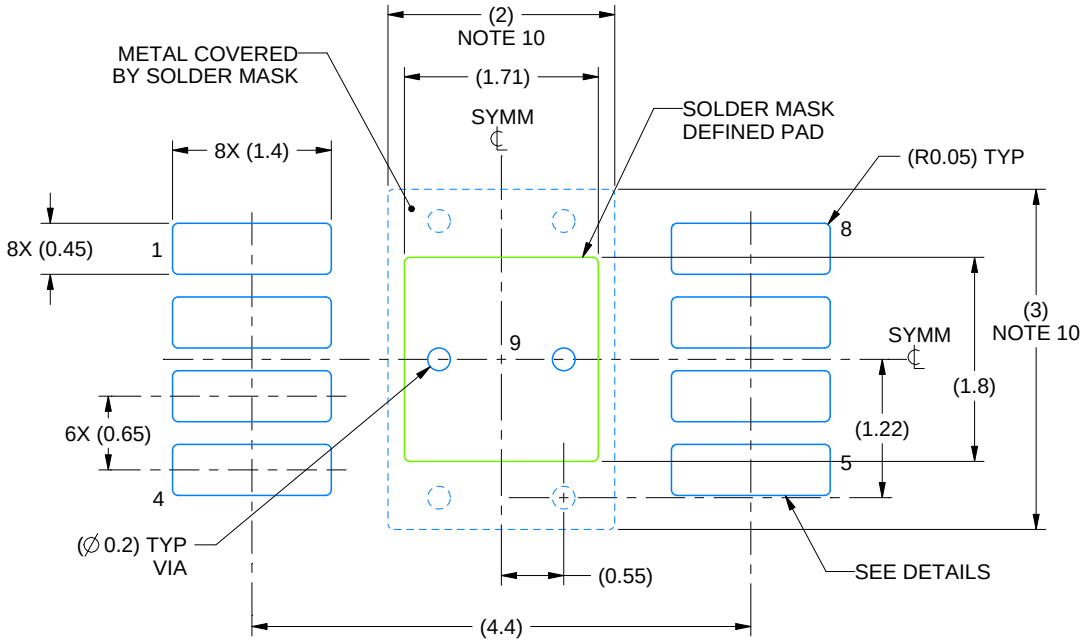
SMALL OUTLINE PACKAGE



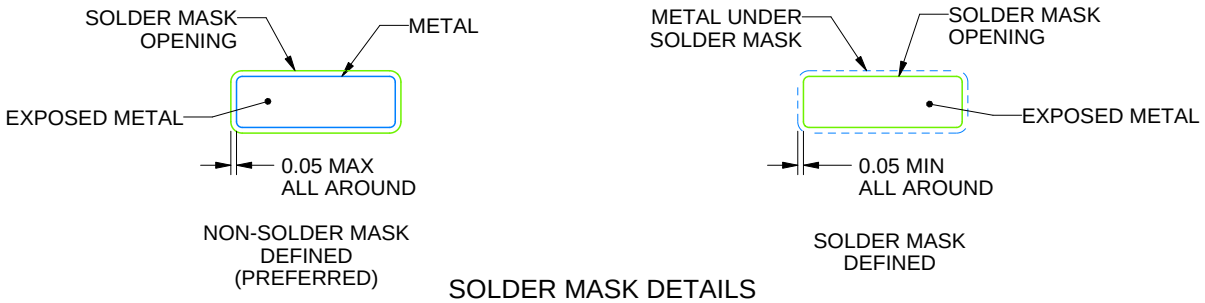
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

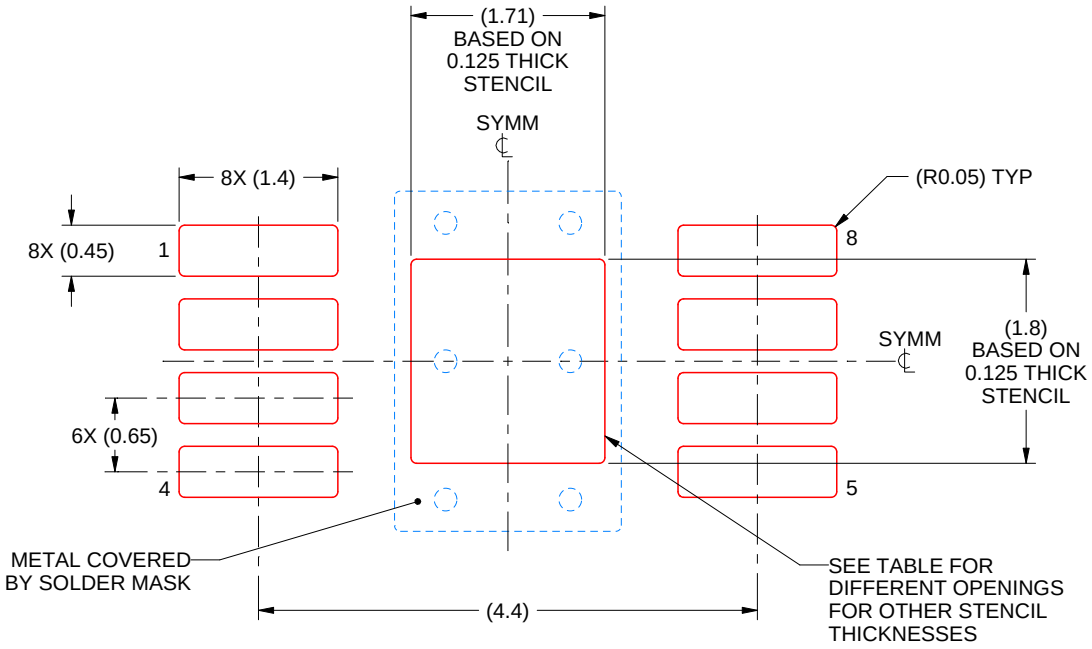


SOLDER MASK DETAILS

4229130/B 05/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



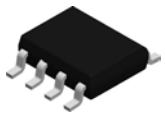
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

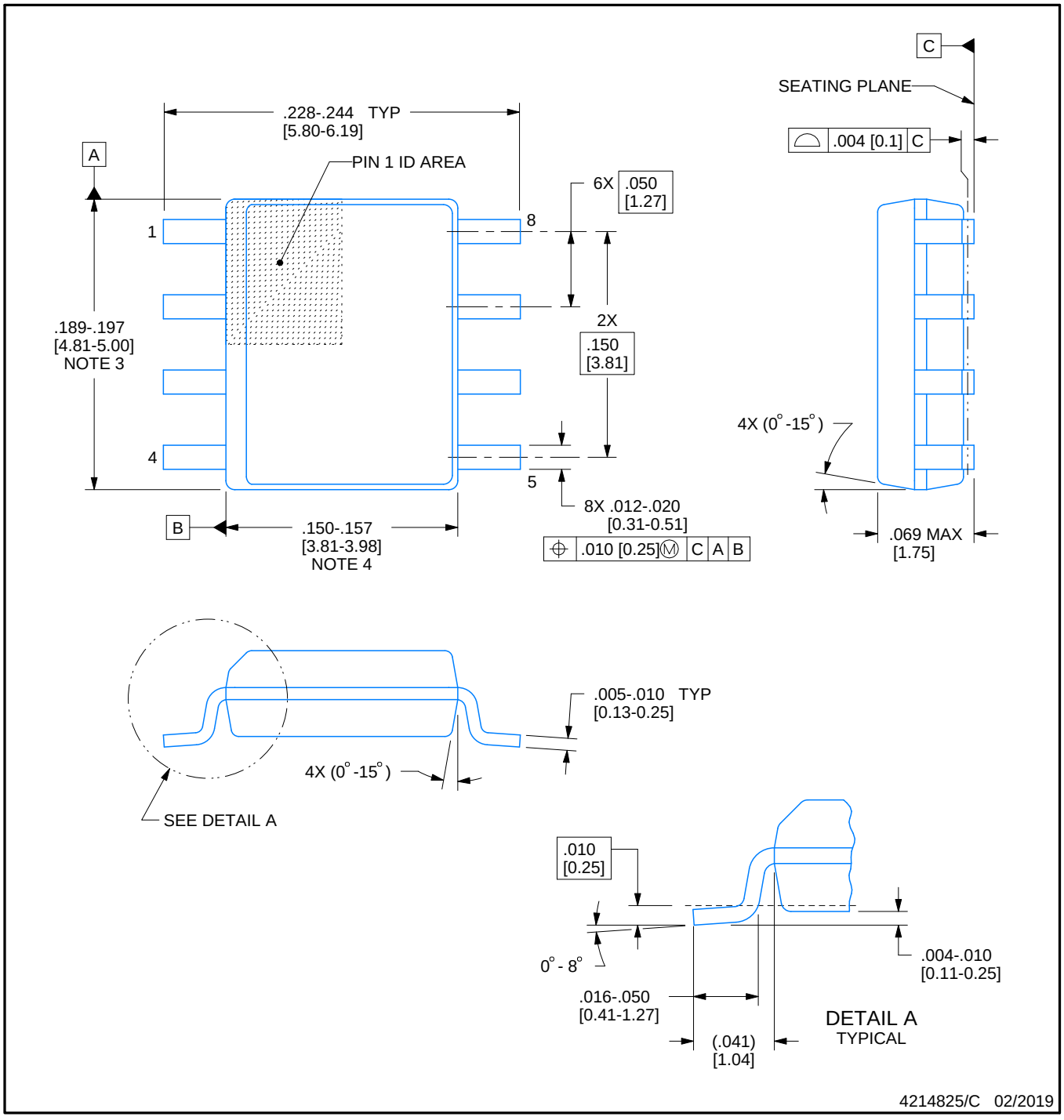


PACKAGE OUTLINE

D0008A

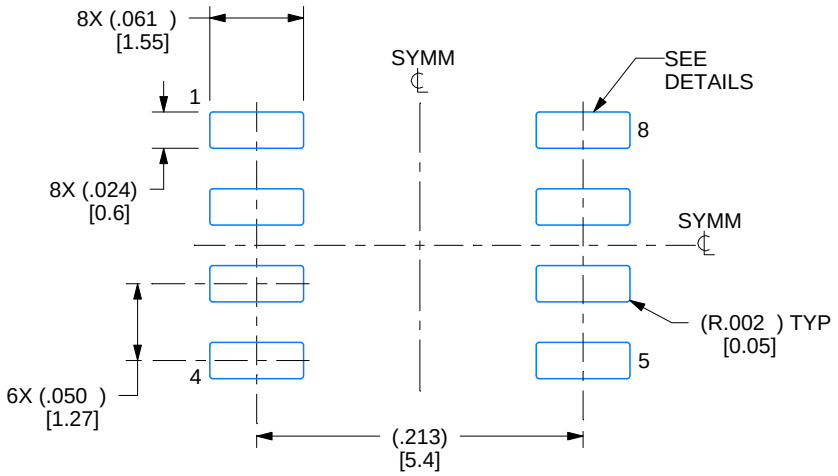
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

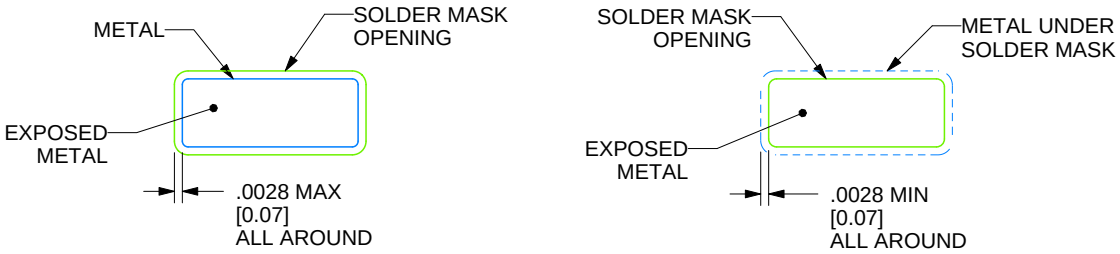


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

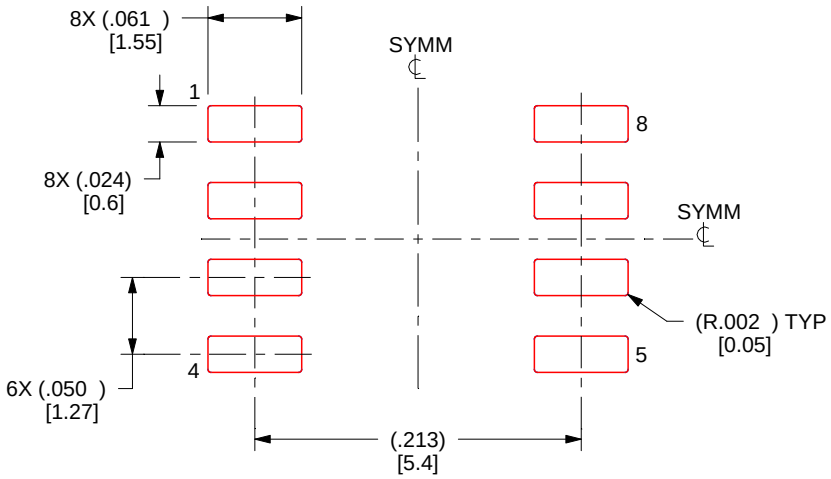
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



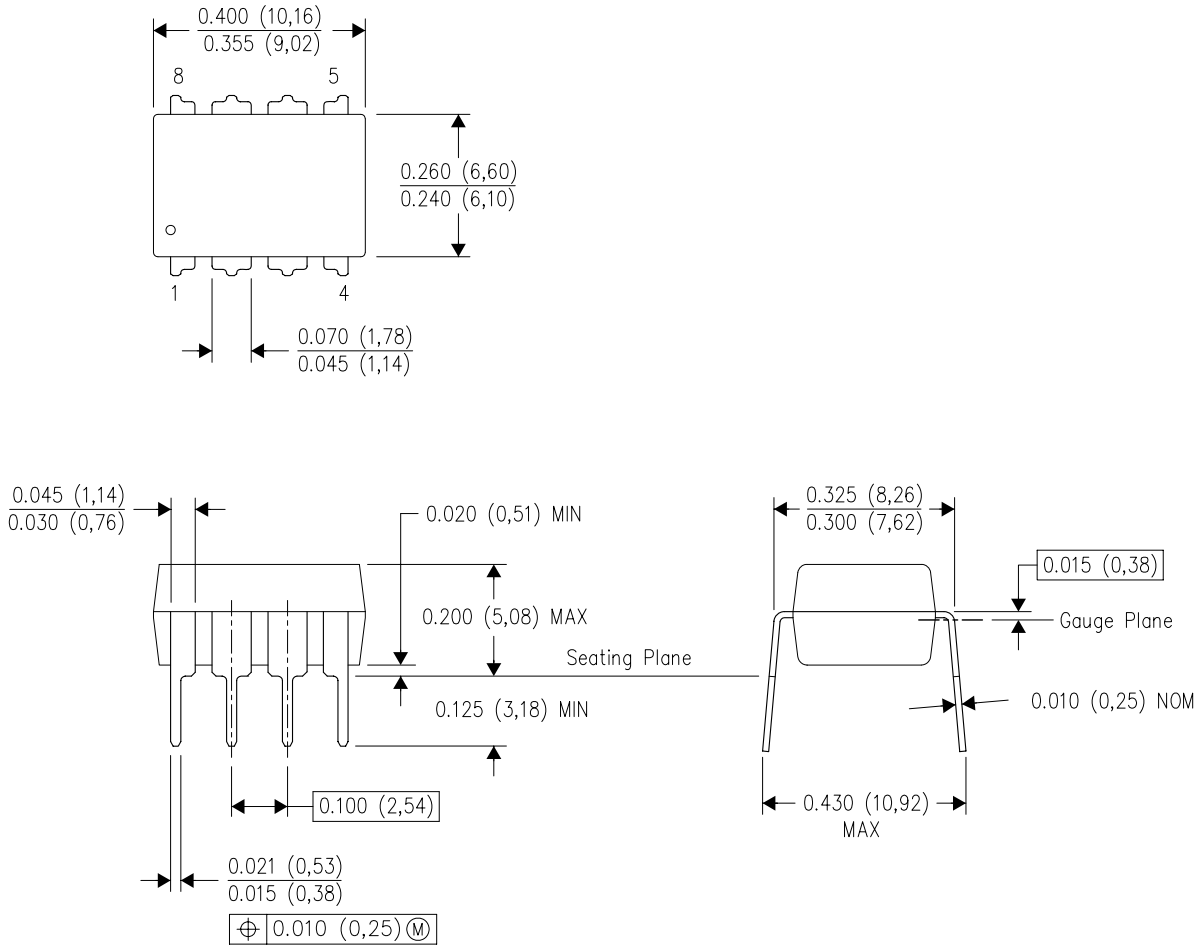
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265