TS5A3166 0.9Ω SPST 模拟开关

1 特性

- 低导通状态电阻 (0.9Ω)
- 控制输入可承受 5.5V 电压
- 低电荷注入
- 低总谐波失真 (THD)
- 1.65V 至 5.5V 单电源运行
- 锁断性能超过 100mA（符合 JESD 78，II 类规范的要求）
- 静电放电 (ESD) 性能测试符合 JESD 22 规范
  - 2000V 人体放电模式（A114-B，II 类）
  - 1000V 充电器件模型 (C101)

2 应用

- 手机
- 掌上电脑 (PDA)
- 便携式仪表
- 音频和视频信号路由
- 低压数据采集系统
- 通信电路
- 调制解调器
- 硬盘
- 计算机外设
- 无线终端和外设
- 麦克风开关 – 笔记本电脑扩展坞

3 说明

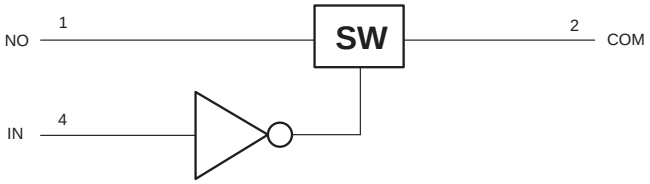
TS5A3166 器件是一款单刀单掷 (SPST) 模拟开关，工作电压范围为 1.65V 至 5.5V。此器件具有较低的导通状态电阻。该器件具有出色的总谐波失真 (THD) 性能和极低的功耗。这些 特性 使得这款器件适合于便携式音频 应用中对于高效率、高电源密度和稳健性的需求。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TS5A3166	SOT-23 (5)	2.90mm × 1.60mm
	SC70 (5)	2.00mm × 1.25mm
	DSBGA (5)	1.388mm × 0.888mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision D (February 2016) to Revision E — **Page**

- Changed the YZP package pin numbers ... 3

Changes from Revision C (May 2015) to Revision D — **Page**

- Added "port" to COM description in *Pin Functions* table ... 3
- Deleted "digitial" from GND description in *Pin Functions* table ... 3

Changes from Revision B (September 2013) to Revision C — **Page**

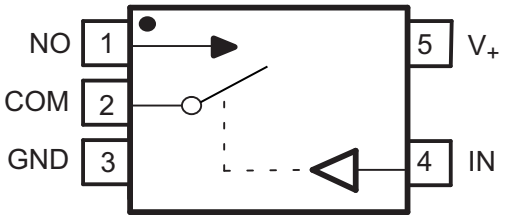
- 已添加*应用*、*器件信息* 表、*引脚功能* 表、*ESD 额定值* 表、*热性能信息* 表、*典型特性*、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 ... 1
- 已删除 *订购信息* 表。 ... 1

Changes from Revision A (October 2012) to Revision B — **Page**

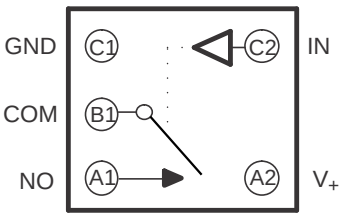
- 删除了特性中的“关断模式隔离 V_+ = 0”*项目符号* ... 1
- 将整个数据表中的引脚名称从 NC 更改成了 NO。 ... 1

5 Pin Configuration and Functions

DBV and DCK Packages
5-Pin SOT-23 and SC-70
Top View



YZP Package
5-Pin DSBGA
Bottom View



Pin Functions

PIN			TYPE	DESCRIPTION
DBC, DCK NO.	YZP NO.	NAME		
1	A1	NO	I/O	Normally opened port
2	B1	COM	I/O	Common port
3	C1	GND	GND	Ground
4	C2	IN	I	Digital control pin to connect COM to NO
5	A2	V_+	Power	Power Supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage(3)(4)(5)		–0.5	V_+ + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	ON-state switch current	V_{NO}, V_{COM} = 0 to V_+	–200	200	mA
	ON-state peak switch current(6)		–400	400	
V_I	Digital input voltage(3)(4)		–0.5	6.5	V
I_{IK}	Digital clamp current	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C
T_j	Junction temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	V_+	V
V_+	Supply voltage	1.65	5.5	V
V_I	Control Input Voltage	0	5.5	V
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TS5A3166			UNIT
		DBV (SOT)	DCK (SC-70)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206	252	132	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics for 5-V Supply

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	4.5 V		0.8	1.1	Ω
				Full				1.2	
r_{on}	ON-state resistance	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	4.5 V		0.7	0.9	Ω
				Full				1	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	4.5 V		0.15		Ω
		V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,		25°C			0.09	0.15	
				Full				0.15	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, see 图 14	25°C	5.5 V	–20	4	20	nA
				Full		–100		100	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		25°C	0 V	–5	0.4	5	μA
				Full		–15		15	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, see 图 14	25°C	5.5 V	–20	4	20	nA
				Full		–100		100	
$I_{COM(PWROFF)}$		V_{COM} = 5.5 V to 0, V_{NO} = 0 to 5.5 V,		25°C	0 V	–5	0.4	5	μA
				Full		–15		15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 5-V Supply (continued)

V_+ = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, see 图 15	25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, see 图 15	25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
V_{IH}	Input logic high			Full		2.4		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	5 V	2.5	4.5	7	ns
				Full	4.5 V to 5.5 V	1.5		7.5	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	5 V	6	9	11.5	ns
				Full	4.5 V to 5.5 V	4		12.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0 ,	C_L = 1 nF, see 图 20	25°C	5 V		1		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See 图 16	25°C	5 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See 图 16	25°C	5 V		18		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See 图 16	25°C	5 V		35.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See 图 16	25°C	5 V		35.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 图 16	25°C	5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 图 18	25°C	5 V		200		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 图 19	25°C	5 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 图 21	25°C	5 V		0.005%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	μA
				Full				0.5	

6.6 Electrical Characteristics for 3.3-V Supply

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	$0 \le V_{NO} \le V_+$, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	3 V		1	1.4	Ω
				Full				1.5	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_{NO} \le V_+$, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	3 V		0.3		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.09	0.15	
				Full				0.15	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see 图 14	25°C	3.6 V	–2	0.5	2	nA
				Full		–20		20	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see 图 14	25°C	3.6 V	–2	0.5	2	nA
				Full		–20		20	
$I_{COM(PWROFF)}$		V_{COM} = 3.6 V to 0, V_{NO} = 0 to 3.6 V,		25°C	0 V	–1	0.1	1	µA
				Full		–5		5	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see 图 15	25°C	3.6 V	–2	0.2	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see 图 15	25°C	3.6 V	–2	0.2	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
V_{IH}	Input logic high			Full		2		5.5	V
V_{IL}	Input logic low			Full		0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	3.3 V	2	5	10	ns
				Full	3 V to 3.6 V	1.5		11	
t_{OFF}	Turnoff time	$V_{COM} = V_+$, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	3.3 V	6.5	9	12	ns
				Full	3 V to 3.6 V	4		13	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see 图 21	25°C	3.3 V		1		pC
$C_{NO(OFF)}$	NO OFF capacitance	$V_{NO} = V_+$ or GND, Switch OFF,	See 图 16	25°C	3.3 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	$V_{COM} = V_+$ or GND, Switch OFF,	See 图 16	25°C	3.3 V		18		pF
$C_{NO(ON)}$	NO ON capacitance	$V_{NO} = V_+$ or GND, Switch ON,	See 图 16	25°C	3.3 V		36		pF
$C_{COM(ON)}$	COM ON capacitance	$V_{COM} = V_+$ or GND, Switch ON,	See 图 16	25°C	3.3 V		36		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 3.3-V Supply (continued)

V_+ = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
C_I	Digital input capacitance	V_I = V_+ or GND,	See 图 16	25°C	3.3 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 图 18	25°C	3.3 V		200		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 图 19	25°C	3.3 V		–64		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 图 21	25°C	3.3 V		0.01%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	3.6 V		0.01	0.1	μA
				Full				0.25	

6.7 Electrical Characteristics for 2.5-V Supply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range				2.3 V	0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	2.3 V		0.7		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.4	0.6	
				Full				0.6	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see 图 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2	0.05	2	μA
				Full		–15		15	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see 图 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 3.6 V to 0, V_{NO} = 0 to 3.6 V,		25°C	0 V	–2	0.05	2	μA
				Full		–15		15	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see 图 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see 图 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.8		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 2.5-V Supply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	2.5 V	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see 图 21	25°C	2.5 V		4		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See 图 16	25°C	2.5 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See 图 16	25°C	2.5 V		18.5		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See 图 16	25°C	2.5 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See 图 16	25°C	2.5 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 图 16	25°C	2.5 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 图 18	25°C	2.5 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 图 19	25°C	2.5 V		–62		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 图 21	25°C	2.5 V		0.02%		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	μA
				Full				0.25	

6.8 Electrical Characteristics for 1.8-V Supply(1)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
Analog Switch									
V_{COM}, V_{NO}	Analog signal range					0		V_+	V
r_{peak}	Peak ON resistance	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	1.65 V		4.2	25	Ω
				Full				30	
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	1.65 V		1.6	3.9	Ω
				Full				4.0	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_{NO} ≤ V_+, I_{COM} = –100 mA,	Switch ON, see 图 13	25°C	1.65 V		2.8		Ω
		V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			4.1	22	
				Full				27	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, see 图 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2		2	μA
				Full		–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 3 V, or V_{COM} = 3 V, V_{NO} = 1 V,	Switch OFF, see 图 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
$I_{COM(PWROFF)}$		V_{COM} = 0 to 3.6 V, V_{NO} = 3.6 V to 0,		25°C	0 V	–2		2	μA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, see 图 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	Switch ON, see 图 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
Digital Control Inputs (IN1, IN2)									
V_{IH}	Input logic high			Full		1.5		5.5	V
V_{IL}	Input logic low			Full		0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	
Dynamic									
t_{ON}	Turnon time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
t_{OFF}	Turnoff time	V_{COM} = V_+, R_L = 50 Ω,	C_L = 35 pF, see 图 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, see 图 21	25°C	1.8 V		2		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_+ or GND, Switch OFF,	See 图 16	25°C	1.8 V		19.5		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_+ or GND, Switch OFF,	See 图 16	25°C	1.8 V		18.5		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

Electrical Characteristics for 1.8-V Supply(1) (continued)

V_+ = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted))

PARAMETER		TEST CONDITIONS		T_A	V_+	MIN	TYP	MAX	UNIT
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_+ or GND, Switch ON,	See 图 16	25°C	1.8 V		36.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_+ or GND, Switch ON,	See 图 16	25°C	1.8 V		36.5		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 图 16	25°C	1.8 V		2		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 图 18	25°C	1.8 V		150		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, see 图 19	25°C	1.8 V		–62		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz see 图 21	25°C	1.8 V		0.055 %		
Supply									
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	μA
				Full				0.15	

6.9 Typical Characteristics

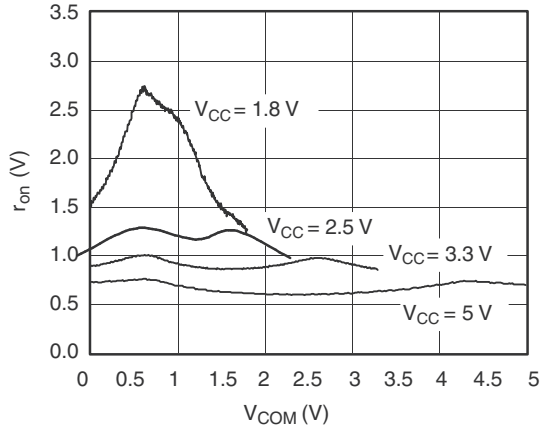


图 1. r_{on} vs V_{COM}

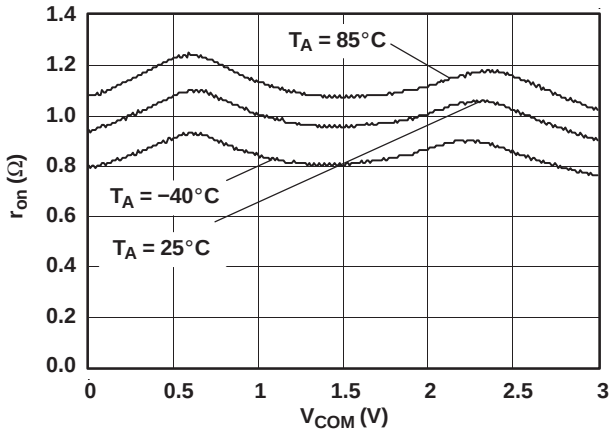


图 2. r_{on} vs V_{COM} (V_+ = 3 V)

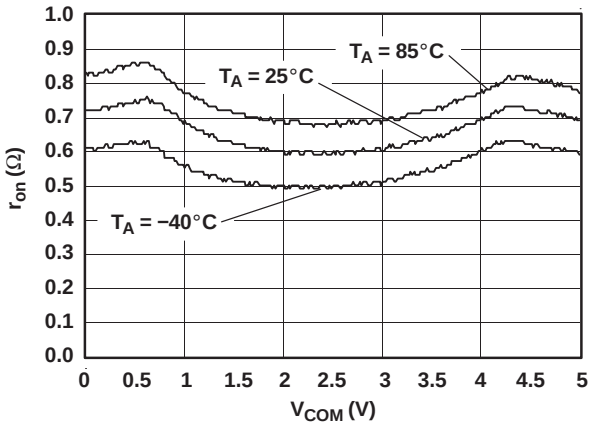


图 3. r_{on} vs V_{COM} (V_+ = 5 V)

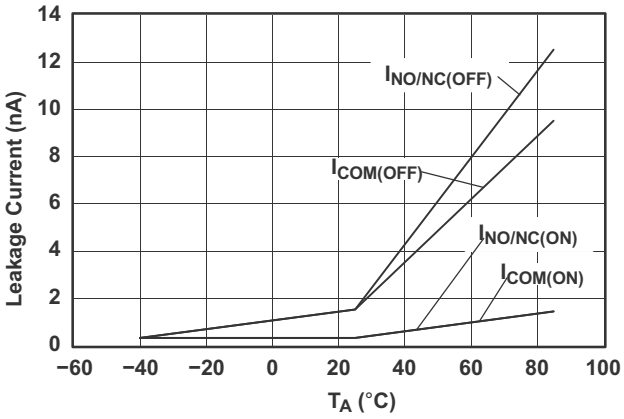


图 4. Leakage Current vs Temperature (V_+ = 5.5 V)

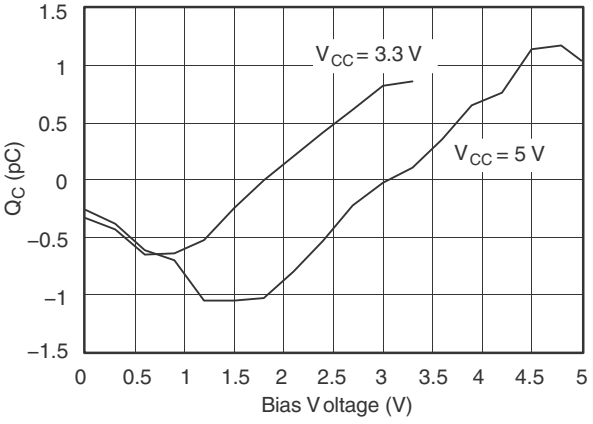


图 5. Charge Injection (Q_C) vs V_{COM}

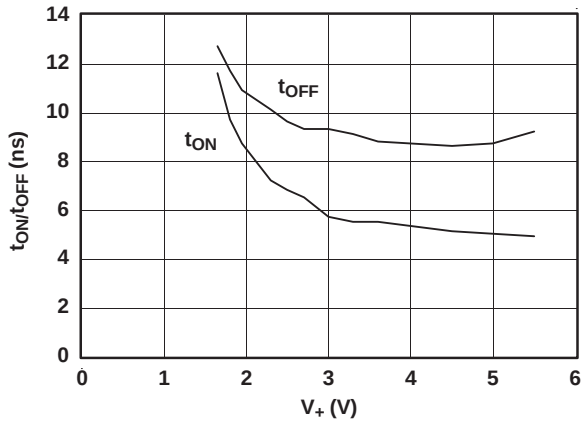


图 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (接下页)

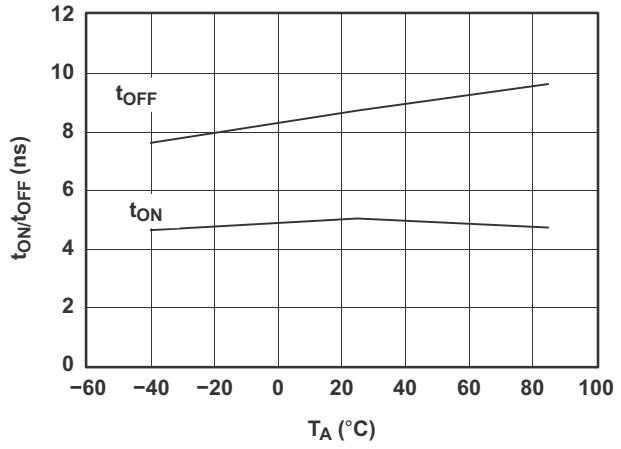


图 7. t_{ON} and t_{OFF} vs Temperature (V_+ = 5 V)

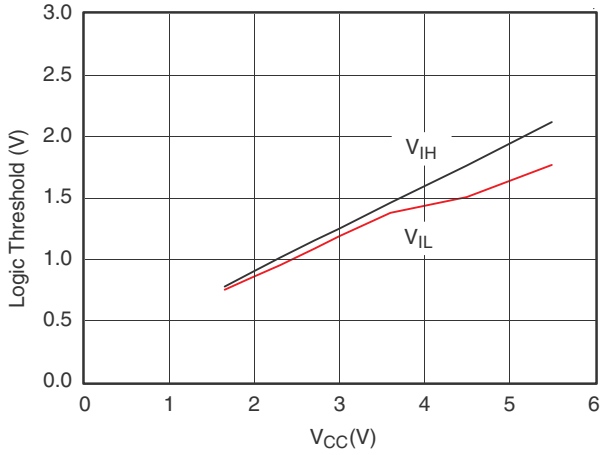


图 8. Logic Threshold vs V_+

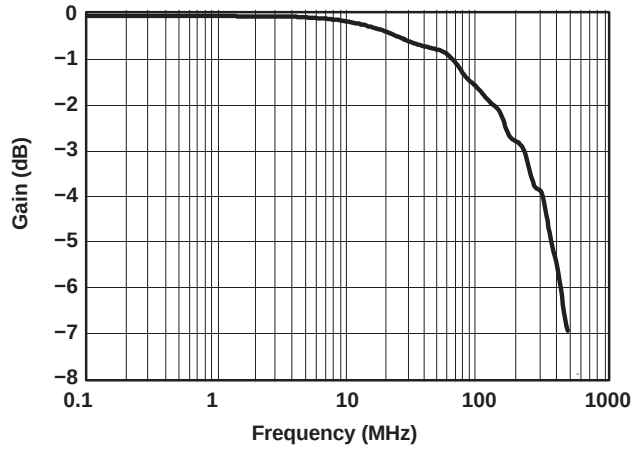


图 9. Gain vs Frequency (V_+ = 5 V)

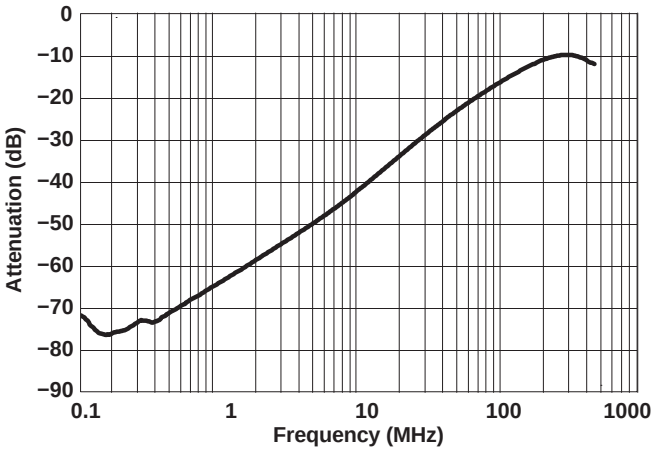


图 10. OFF Isolation vs Frequency (V_+ = 5 V)

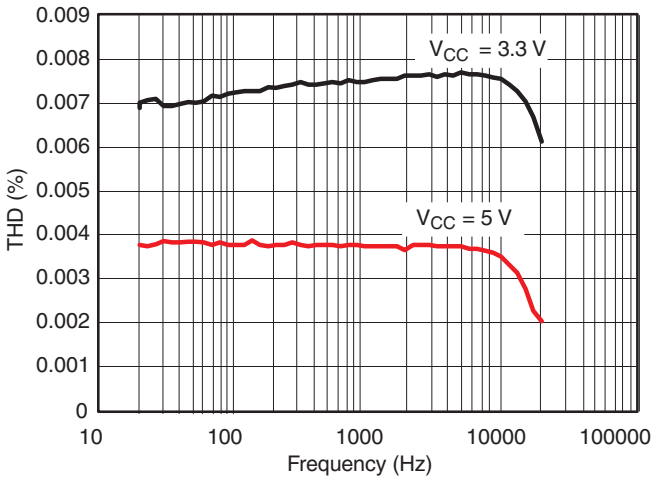


图 11. Total Harmonic Distortion vs Frequency (V_+ = 5 V)

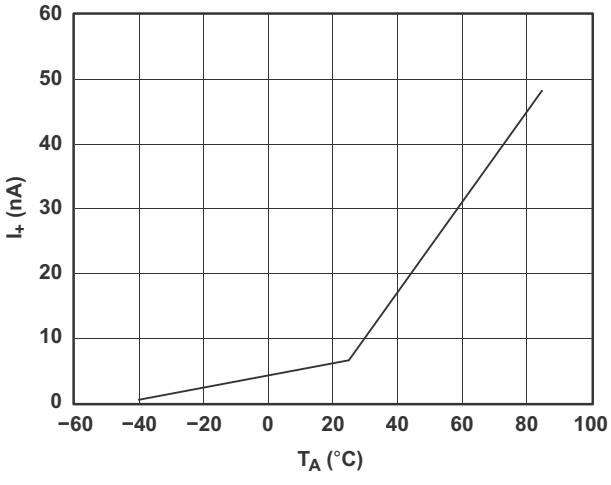
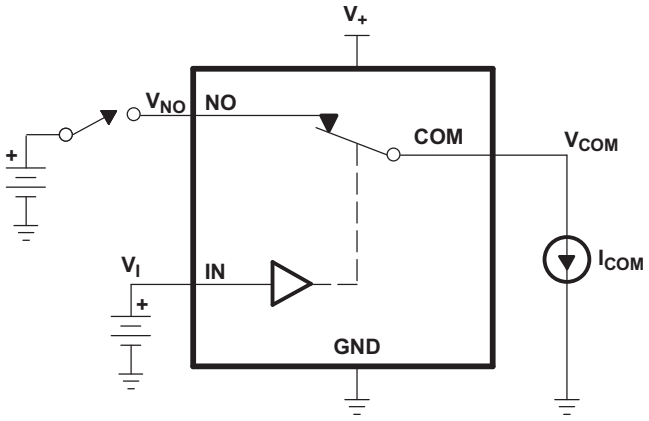


图 12. Power-Supply Current vs Temperature (V_+ = 5 V)

7 Parameter Measurement Information

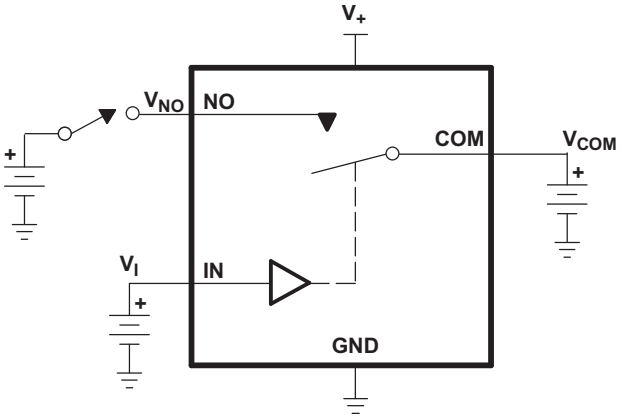


Channel ON

$$r_{on} = \frac{V_{COM} - V_{NC}}{I_{COM}} \Omega$$

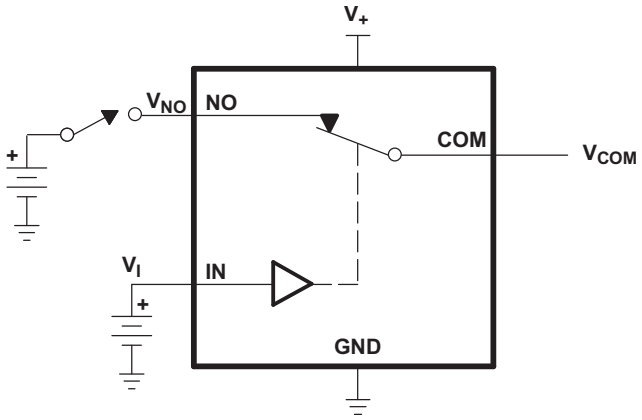
$V_I = V_{IH}$ or V_{IL}

图 13. ON-State Resistance (r_{on})



OFF-State Leakage Current
Channel OFF
$V_I = V_{IH}$ or V_{IL}

图 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$, $I_{COM(PWROFF)}$, $I_{NO(PWR(FF)}$)



ON-State Leakage Current
Channel ON
$V_I = V_{IH}$ or V_{IL}

图 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (接下页)

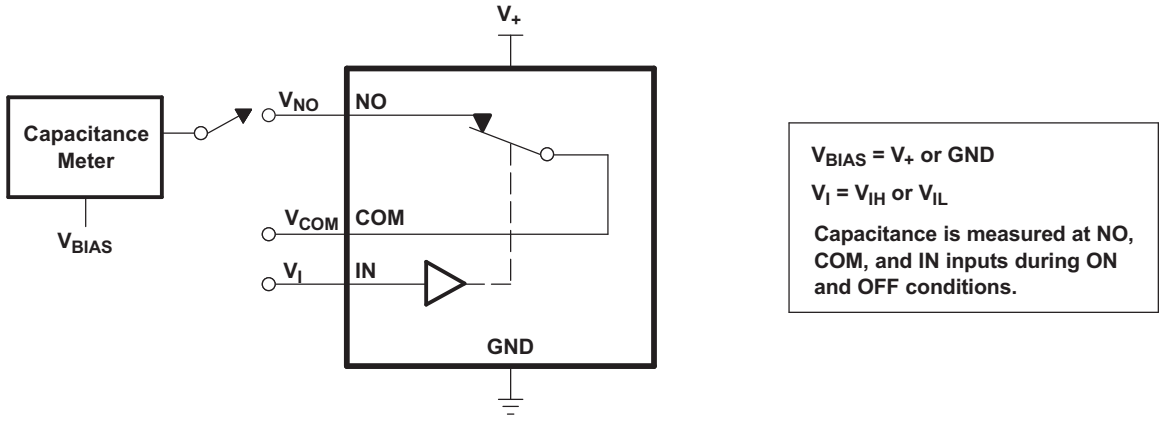
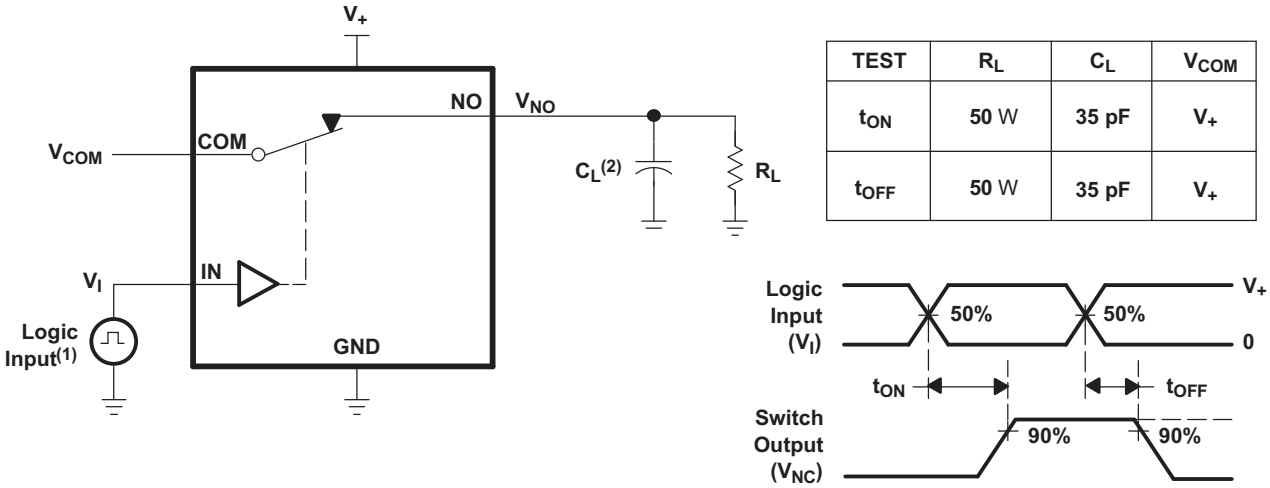


图 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_+
t_{OFF}	50 Ω	35 pF	V_+

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

图 17. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

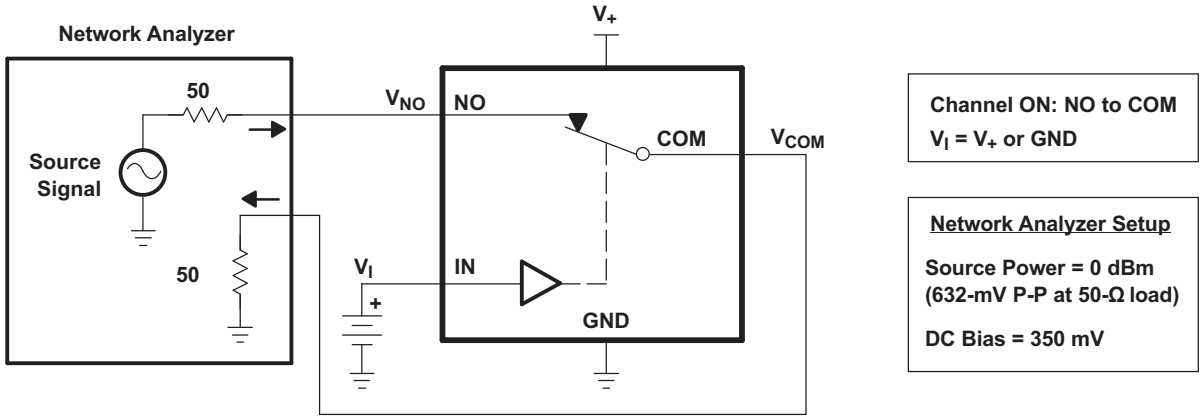


图 18. Bandwidth (BW)

Parameter Measurement Information (接下页)

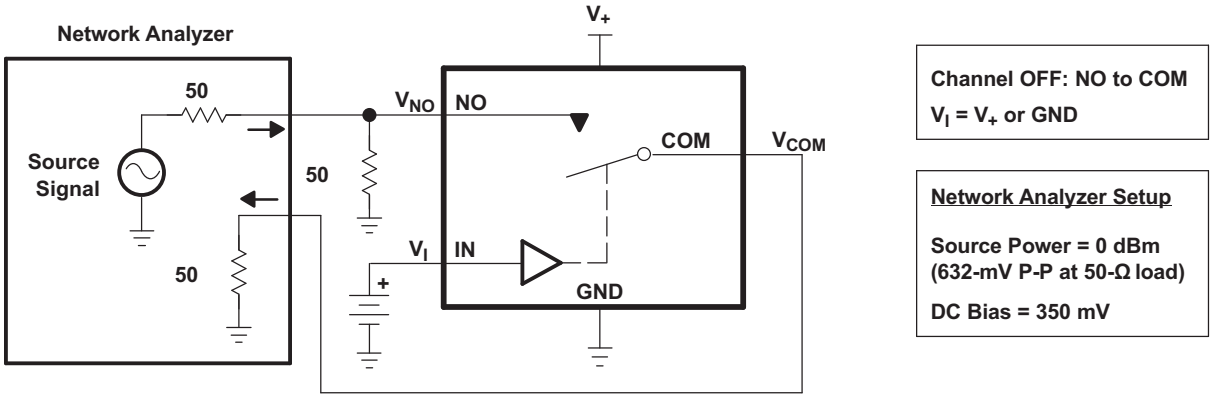
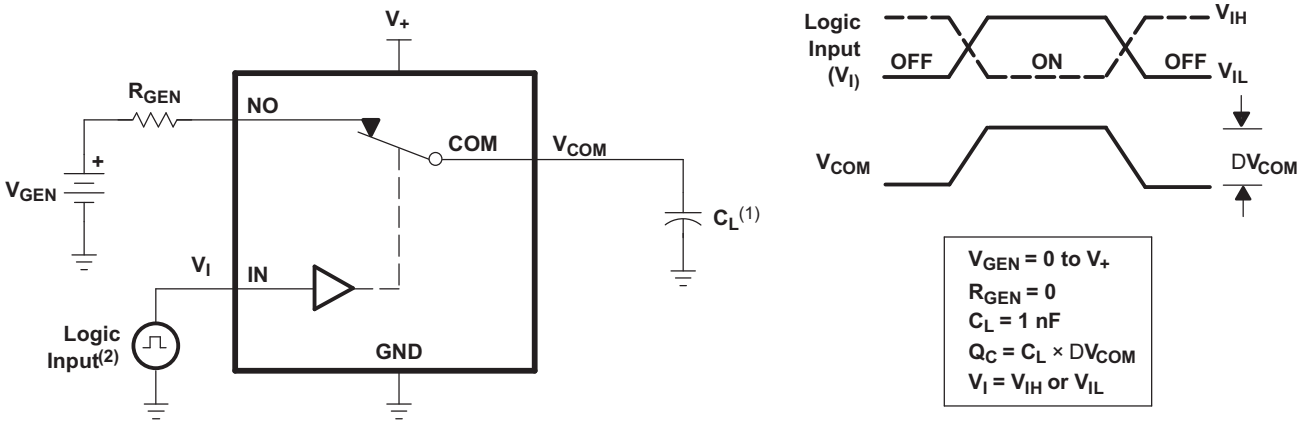


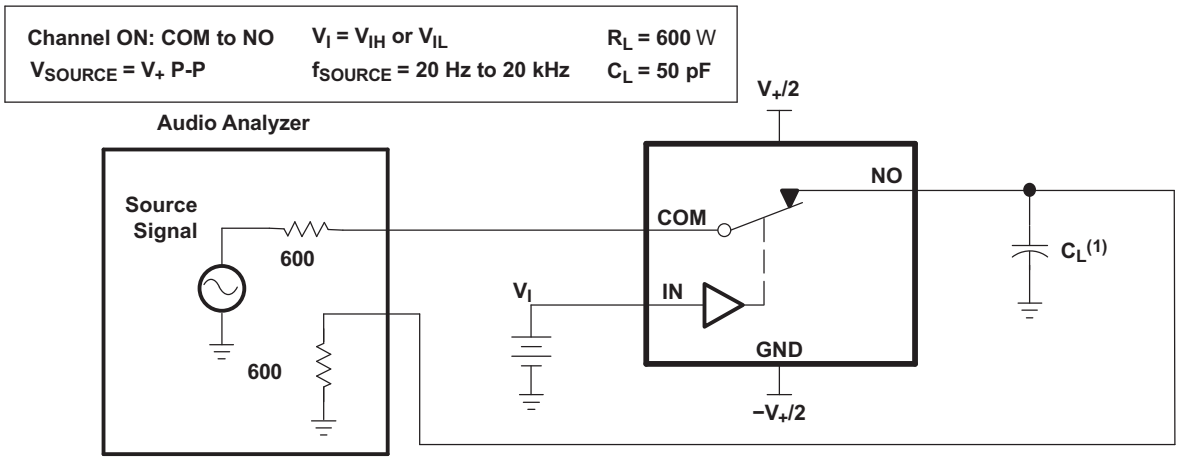
图 19. OFF Isolation (O_{ISO})



(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

图 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

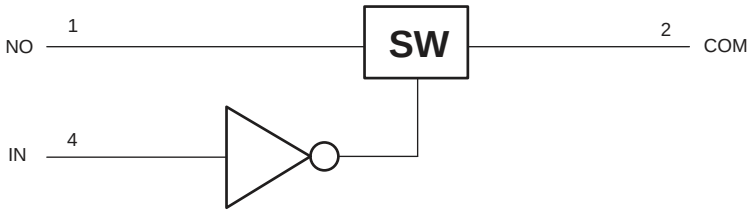
图 21. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A3166 is a single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. The device offers a low ON-state resistance. The device has excellent total harmonic distortion (THD) performance and consumes very low power. These features make this device suitable for portable audio applications.

8.2 Functional Block Diagram



8.3 Feature Description

The low ON-state resistance, ON-state resistance matching, and charge injection in the TS5A3166 make this switch an excellent choice for analog signals that require minimal distortion. In addition, the low THD allows audio signals to be preserved more clearly as they pass through the device.

The 1.65-V to 5.5-V operation allows compatibility with more logic levels, and the bidirectional I/Os can pass analog signals from 0 V to V_+ with low distortion.

8.4 Device Functional Modes

表 1. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

SPST analog switch is a basic component that could be used in any electrical system design. 图 22 and 图 23 are some basic applications that utilize the TS5A3166.

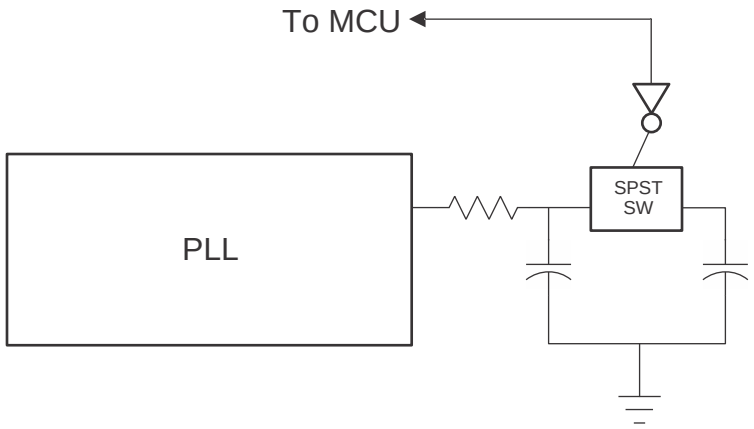


图 22. Improved Lock Time Circuit Simplified Block Diagram

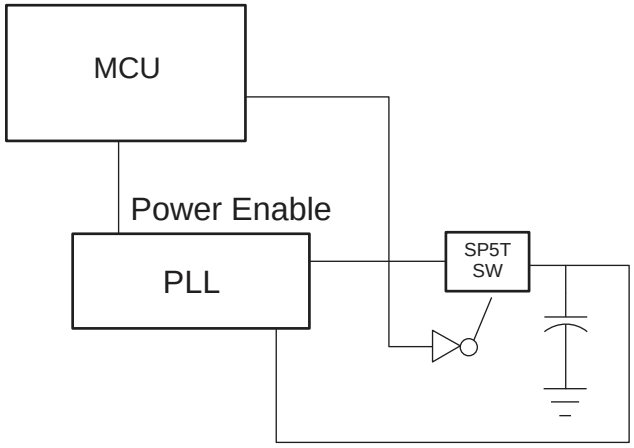


图 23. PLL Improved Power Consumption Simplified Block Diagram

9.2 Typical Application

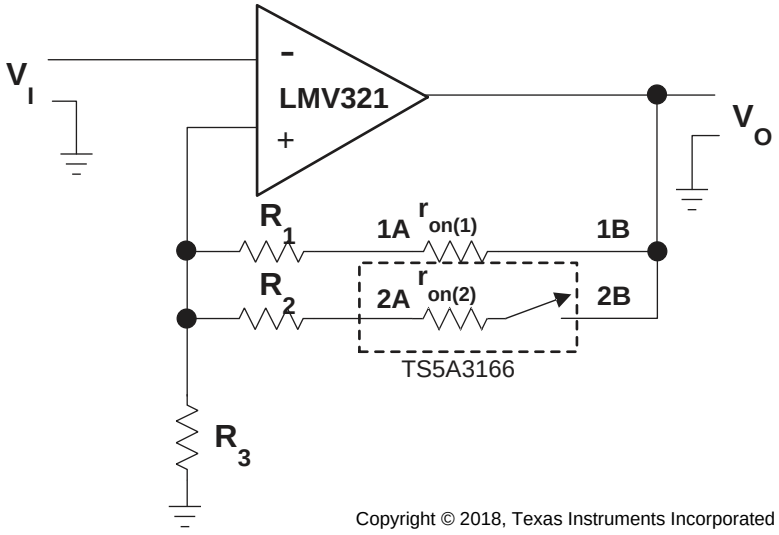


图 24. Gain-Control Circuit for Operational Amplifier

9.2.1 Design Requirements

By choosing values of R1 and R2, such that Rx >> $r_{on(x)}$, r_{on} of TS5A3166 can be ignored. The gain of operational amplifier can be calculated as follow:

$$Vo / VI = 1 + R|| / R3 \quad (1)$$

$$R|| = (R1+r_{on(1)}) \,||\, (R2+r_{on(2)}) \quad (2)$$

9.2.2 Detailed Design Procedure

Place a switch in series with the input of the operational amplifier. Since the operational amplifier input impedance is very large, a switch on $r_{on(1)}$ is irrelevant.

9.2.3 Application Curves

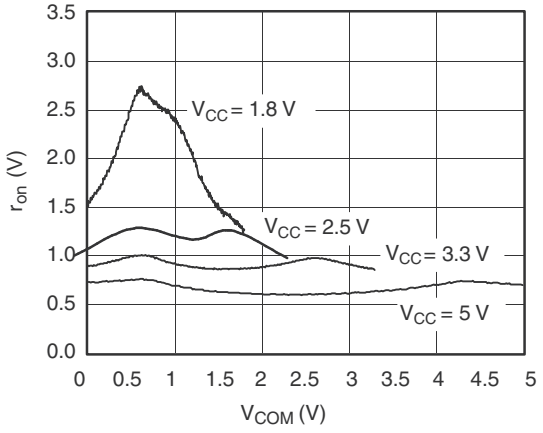


图 25. r_{on} vs V_{COM}

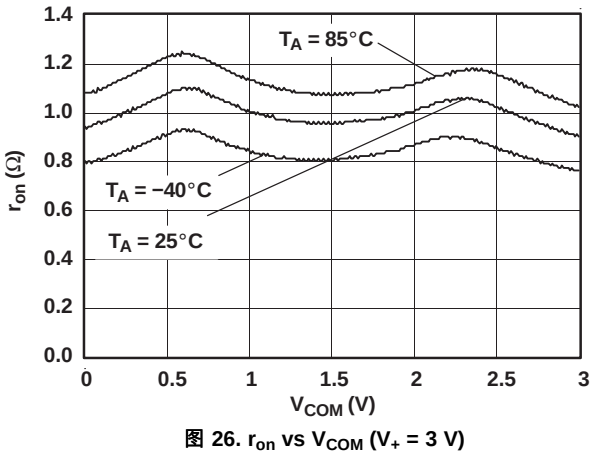


图 26. r_{on} vs V_{COM} (V_+ = 3 V)

Typical Application (接下页)

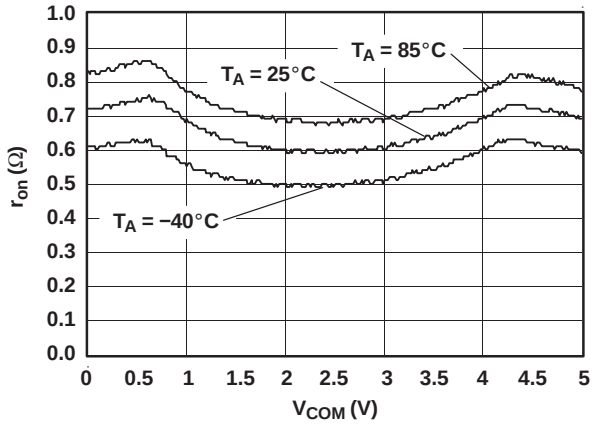


图 27. r_{on} vs V_{COM} (V_+ = 5 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-μF or 0.022-μF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-μF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and so they will have to turn corners. 图 28 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

11.2 Layout Example

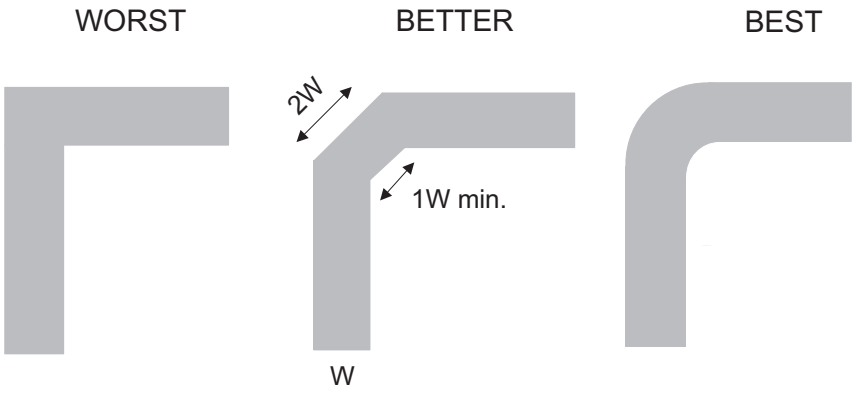


图 28. Trace Example

12 器件和文档支持

12.1 器件支持

12.1.1 器件命名规则

表 **2.** 参数 说明

符号	说明
V_{COM}	COM 时的电压
V_{NO}	NO 时的电压
r_{on}	通道导通时 COM 和 NO 端口之间的电阻
r_{peak}	额定电压范围的导通电阻峰值
$r_{on(flat)}$	额定条件范围下，同一通道内 r_{on} 最大值与最小值之间的差值
$I_{NO(OFF)}$	在最不理想的输入和输出条件下，相应通道（NO 到 COM）处于关断状态时，在 NO 端口测得的泄漏电流
$I_{NO(PWROFF)}$	在电源关断状态下，$V_+ = 0$ 时，在 NO 端口测量的泄漏电流
$I_{COM(OFF)}$	在最不理想的输入和输出条件下，相应通道（COM 到 NO）处于关断状态时，在 COM 端口测得的泄漏电流
$I_{COM(PWROFF)}$	在电源关断状态下，$V_+ = 0$ 时，在 COM 端口测量的泄漏电流
$I_{NO(ON)}$	相应通道（NO 到 COM）处于导通状态且输出 (COM) 处于开路状态时，在 NO 端口测得的泄漏电流
$I_{COM(ON)}$	相应通道（COM 到 NO）处于导通状态且输出 (NO) 处于开路状态时，在 COM 端口测得的泄漏电流
V_{IH}	控制输入 (IN) 逻辑高电平的最小输入电压
V_{IL}	控制输入 (IN) 逻辑低电平的最大输入电压
V_I	控制输入 (IN) 处的电压
I_{IH}、I_{IL}	控制输入 (IN) 处测量的泄漏电流
t_{ON}	开关导通时间。此参数是在特定条件范围下，开关导通时，通过数字控制 (IN) 信号和模拟输出（COM 或 NO）信号之间的传播延迟测量得出。
t_{OFF}	开关关断时间。此参数是在特定条件范围下，开关关断时，通过数字控制 (IN) 信号和模拟输出（COM 或 NO）信号之间的传播延迟测量得出。
Q_C	电荷注入是对从控制 (IN) 输入到模拟（NO 或 COM）输出产生的多余信号耦合的度量。电荷注入以库仑为单位，可通过测量开关控制输入产生的总感应电荷得出该值。电荷注入，$Q_C = C_L \times \Delta V_{COM}$，$C_L$ 是负载电容，ΔV_{COM} 是模拟输出电压的变化。
$C_{NO(OFF)}$	相应通道（NO 到 COM）关断时 NO 端口的电容
$C_{COM(OFF)}$	相应通道（COM 到 NO）关断时 COM 端口的电容
$C_{NO(ON)}$	相应通道（NO 到 COM）导通时 NO 端口的电容
$C_{COM(ON)}$	相应通道（COM 到 NO）导通时 COM 端口的电容
C_I	控制输入 (IN) 电容
O_{ISO}	开关关断隔离用于衡量关断状态开关阻抗的大小。关断隔离以 dB 为单位，当相应通道（NO 到 COM）处于关断状态时，在特定频率下测量得出。
BW	开关的带宽。这是导通通道增益低于直流增益 -3dB 时的频率。
THD	总谐波失真描述由模拟开关导致的信号失真。其定义为基础谐波的第二、第三或更高谐波与基础谐波的绝对幅度的均方根 (RMS) 的比值。
I_+	静态电源电流，以及 V_+ 或 GND 的控制 (IN) 引脚

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3166DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JASF, JASR)	Samples
TS5A3166DBVRG4	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	JASF	
TS5A3166DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)	Samples
TS5A3166DCKRE4	LIFEBUY	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)	
TS5A3166DCKRG4	LIFEBUY	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JF5, JFF, JFR)	
TS5A3166YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JFN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TS5A3166 :

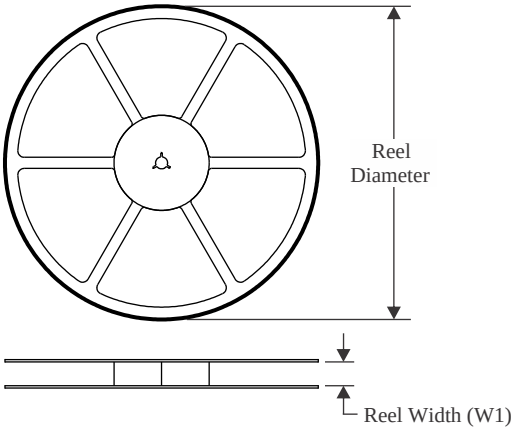
- Automotive : TS5A3166-Q1

NOTE: Qualified Version Definitions:

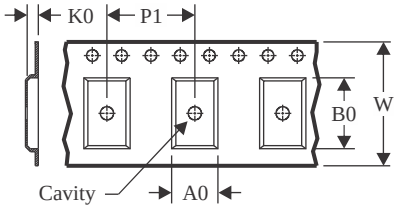
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

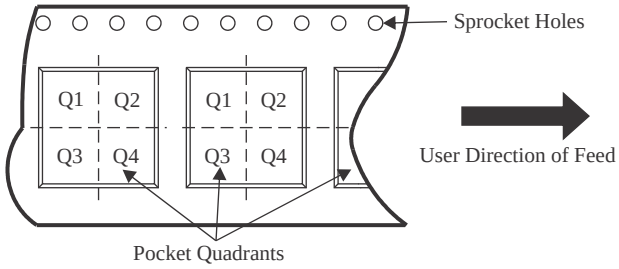


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

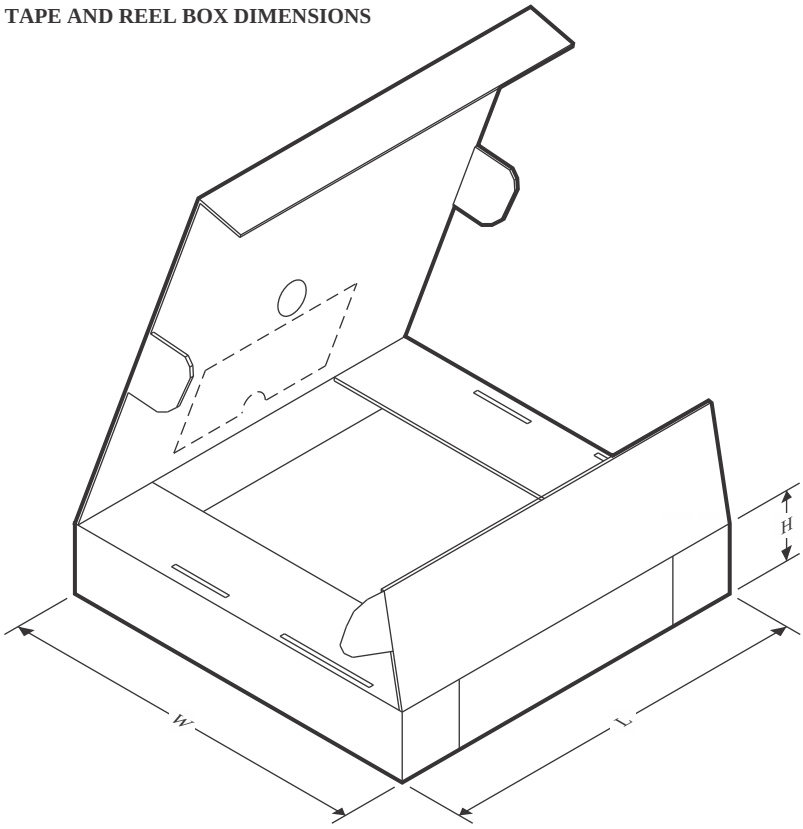
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
TS5A3166DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
TS5A3166YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

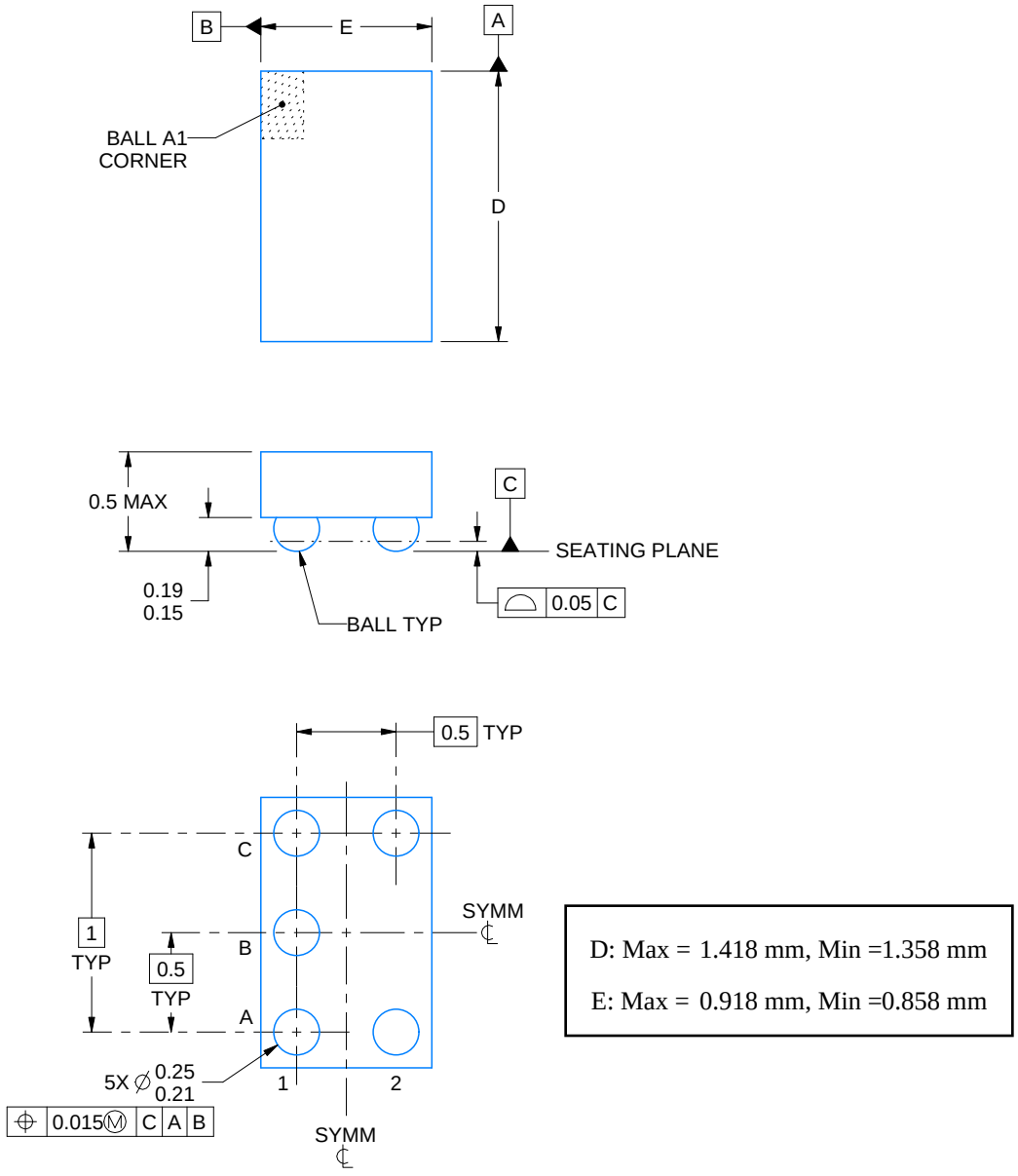
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3166DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TS5A3166DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3166DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3166DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3166DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3166DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
TS5A3166YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

PACKAGE OUTLINE

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



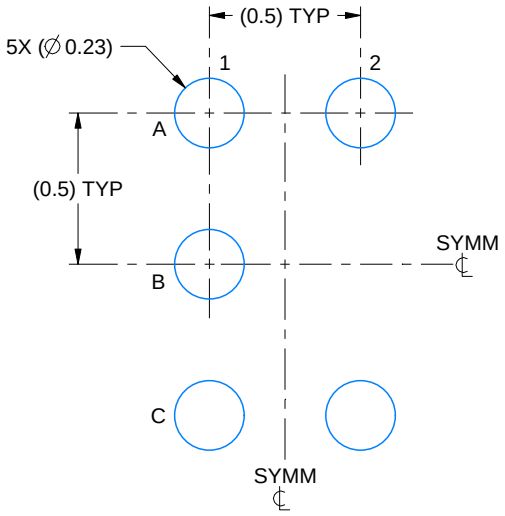
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

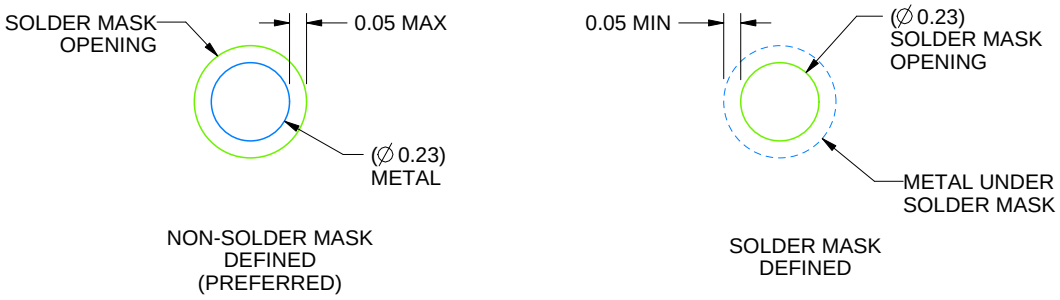
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

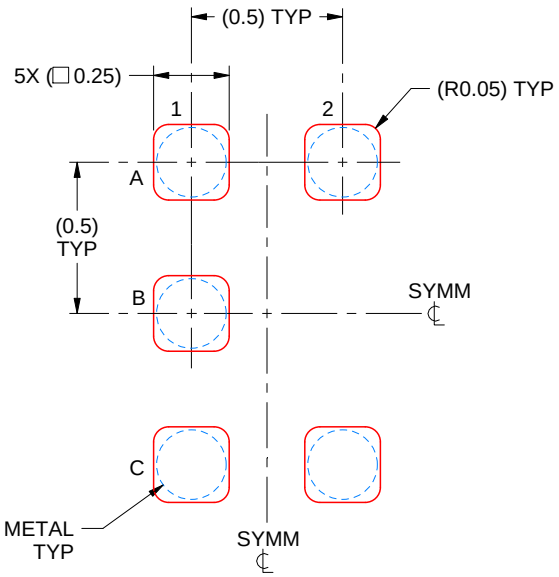


SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

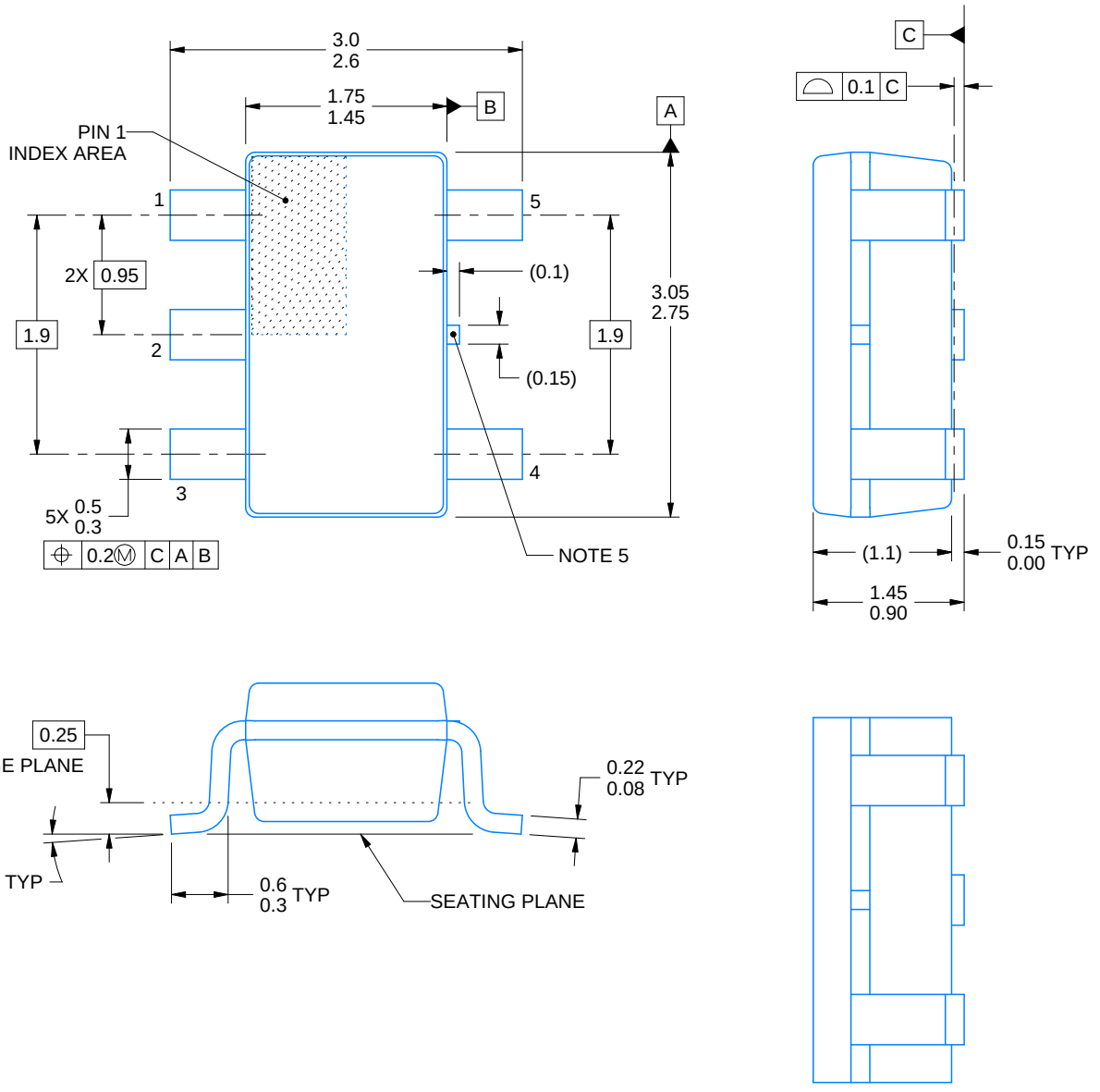
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

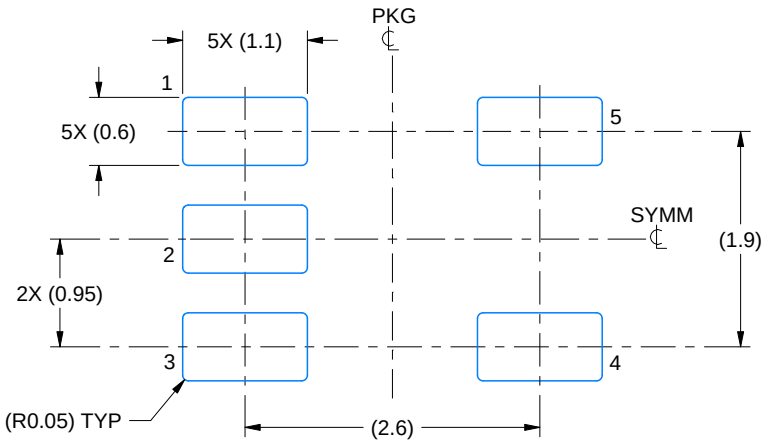


ALTERNATIVE PACKAGE SINGULATION VIEW

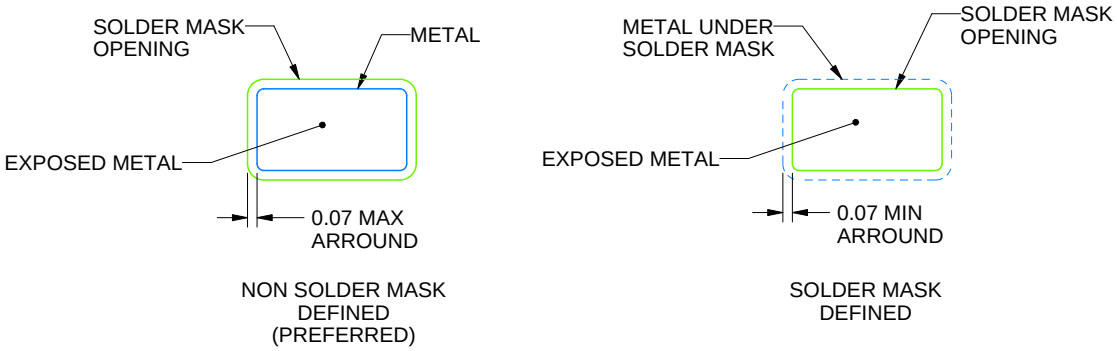
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

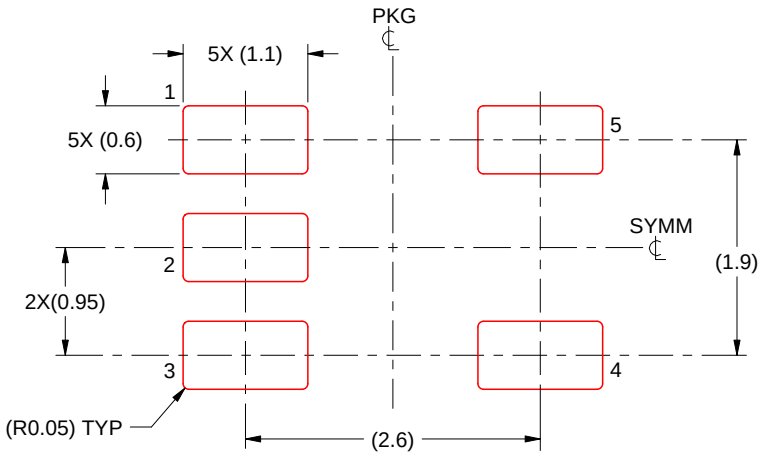


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

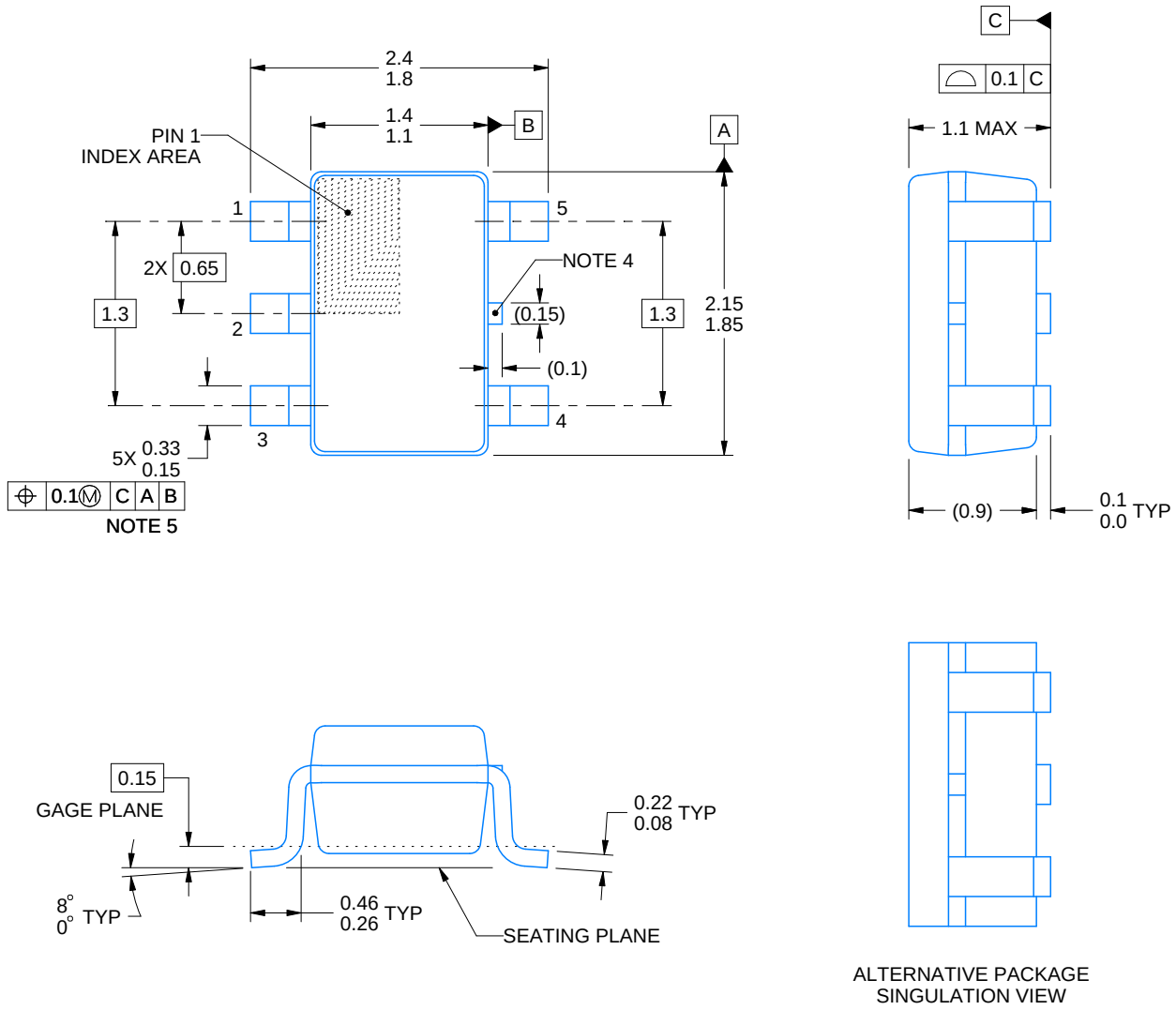
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

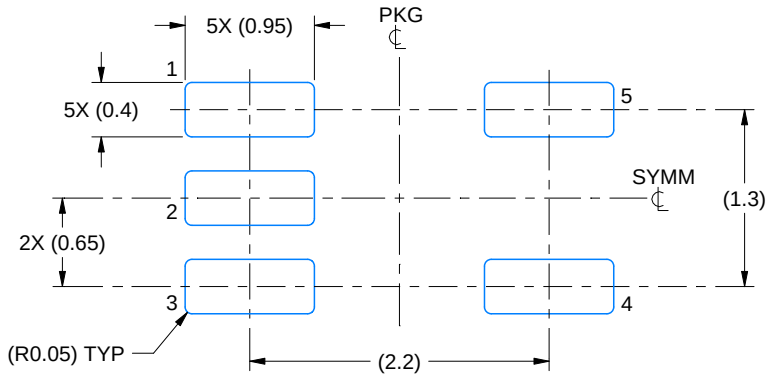
SMALL OUTLINE TRANSISTOR



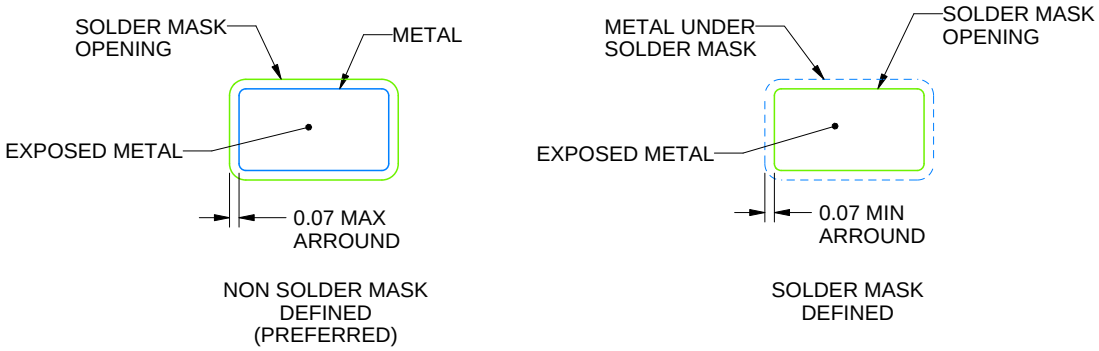
4214834/E 06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

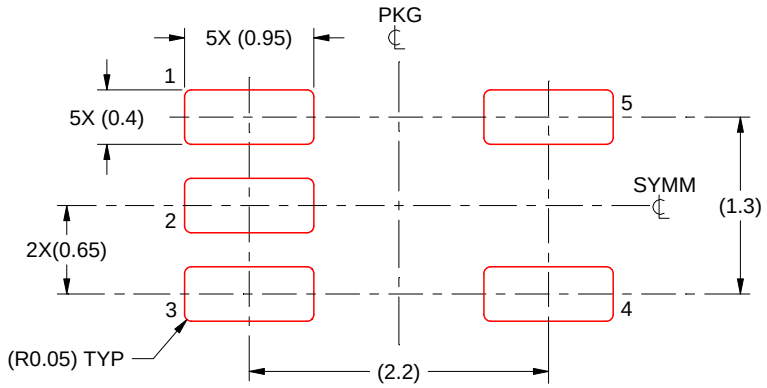


SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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