

# TLV237x 具有关断功能的 500- $\mu$ A/Ch、3-MHz 轨至轨输入和输出运算放大器

## 1 特性

- 轨至轨输入和输出
- 带宽宽：3MHz
- 高转换率：2.4 V/ $\mu$ s
- 高输出驱动：105mA
- 电源电压范围：2.7V 至 16V
- 电源电流：550 $\mu$ A/通道
- 低功耗关断模式
  - $I_{DD(SHDN)}$ : 25 $\mu$ A/通道
- 输入偏置电流：1pA
- 输入噪声电压：39nV/ $\sqrt{\text{Hz}}$
- 单位增益稳定
- 额定温度范围：
  - -40°C 至 +125°C（工业级）
- 超小型封装：
  - 5 引脚或 6 引脚 SOT-23（TLV2370、TLV2371）
  - 8 引脚或 10 引脚 VSSOP（TLV2372、TLV2373）

## 2 应用

- 白色家电
- 手持测试设备
- 便携式血糖仪
- 远程感测
- 有源滤波器
- 工业自动化
- 电池供电型电子产品

## 3 说明

TLV237x 单电源运算放大器具有轨至轨输入和输出功能。TLV237x 在扩展级工业温度范围内的最小工作电源电压低至 2.7V，同时还增添了轨到轨输出摆幅特性。TLV237x 可由低至仅 550 $\mu$ A 的电流提供 3MHz 带宽。最大建议电源电压为 16V，由此，器件可以由多种可充电电池供电运行（支持  $\pm 8V$  低至  $\pm 1.35V$  的电源）。

适用于高阻抗传感器接口的 CMOS 输入特性以及低压运行功能使其成为电池供电应用中 TLV227x 的理想替代器件。轨到轨输入级进一步增强了其多功能性。

TLV237x 是 TI 快速发展的 RRIO 产品中推出的第七款器件，也是首款具有出色交流性能且可支持高达 16V 电源轨的器件。

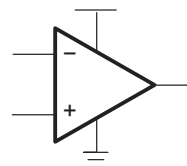
该系列所有产品均采用 PDIP 与 SOIC 封装，单通道器件采用小型 SOT-23 封装，双通道器件采用 MSOP 封装，四通道产品采用 TSSOP 封装。TLV237x 可在 2.7V 电压下运行，兼容锂离子电池供电系统和当今多种低功耗微控制器工作电源电压范围，包括 TI 的 MSP430。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸（标称值）
TLV237x	PDIP (8)	9.81mm x 6.35mm
	PDIP (14)	19.30mm x 6.35mm
	SOIC (8)	4.90mm x 3.91mm
	SOIC (14)	8.65mm x 3.91mm
	TSSOP (14)	5.00mm x 4.40mm
	TSSOP (16)	
	SOT-23 (6)	2.90mm x 1.60mm
	SOT-23 (5)	
	VSSOP (8)	3.00mm x 3.00mm
	VSSOP (10)	

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

运算放大器



## 目录

1	特性 .....	1	9.2	Functional Block Diagram .....	25
2	应用 .....	1	9.3	Feature Description .....	26
3	说明 .....	1	9.4	Device Functional Modes .....	27
4	修订历史记录 .....	2	<b>10</b>	<b>Application and Implementation .....</b>	<b>28</b>
5	<b>Device Comparison Tables .....</b>	<b>3</b>	10.1	Application Information .....	28
6	<b>Pin Configuration and Functions .....</b>	<b>4</b>	10.2	Typical Application .....	28
7	<b>Specifications .....</b>	<b>9</b>	<b>11</b>	<b>Power Supply Recommendations .....</b>	<b>30</b>
7.1	Absolute Maximum Ratings .....	9	<b>12</b>	<b>Layout .....</b>	<b>30</b>
7.2	Recommended Operating Conditions .....	9	12.1	Layout Guidelines .....	30
7.3	Thermal Information: TLV2370 .....	10	12.2	Layout Example .....	31
7.4	Thermal Information: TLV2371 .....	10	12.3	Power Dissipation Considerations .....	32
7.5	Thermal Information: TLV2372 .....	10	<b>13</b>	<b>器件和文档支持 .....</b>	<b>33</b>
7.6	Thermal Information: TLV2373 .....	11	13.1	文档支持 .....	33
7.7	Thermal Information: TLV2374 .....	11	13.2	相关链接 .....	33
7.8	Thermal Information: TLV2375 .....	11	13.3	接收文档更新通知 .....	33
7.9	Electrical Characteristics .....	12	13.4	社区资源 .....	33
<b>8</b>	<b>Typical Characteristics .....</b>	<b>18</b>	13.5	商标 .....	33
<b>9</b>	<b>Detailed Description .....</b>	<b>25</b>	13.6	静电放电警告 .....	33
9.1	Overview .....	25	13.7	Glossary .....	33
			<b>14</b>	<b>机械、封装和可订购信息 .....</b>	<b>33</b>

## 4 修订历史记录

Changes from Revision E (May 2016) to Revision F	Page
• Changed names of pins 2 and 3 in TLV2372 D, DGK, and P packages pinout diagram .....	5

Changes from Revision D (January 2005) to Revision E	Page
• 添加了 ESD 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分。 .....	1
• Deleted TLV2370 and TLV2371 Available Options, TLV2372 AND TLV2373 Available Options, and TLV2374 and TLV2375 Available Options tables .....	3
• Deleted Continuous total power dissipation and lead temperature specifications from Absolute Maximum Ratings table ...	9
• Deleted Dissipation Ratings table .....	17

## 5 Device Comparison Tables

**Table 1. Selection of Signal Amplifier Products<sup>(1)</sup>**

DEVICE	V <sub>DD</sub> (V)	V <sub>IO</sub> ( $\mu$ V)	I <sub>Q</sub> /Ch ( $\mu$ A)	I <sub>IB</sub> (pA)	GBW (MHz)	SR (V/ $\mu$ s)	SHUTDOWN	RAIL-TO-RAIL	SINGLES, DUALS, QUADS
TLV237x	2.7 to 16	500	550	1	3	2.4	Yes	I/O	S, D, Q
TLC227x	4 to 16	300	1100	1	2.2	3.6	—	O	D, Q
TLV27x	2.7 to 16	500	550	1	3	2.4	—	O	S, D, Q
TLC27x	3 to 16	1100	675	1	1.7	3.6	—	—	S, D, Q
TLV246x	2.7 to 16	150	550	1300	6.4	1.6	Yes	I/O	S, D, Q
TLV247x	2.7 to 16	250	600	2	2.8	1.5	Yes	I/O	S, D, Q
TLV244x	2.7 to 10	300	725	1	1.8	1.4	—	O	D, Q

(1) Typical values measured at 5 V and 25°C.

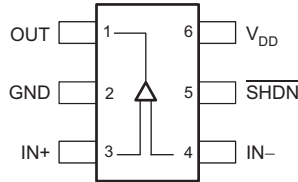
**Table 2. Family Package Table<sup>(1)</sup>**

DEVICE	NUMBER OF CHANNELS	PACKAGE TYPES					SHUTDOWN	UNIVERSAL EVM BOARD
		PDIP	SOIC	SOT-23	TSSOP	MSOP		
TLV2370	1	8	8	6	—	—	Yes	See the <i>EVM Selection Guide</i>
TLV2371	1	8	8	5	—	—	—	
TLV2372	2	8	8	—	—	8	—	
TLV2373	2	14	14	—	—	10	Yes	
TLV2374	4	14	14	—	14	—	—	
TLV2375	4	16	16	—	16	—	Yes	

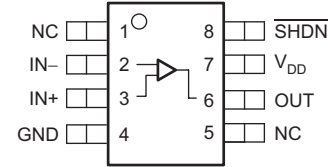
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

## 6 Pin Configuration and Functions

**TLV2370 DBV Package  
6-Pin SOT-23  
Top View**



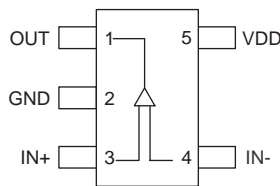
**TLV2370 D and P Packages  
8-Pin SOIC and PDIP  
Top View**



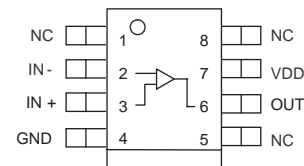
### Pin Functions: TLV2370

NAME	PIN		I/O	DESCRIPTION
	SOT-23	SOIC, PDIP		
GND	2	4	—	Ground connection
IN-	4	2	I	Negative (inverting) input
IN+	3	3	I	Positive (noninverting) input
NC	—	1, 5	—	No internal connection (can be left floating)
OUT	1	6	O	Output
SHDN	5	8	I	Shutdown control (active low, can be left floating)
V <sub>DD</sub>	6	7	—	Positive power supply

**TLV2371 DBV Package  
5-Pin SOT-23  
Top View**



**TLV2371 D and P Packages  
8-Pin SOIC and PDIP  
Top View**

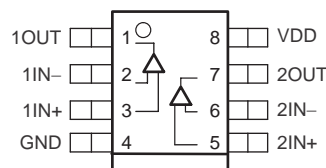


NC- no internal connection

### Pin Functions: TLV2371

NAME	PIN		I/O	DESCRIPTION
	SOT-23	SOIC, PDIP		
GND	2	4	—	Ground connection
IN-	4	2	I	Negative (inverting) input
IN+	3	3	I	Positive (noninverting) input
NC	—	1, 5, 8	—	No internal connection (can be left floating)
OUT	1	6	O	Output
V <sub>DD</sub>	5	7	—	Positive power supply

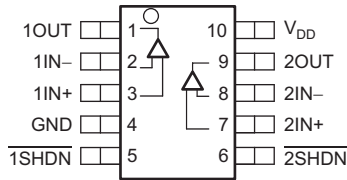
**TLV2372 D, DGK, and P Packages  
8-Pin SOIC, VSSOP, and PDIP  
Top View**



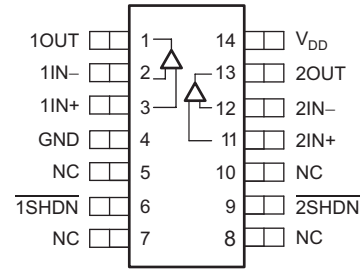
**Pin Functions: TLV2372**

PIN		I/O	DESCRIPTION
NAME	SOIC, VSSOP, PDIP		
GND	4	—	Ground connection
1IN–	2	I	Inverting input, channel 1
1IN+	3	I	Noninverting input, channel 1
2IN–	6	I	Inverting input, channel 2
2IN+	5	I	Noninverting input, channel 2
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
V <sub>DD</sub>	8	—	Positive power supply

**TLV2373 DGS Package  
 10-Pin VSSOP  
 Top View**



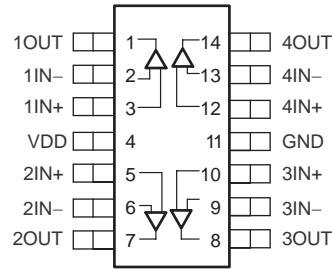
**TLV2373 D and N Packages  
 14-Pin SOIC and PDIP  
 Top View**



**Pin Functions: TLV2373**

NAME	PIN		I/O	DESCRIPTION
	SOIC, PDIP	VSSOP		
GND	4	4	—	Ground connection
1IN-	2	2	I	Inverting input, channel 1
1IN+	3	3	I	Noninverting input, channel 1
2IN-	12	8	I	Inverting input, channel 2
2IN+	11	7	I	Noninverting input, channel 2
1OUT	1	1	O	Output, channel 1
2OUT	13	9	O	Output, channel 2
$\overline{1}$ SHDN	6	5	I	Shutdown control, channel 1, (active low, can be left floating)
$\overline{2}$ SHDN	9	6	I	Shutdown control, channel 2, (active low, can be left floating)
V <sub>DD</sub>	14	10	—	Positive power supply
NC	5, 7, 8, 10	—	—	No internal connection (can be left floating)

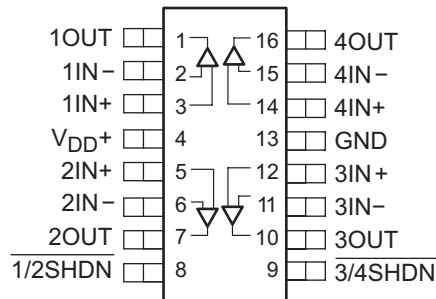
**TLV2374 D, N, and PW Packages  
14-Pin SOIC, PDIP, and TSSOP  
Top View**



**Pin Functions: TLV2374**

PIN		I/O	DESCRIPTION
NAME	SOIC, PDIP, TSSOP		
GND	11	—	Ground connection
1IN-	2	I	Inverting input, channel 1
1IN+	3	I	Noninverting input, channel 1
2IN-	6	I	Inverting input, channel 2
2IN+	5	I	Noninverting input, channel 2
3IN-	9	I	Inverting input, channel 3
3IN+	10	I	Noninverting input, channel 3
4IN-	13	I	Inverting input, channel 4
4IN+	12	I	Noninverting input, channel 4
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
3OUT	8	O	Output, channel 3
4OUT	14	O	Output, channel 4
V <sub>DD</sub>	4	—	Positive power supply

TLV2375 D, N, and PW Packages  
 16-Pin SOIC, PDIP, and TSSOP  
 Top View



Pin Functions: TLV2375

PIN		I/O	DESCRIPTION
NAME	SOIC, PDIP, TSSOP		
GND	13	—	Ground connection
1IN–	2	I	Inverting input, channel 1
2IN–	6	I	Inverting input, channel 2
3IN–	11	I	Inverting input, channel 3
4IN–	15	I	Inverting input, channel 4
1IN+	3	I	Noninverting input, channel 1
2IN+	5	I	Noninverting input, channel 2
3IN+	12	I	Noninverting input, channel 3
4IN+	14	I	Noninverting input, channel 4
1OUT	1	O	Output, channel 1
2OUT	7	O	Output, channel 2
3OUT	10	O	Output, channel 3
4OUT	16	O	Output, channel 4
$\overline{1/2}$ SHDN	8	I	Shutdown control, channels 1 and 2, (active low, can be left floating)
$\overline{3/4}$ SHDN	9	I	Shutdown control, channels 3 and 4, (active low, can be left floating)
V <sub>DD</sub>	4	—	Positive power supply



## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	Supply voltage, $V_{DD}$ <sup>(2)</sup>		16.5	V
	Differential input voltage, $V_{ID}$	$-V_{DD}$	$V_{DD}$	
	Input voltage, $V_I$ <sup>(2)</sup>	-0.2	$V_{DD} + 0.2$	
Current	Input current, $I_{IN}$	-10	10	mA
	Output current, $I_O$	-100	100	
Temperature	Operating free-air temperature, $T_A$ : I-suffix	-40	125	°C
	Maximum junction temperature, $T_J$		150	
	Storage temperature, $T_{stg}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.

### 7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	MAX	UNIT
Supply voltage, $V_{DD}$	Single supply	2.7	16	V
	Split supply	$\pm 1.35$	$\pm 8$	
Common-mode input voltage, $V_{CM}$		0	$V_{DD}$	V
Operating free-air temperature, $T_A$	I-suffix	-40	125	°C
Turnon voltage (shutdown pin voltage level), $V_{(ON)}$ , relative to GND pin voltage			2	V
Turnoff (shutdown pin voltage level), $V_{(OFF)}$ , relative to GND pin voltage		0.8		V

### 7.3 Thermal Information: TLV2370

THERMAL METRIC <sup>(1)</sup>		TLV2370			UNIT
		DBV (SOT-23)	D (SOIC)	P (PDIP)	
		6 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	138.4	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	89.5	39.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	78.6	26.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.7	29.9	15.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	53.8	78.1	26.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.4 Thermal Information: TLV2371

THERMAL METRIC <sup>(1)</sup>		TLV2371			UNIT
		DBV (SOT-23)	D (SOIC)	P (PDIP)	
		5 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.5	138.4	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	99.1	89.5	39.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.6	78.6	26.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	7.7	29.9	15.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	53.8	78.1	26.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 7.5 Thermal Information: TLV2372

THERMAL METRIC <sup>(1)</sup>		TLV2372			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	191.2	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	61.9	39.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	111.9	26.4	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	29.9	5.1	15.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	78.1	110.2	26.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Thermal Information: TLV2373

THERMAL METRIC <sup>(1)</sup>		TLV2373			UNIT
		DGS (VSSOP)	D (SOIC)	P (PDIP)	
		10 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	166.5	67	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.8	24.1	20.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	86.1	22.5	26.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.5	2.2	2.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	84.7	22.1	26.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Thermal Information: TLV2374

THERMAL METRIC <sup>(1)</sup>		TLV2374			UNIT
		D (SOIC)	N (PDIP)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67	66.3	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	20.5	49.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	26.8	62.8	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	2.2	2.1	5.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	22.1	26.2	62.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.8 Thermal Information: TLV2375

THERMAL METRIC <sup>(1)</sup>		TLV2375			UNIT
		D (SOIC)	N (PDIP)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83	55.8	115.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44	43.1	50.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.5	35.8	60.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	11.5	27.9	7.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	40.2	35.7	60.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.9 Electrical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DC PERFORMANCE</b>						
$V_{OS}$	Input offset voltage	At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $V_O = V_{DD}/2$ , $R_S = 50\ \Omega$		2	4.5	mV
		At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $V_O = V_{DD}/2$ , $R_S = 50\ \Omega$			6	mV
$dV_{OS}/dT$	Offset voltage drift	At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $V_O = V_{DD}/2$ , $R_S = 50\ \Omega$		2		$\mu\text{V}/^\circ\text{C}$
CMRR	Common-mode rejection ratio	$V_{DD} = 2.7\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ to $V_{DD}$	50	68	dB
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = 0$ to $V_{DD}$	49		
			$V_{IC} = 0$ to $V_{DD} - 1.35\text{ V}$	56	70	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = 0$ to $V_{DD} - 1.35\text{ V}$	54		
		$V_{DD} = 5\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ to $V_{DD}$	55	72	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = 0$ to $V_{DD}$	54		
			$V_{IC} = 0$ to $V_{DD} - 1.35\text{ V}$	67	80	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = 0$ to $V_{DD} - 1.35\text{ V}$	64		
		$V_{DD} = 15\text{ V}$ , $R_S = 50\ \Omega$	$V_{IC} = 0$ to $V_{DD}$	64	82	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = 0$ to $V_{DD}$	63		
			$V_{IC} = 0$ to $V_{DD} - 1.35\text{ V}$	67	84	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = 0$ to $V_{DD} - 1.35\text{ V}$	66		
$A_{VD}$	Large-signal differential voltage amplification	$V_{DD} = 2.7\text{ V}$ , $V_{O(PP)} = V_{DD}/2$ , $R_L = 10\text{ k}\Omega$		98	106	dB
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	76		
		$V_{DD} = 5\text{ V}$ , $V_{O(PP)} = V_{DD}/2$ , $R_L = 10\text{ k}\Omega$		100	110	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	86		
		$V_{DD} = 15\text{ V}$ , $V_{O(PP)} = V_{DD}/2$ , $R_L = 10\text{ k}\Omega$		81	83	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$	79		
<b>INPUT CHARACTERISTICS</b>						
$I_{OS}$	Input offset current	$V_{DD} = 15\text{ V}$ , $V_{IC} = V_O = V_{DD}/2$		1	60	pA
			At $T_A = 70^\circ\text{C}$		100	
			At $T_A = 125^\circ\text{C}$		1000	
$I_B$	Input bias current	$V_{DD} = 15\text{ V}$ , $V_{IC} = V_O = V_{DD}/2$		1	60	pA
			At $T_A = 70^\circ\text{C}$		100	
			At $T_A = 125^\circ\text{C}$		1000	
	Differential input resistance			1000		$\text{G}\Omega$
	Common-mode input capacitance	$f = 21\text{ kHz}$		8		pF

## Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OUTPUT CHARACTERISTICS</b>					

### Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$V_{DD} = 2.7\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$	2.55	2.58		
		$V_{DD} = 2.7\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$	2.48			
		$V_{DD} = 5\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$	4.9	4.93		
		$V_{DD} = 5\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$	4.85			
		$V_{DD} = 15\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$	14.92	14.96		
		$V_{DD} = 15\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -1\text{ mA}$	14.9			
		$V_{DD} = 2.7\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -5\text{ mA}$	1.9	2		V
		$V_{DD} = 2.7\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -5\text{ mA}$	1.6			
		$V_{DD} = 5\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -5\text{ mA}$	4.6	4.68		
		$V_{DD} = 5\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -5\text{ mA}$	4.5			
		$V_{DD} = 15\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -5\text{ mA}$	14.7	14.8		
		$V_{DD} = 15\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OH} = -5\text{ mA}$	14.6			
$V_{OL}$	Low-level output voltage	$V_{DD} = 2.7\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$		0.1	0.15	
		$V_{DD} = 2.7\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$			0.22	
		$V_{DD} = 5\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$		0.05	0.1	
		$V_{DD} = 5\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$			0.15	
		$V_{DD} = 15\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$		0.05	0.08	
		$V_{DD} = 15\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 1\text{ mA}$			0.1	
		$V_{DD} = 2.7\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 5\text{ mA}$		0.52	0.7	V
		$V_{DD} = 2.7\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 5\text{ mA}$			1.1	
		$V_{DD} = 5\text{ V}$ At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 5\text{ mA}$		0.28	0.4	
		$V_{DD} = 5\text{ V}$ At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 5\text{ mA}$			0.5	

**Electrical Characteristics (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	At $T_A = 25^\circ\text{C}$ , $V_{IC} = V_{DD}/2$ , $I_{OL} = 5\text{ mA}$			UNIT
		MIN	TYP	MAX	
	$V_{DD} = 15\text{ V}$			0.35	
$I_O$ Output current	$V_{DD} = 2.7\text{ V}$ , $V_O = 0.5\text{ V}$ from rail	Positive rail		4	mA
		Negative rail		5	
	$V_{DD} = 5\text{ V}$ , $V_O = 0.5\text{ V}$ from rail	Positive rail		7	
		Negative rail		8	
	$V_{DD} = 15\text{ V}$ , $V_O = 0.5\text{ V}$ from rail	Positive rail		16	
		Negative rail		15	

### Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>POWER SUPPLY</b>							
$I_{DD}$	Supply current (per channel)	$V_{DD} = 2.7\text{ V}$ , $V_O = V_{DD}/2$			470	560	$\mu\text{A}$
		$V_{DD} = 5\text{ V}$ , $V_O = V_{DD}/2$			550	660	
		$V_{DD} = 15\text{ V}$ , $V_O = V_{DD}/2$	At $T_A = 25^\circ\text{C}$			750	
At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$					1200		
PSRR	Power-supply rejection ratio ( $\Delta V_{DD}/\Delta V_{IO}$ )	$V_{DD} = 2.7\text{ V}$ to $15\text{ V}$ , $V_{IC} = V_{DD}/2$ , no load	At $T_A = 25^\circ\text{C}$		70	80	dB
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		65		
<b>DYNAMIC PERFORMANCE</b>							
UGBW	Unity gain bandwidth	$V_{DD} = 2.7\text{ V}$	$R_L = 2\text{ k}\Omega$ , $C_L = 10\text{ pF}$			2.4	MHz
		$V_{DD} = 5\text{ V}$ to $15\text{ V}$		$R_L = 2\text{ k}\Omega$ , $C_L = 10\text{ pF}$			
SR	Slew rate at unity gain	$V_{DD} = 2.7\text{ V}$	At $T_A = 25^\circ\text{C}$ , $V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1.4	2	V/ $\mu\text{s}$
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1		
		$V_{DD} = 5\text{ V}$	At $T_A = 25^\circ\text{C}$ , $V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1.6	2.4	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1.2		
$V_{DD} = 15\text{ V}$	At $T_A = 25^\circ\text{C}$ , $V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1.9	2.1			
	At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , $V_{O(PP)} = V_{DD}/2$ , $C_L = 50\text{ pF}$ , $R_L = 10\text{ k}\Omega$		1.4				
$\phi_m$	Phase margin	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$			65		$^\circ$
	Gain margin	$R_L = 2\text{ k}\Omega$ , $C_L = 10\text{ pF}$			18		dB
$t_s$	Settling time	$V_{DD} = 2.7\text{ V}$ , $V_{(STEP)PP} = 1\text{ V}$ , $A_V = -1$ , $C_L = 10\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $0.1\%$			2.9		$\mu\text{s}$
		$V_{DD} = 5\text{ V}$ , $15\text{ V}$ , $V_{(STEP)PP} = 1\text{ V}$ , $A_V = -1$ , $C_L = 47\text{ pF}$ , $R_L = 2\text{ k}\Omega$ , $0.1\%$			2		



## Electrical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 2.7\text{ V}$ ,  $5\text{ V}$ , and  $15\text{ V}$  (unless otherwise noted).

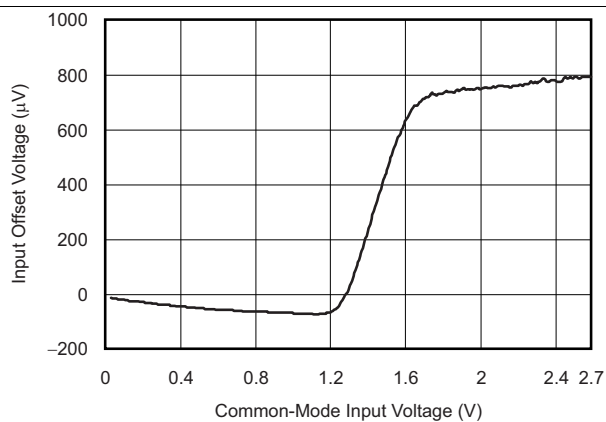
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>NOISE, DISTORTION PERFORMANCE</b>							
THD + N	Total harmonic distortion plus noise	$V_{DD} = 2.7\text{ V}$	$V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ , $A_V = 1$		0.02%		
			$V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ , $A_V = 10$		0.05%		
			$V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ , $A_V = 100$		0.18%		
		$V_{DD} = 5\text{ V}$ , $15\text{ V}$	$V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ , $A_V = 1$		0.02%		
			$V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ , $A_V = 10$		0.09%		
			$V_{O(PP)} = V_{DD}/2\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $f = 10\text{ kHz}$ , $A_V = 100$		0.5%		
$V_n$	Equivalent input noise voltage	$f = 1\text{ kHz}$			39		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$			35		
$I_n$	Equivalent input noise current	$f = 1\text{ kHz}$			0.6		$\text{fA}/\sqrt{\text{Hz}}$
<b>SHUTDOWN CHARACTERISTICS</b>							
$I_{DD(\text{SHDN})}$	Supply current in shutdown mode (TLV2370, TLV2373, TLV2375) (per channel)	$V_{DD} = 2.7\text{ V}$ , $5\text{ V}$ , SHDN = $0\text{ V}$	At $T_A = 25^\circ\text{C}$		25	30	$\mu\text{A}$
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			35	
		$V_{DD} = 15\text{ V}$ , SHDN = $0\text{ V}$	At $T_A = 25^\circ\text{C}$		40	45	
			At $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			50	
$t_{(\text{on})}$	Amplifier turnon time <sup>(1)</sup>	$R_L = 2\text{ k}\Omega$			0.8		$\mu\text{s}$
$t_{(\text{off})}$	Amplifier turnoff time <sup>(1)</sup>	$R_L = 2\text{ k}\Omega$			1		$\mu\text{s}$

- (1) Disable time and enable time are defined as the interval between application of the logic signal to the SHDN terminal and the point at which the supply current has reached one half of its final value.

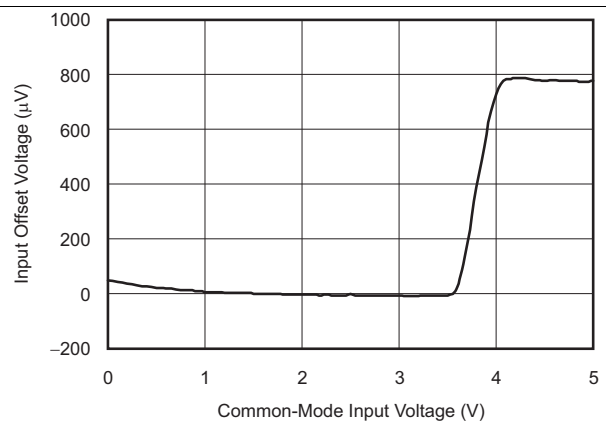
## 8 Typical Characteristics

**Table 3. Table of Graphs**

			FIGURE
$V_{IO}$	Input offset voltage	vs Common-mode input voltage	Figure 1, Figure 2, Figure 3
CMRR	Common-mode rejection ratio	vs Frequency	Figure 4
	Input bias and offset current	vs Free-air temperature	Figure 5
$V_{OL}$	Low-level output voltage	vs Low-level output current	Figure 6, Figure 8, Figure 10
$V_{OH}$	High-level output voltage	vs High-level output current	Figure 7, Figure 9, Figure 11
$V_{O(PP)}$	Peak-to-peak output voltage	vs Frequency	Figure 12
$I_{DD}$	Supply current	vs Supply voltage	Figure 13
PSRR	Power supply rejection ratio	vs Frequency	Figure 14
$A_{VD}$	Differential voltage gain and phase	vs Frequency	Figure 15
	Gain-bandwidth product	vs Free-air temperature	Figure 16
SR	Slew rate	vs Supply voltage	Figure 17
		vs Free-air temperature	Figure 18
$\phi_m$	Phase margin	vs Capacitive load	Figure 19
$V_n$	Equivalent input noise voltage	vs Frequency	Figure 20
	Voltage-follower large-signal pulse response		Figure 21, Figure 22
	Voltage-follower small-signal pulse response		Figure 23
	Inverting large-signal response		Figure 24, Figure 25
	Inverting small-signal response		Figure 26
	Crosstalk	vs Frequency	Figure 27
	Shutdown forward & reverse isolation	vs Frequency	Figure 28
$I_{DD(SHDN)}$	Shutdown supply current	vs Supply voltage	Figure 29
$I_{DD(SHDN)}$	Shutdown pin leakage current	vs Shutdown pin voltage	Figure 30
$I_{DD(SHDN)}$	Shutdown supply current, output voltage	vs Time	Figure 31, Figure 32



**Figure 1. Input Offset Voltage vs Common-Mode Input Voltage**



**Figure 2. Input Offset Voltage vs Common-Mode Input Voltage**

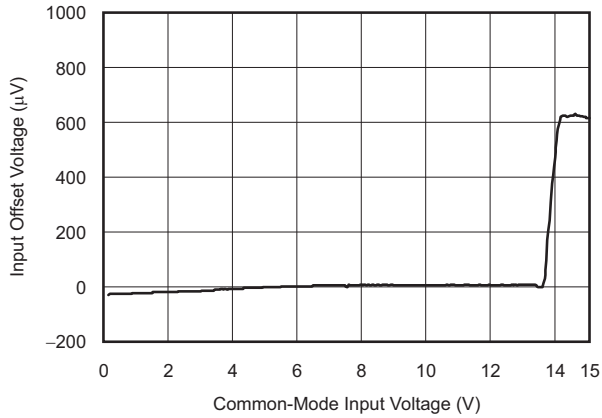


Figure 3. Input Offset Voltage vs Common-Mode Input Voltage

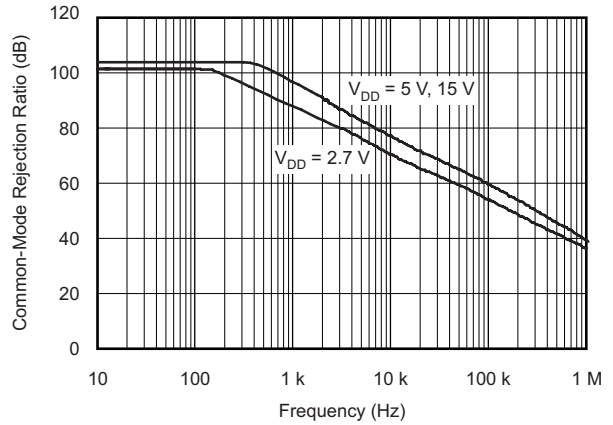


Figure 4. Common-Mode Rejection Ratio vs Frequency

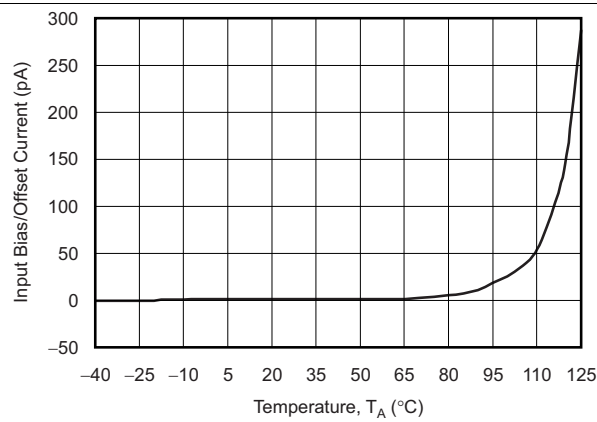


Figure 5. Input Bias or Offset Current vs Free-Air Temperature

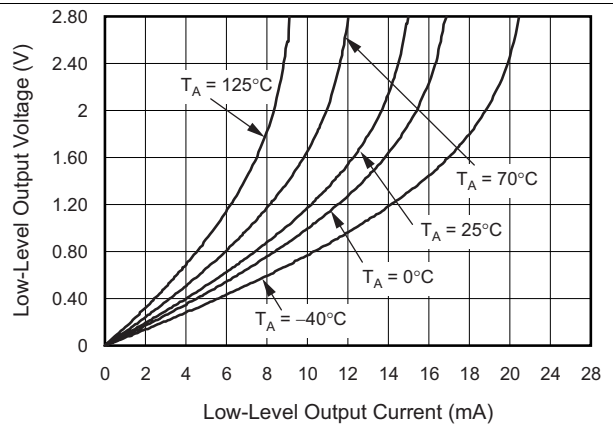


Figure 6. Low-Level Output Voltage vs Low-Level Output Current

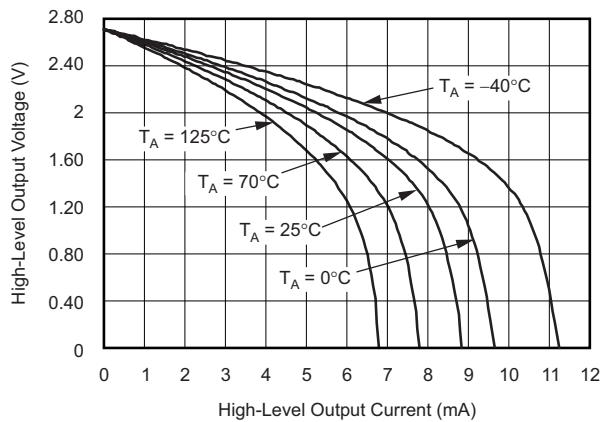


Figure 7. High-Level Output Voltage vs High-Level Output Current

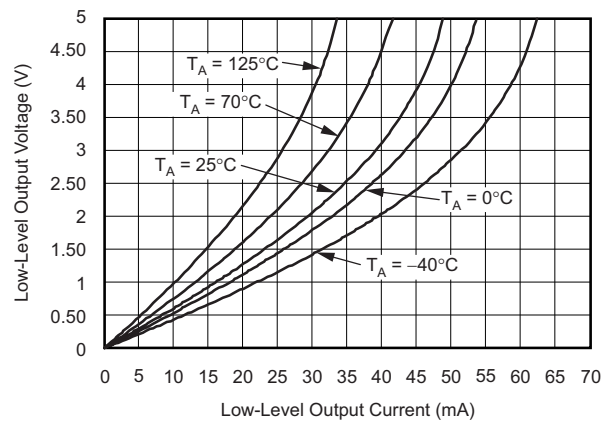


Figure 8. Low-Level Output Voltage vs Low-Level Output Current

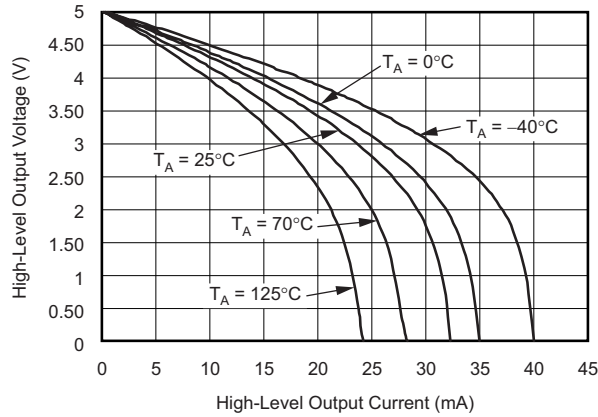


Figure 9. High-Level Output Voltage vs High-Level Output Current

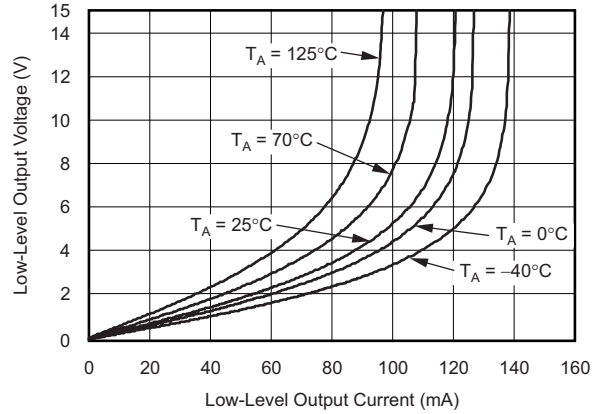


Figure 10. Low-Level Output Voltage vs Low-Level Output Current

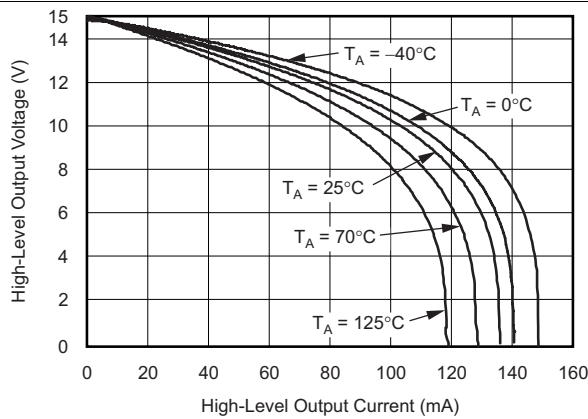


Figure 11. High-Level Output Voltage vs High-Level Output Current

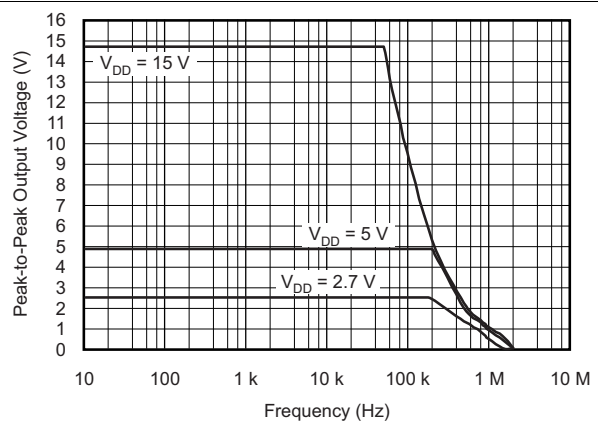


Figure 12. Peak-to-Peak Output Voltage vs Frequency

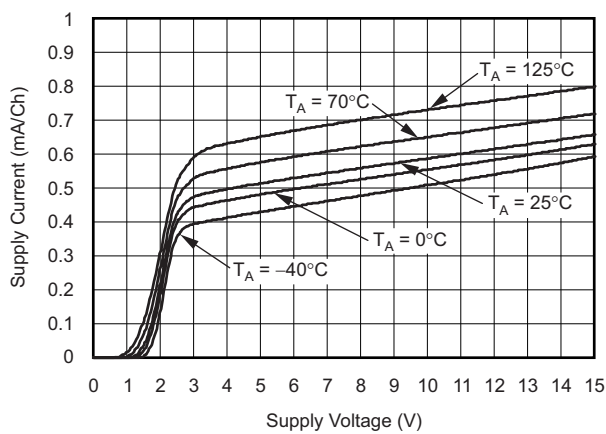


Figure 13. Supply Current vs Supply Voltage

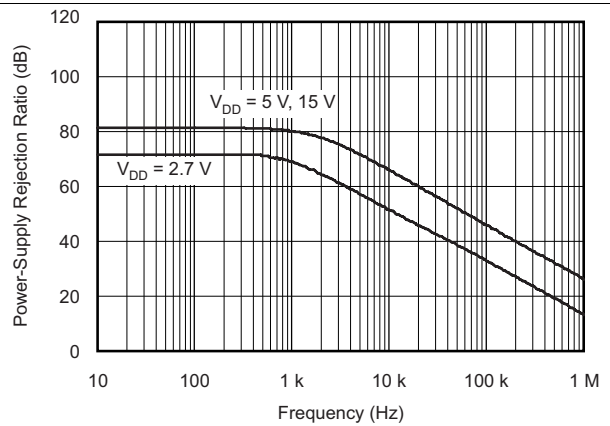


Figure 14. Power Supply Rejection Ratio vs Frequency

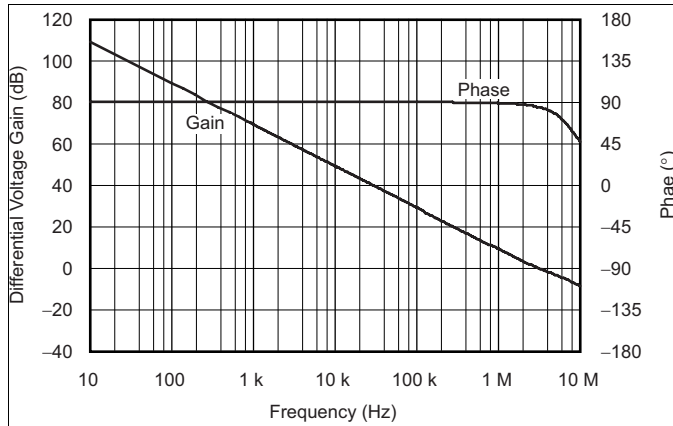


Figure 15. Differential Voltage Gain and Phase vs Frequency

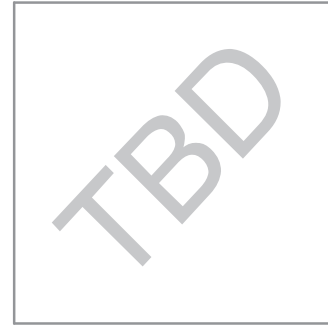


Figure 16. Gain Bandwidth Product vs Free-Air Temperature

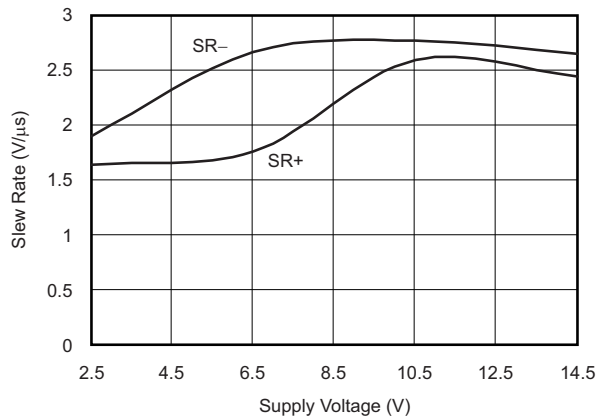


Figure 17. Slew Rate vs Supply Voltage

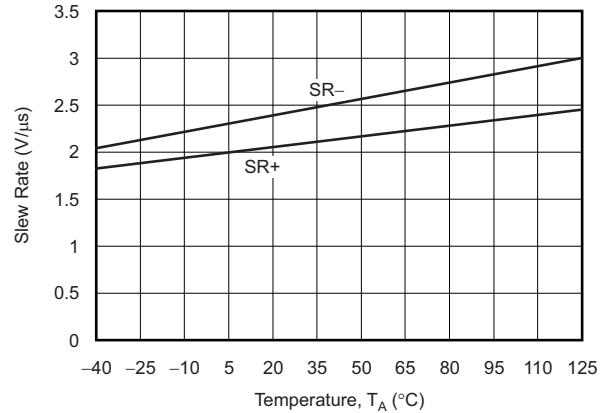


Figure 18. Slew Rate vs Free-Air Temperature

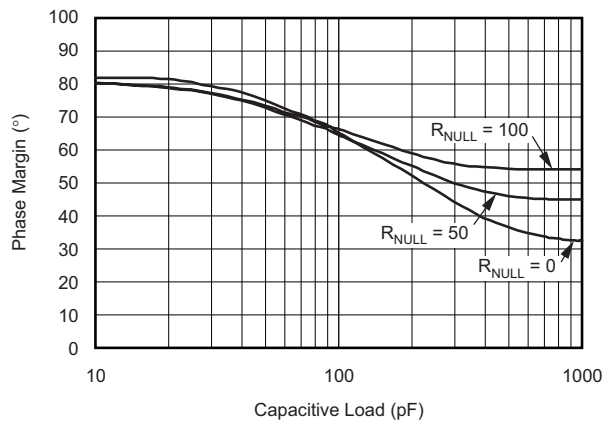


Figure 19. Phase Margin vs Capacitive Load

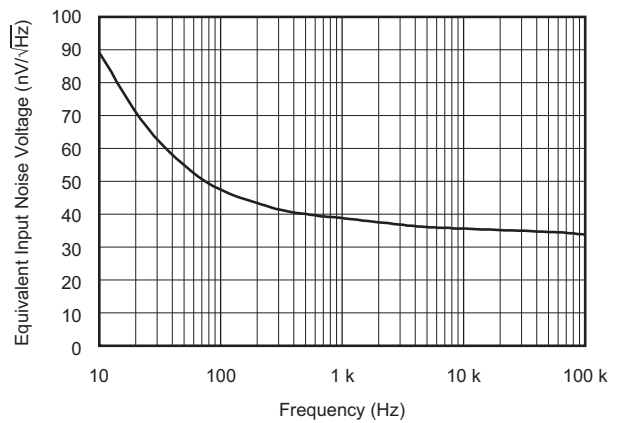
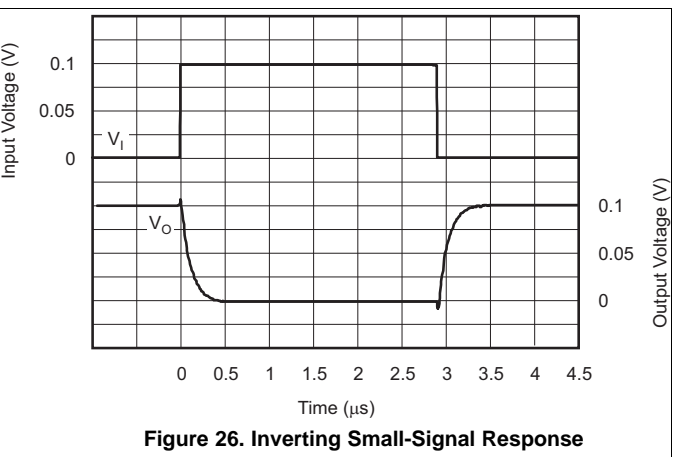
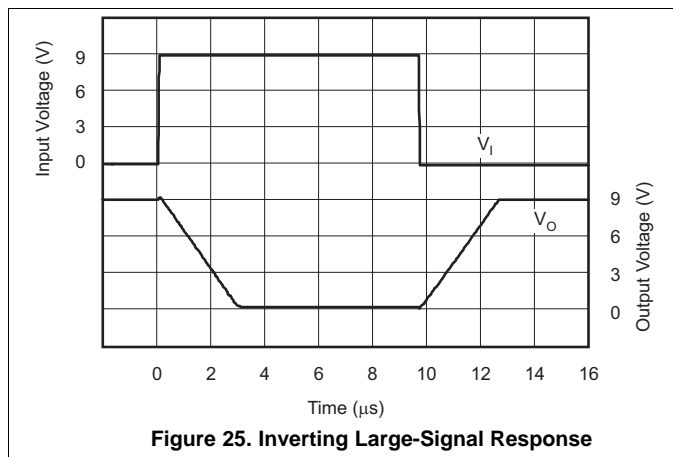
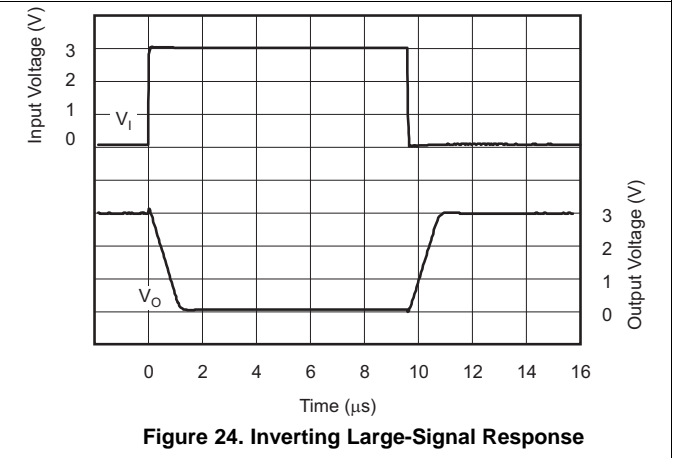
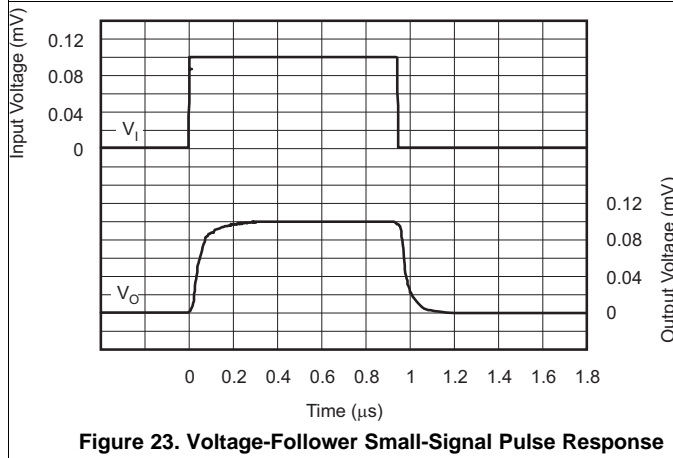
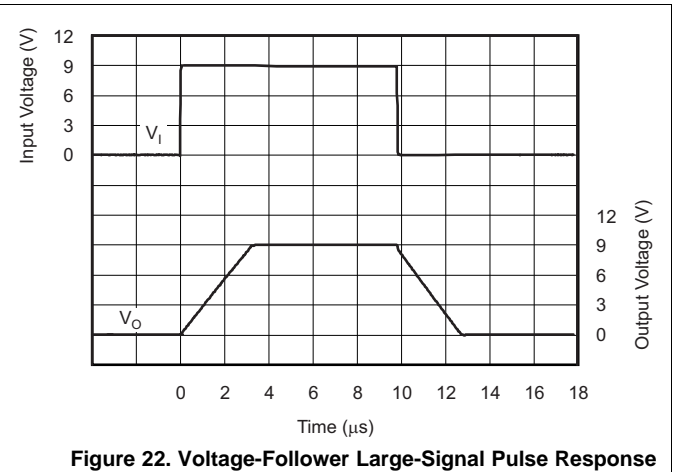
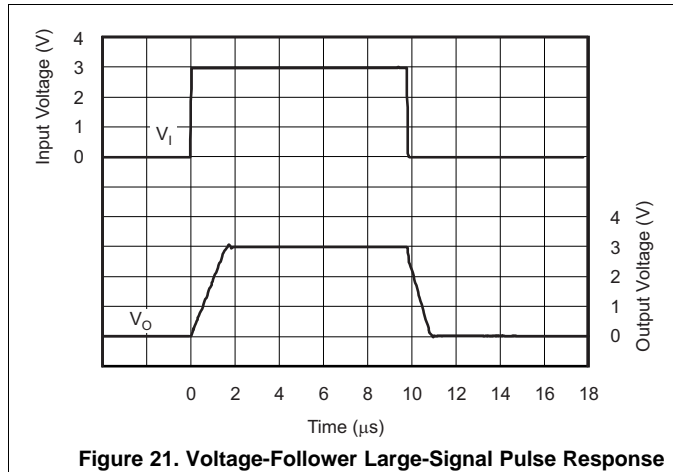


Figure 20. Equivalent Input Noise Voltage vs Frequency



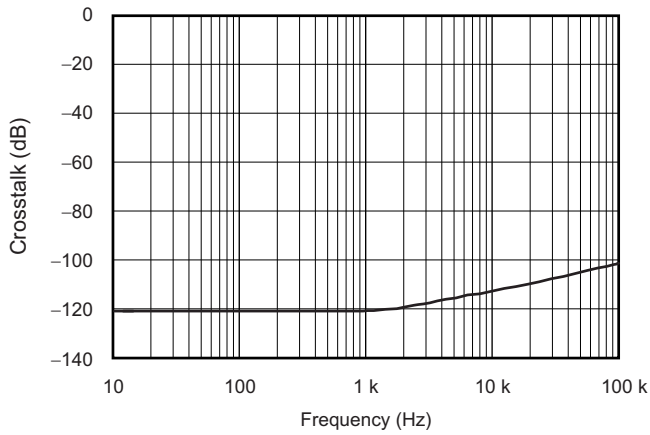


Figure 27. Crosstalk vs Frequency

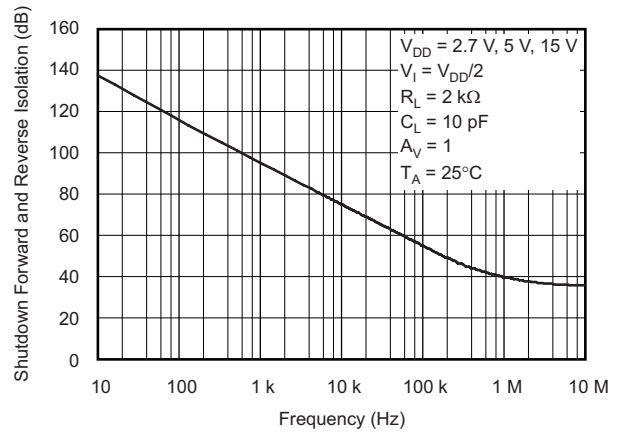


Figure 28. Shutdown Forward and Reverse Isolation vs Frequency

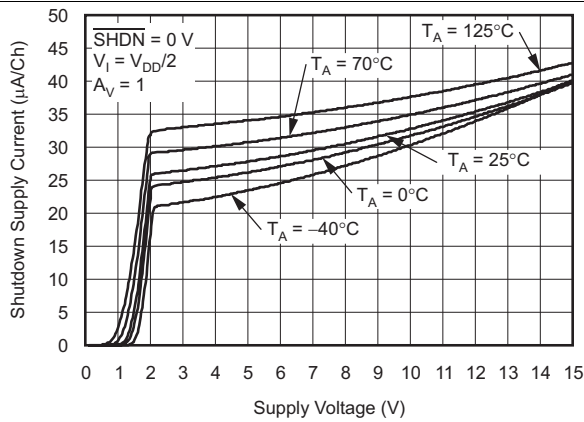


Figure 29. Shutdown Supply Current vs Supply Voltage

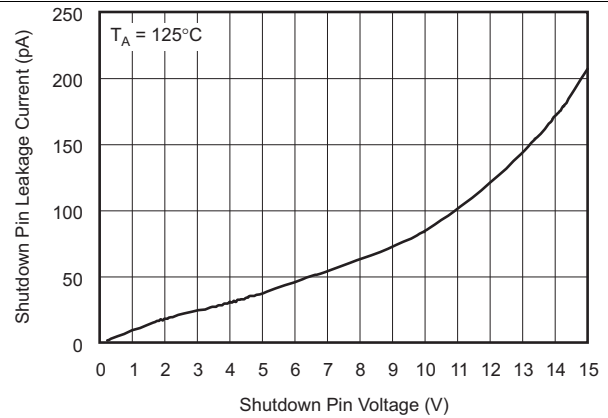
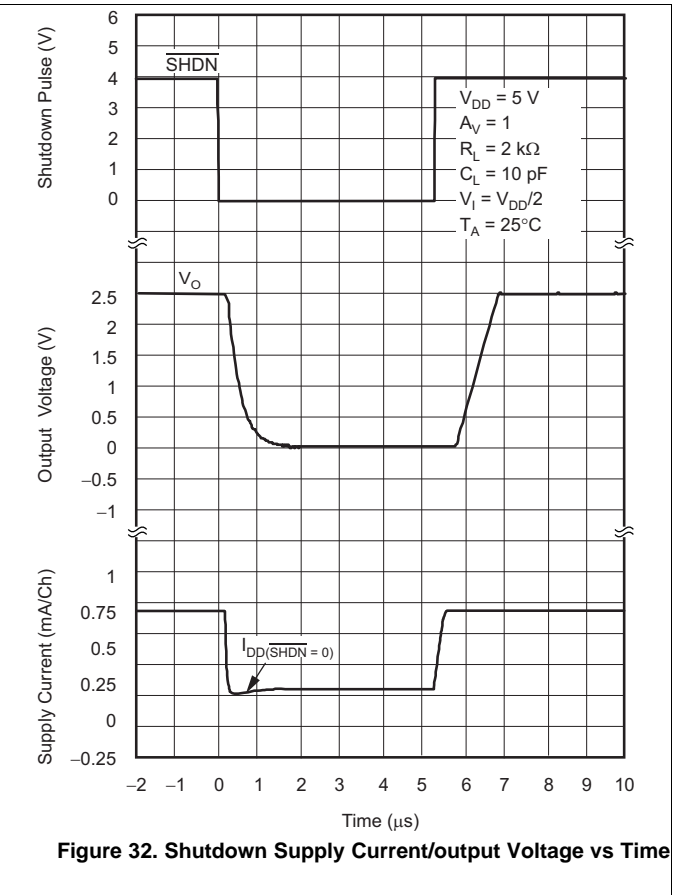
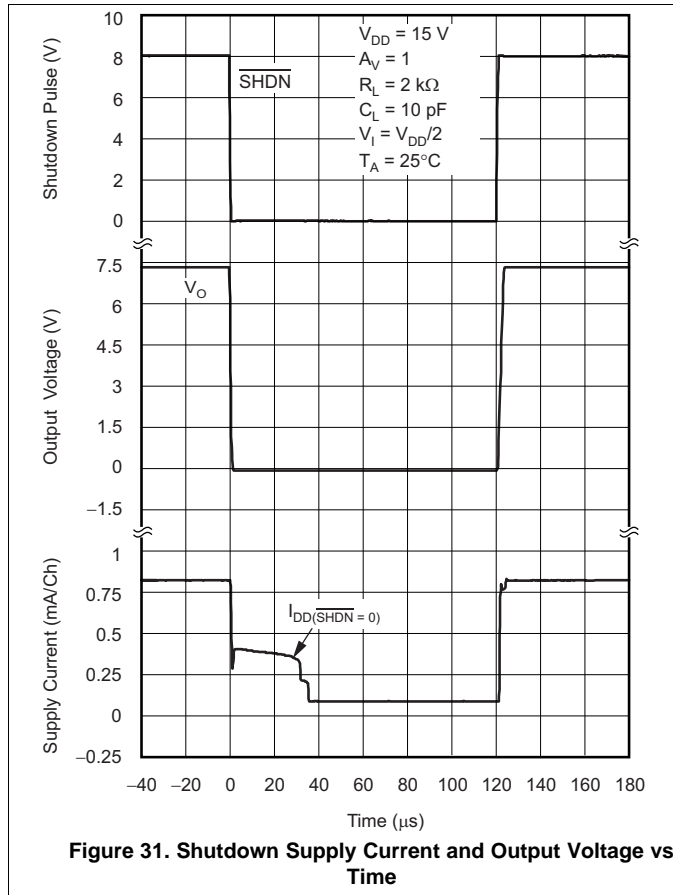


Figure 30. Shutdown Pin Leakage Current vs Shutdown Pin Voltage



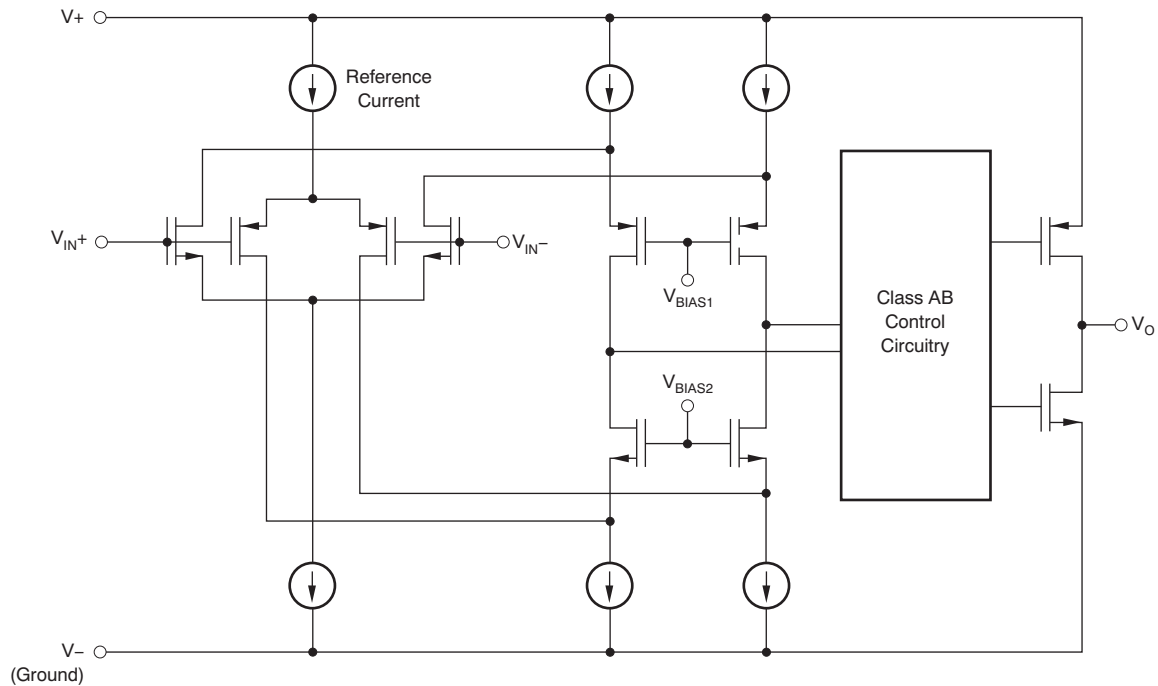


## 9 Detailed Description

### 9.1 Overview

The TLV237x single-supply CMOS operational amplifiers provide rail-to-rail input and output capability with 3-MHz bandwidth. Consuming 550  $\mu\text{A}$ , the TLV237x is designed for portable and battery-operated applications. The maximum recommended supply voltage is 16 V, which allows the devices to operate from ( $\pm 8\text{-V}$  supplies down to  $\pm 1.35\text{ V}$ ) a variety of rechargeable cells. The rail-to-rail inputs with high input impedance make the TLV237x an option for sensor signal-conditioning applications.

### 9.2 Functional Block Diagram



## 9.3 Feature Description

### 9.3.1 Rail-to-Rail Input Operation

The TLV237x input stage consists of two differential transistor pairs (NMOS and PMOS) that operate together to achieve rail-to-rail input operation. The transition point between these two pairs are shown in [Figure 1](#), [Figure 2](#), and [Figure 3](#) for a 2.7-V, 5-V, and 15-V supply. As the common-mode input voltage approaches the positive supply rail, the input pair switches from the PMOS differential pair to the NMOS differential pair. This transition occurs approximately 1.35 V from the positive rail and results in a change in offset voltage due to different device characteristics between the NMOS and PMOS pairs. If the input signal to the device is large enough to swing between both rails, this transition results in a reduction in common-mode rejection ratio (CMRR). If the input signal does not swing between both rails, bias the signal in the region where only one input pair is active. This is the region in [Figure 1](#) and [Figure 3](#) where the offset voltage varies slightly across the input range and optimal CMRR can be achieved. This has the greatest impact when operating from a 2.7-V supply voltage.

### 9.3.2 Driving a Capacitive Load

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device phase margin leading to high frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, TI recommends placing a resistor in series ( $R_{NULL}$ ) with the output of the amplifier, as shown in [Figure 33](#). A minimum value of 20  $\Omega$  works well for most applications.

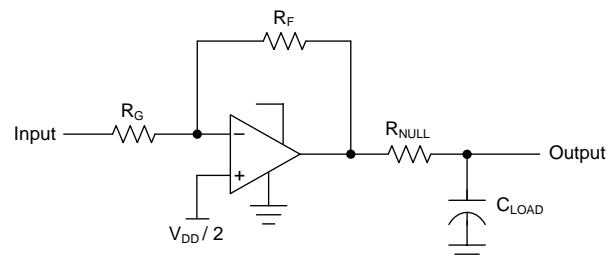
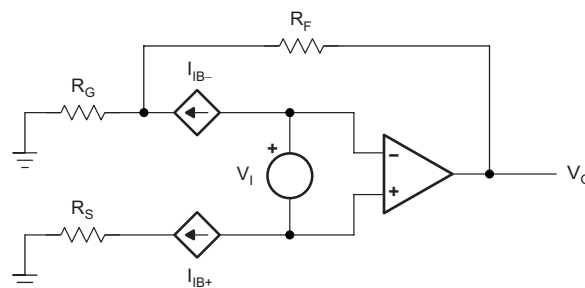


Figure 33. Driving a Capacitive Load

### 9.3.3 Offset Voltage

The output offset voltage ( $V_{OO}$ ) is the sum of the input offset voltage ( $V_{IO}$ ) and input bias currents ( $I_{IB}$ ) times the corresponding gains. [Figure 34](#) can be used to calculate the output offset voltage. Note that this does not include other parameters that can affect the offset voltage, such as PSRR and CMRR.



$$V_{OO} = V_{IO} \left[ 1 + \left( \frac{R_F}{R_G} \right) \right] \pm I_{IB+} R_S \left[ 1 + \left( \frac{R_F}{R_G} \right) \right] \pm I_{IB-} R_F$$

Figure 34. Output Offset Voltage Model

## Feature Description (continued)

### 9.3.4 General Configurations

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to accomplish this is to place an RC filter at the noninverting terminal. **To accomplish this, place an RC filter at the noninverting terminal** (see Figure 35).

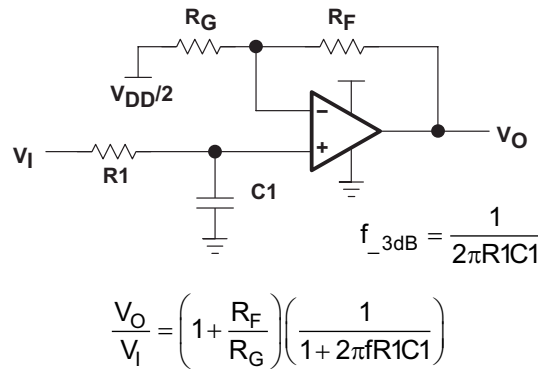


Figure 35. Single-Pole Low-Pass Filter

If even more attenuation is required, a multiple pole filter is required. The Sallen-key filter **is** used for this task. For best results, the amplifier must have a bandwidth that is eight to 10 times the filter frequency bandwidth. Failure to do this **results** in phase shift of the amplifier.

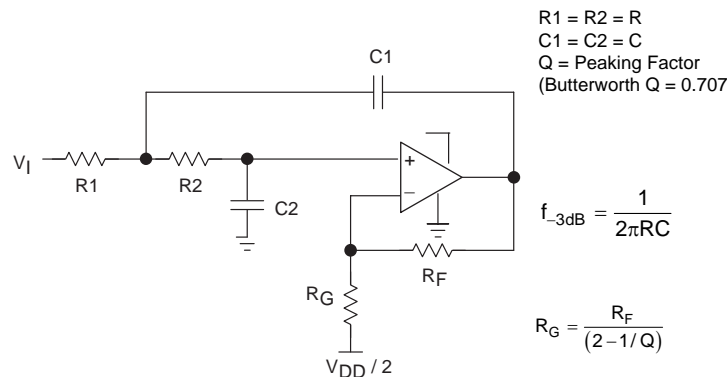


Figure 36. 2-Pole, Low-Pass, Sallen-Key Filter

### 9.3.5 Shutdown Function

Three members of the TLV237x family (TLV2370, TLV2373, and TLV2375) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to 25  $\mu$ A/channel, the amplifier is disabled, and the outputs are placed in a high impedance mode. To enable the amplifier, the shutdown terminal can either be left floating or pulled high. When the shutdown terminal is left floating, take care to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

## 9.4 Device Functional Modes

The TLV2371, TLV2372, and TLV2374 have a single functional mode. These devices are operable as long as the power-supply voltage is between 2.7 V ( $\pm 1.35$  V) and 16 V ( $\pm 8$  V).

The TLV2370, TLV2373, and TLV2375 are likewise operational as long as the power-supply voltage is between 2.7 V ( $\pm 1.35$  V) and 16 V ( $\pm 8$  V), additionally these devices also have a shutdown capability. When the shutdown control pin is driven below 0.8 V above ground, the device is in shutdown. If the shutdown control pin voltage is driven to greater than 2 V above ground, the device is in its normal operating mode. See [Shutdown Function](#) for additional information regarding shutdown operation.

## 10 Application and Implementation

### NOTE

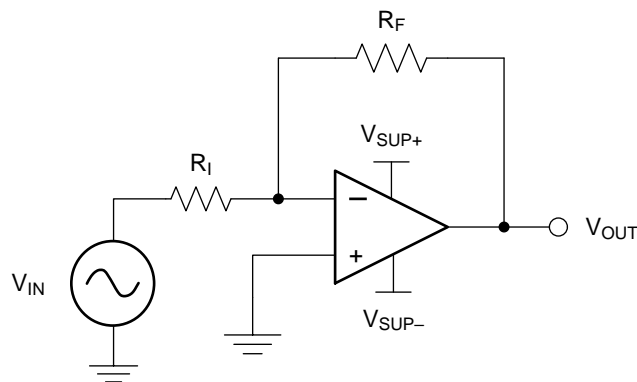
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

When designing for low power, choose system components carefully. To minimize current consumption, select large-value resistors. Any resistors react with stray capacitance in the circuit and the input capacitance of the operational amplifier. These parasitic RC combinations affect the stability of the overall system. Use of a feedback capacitor assures stability and limits overshoot or gain peaking.

### 10.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as [Figure 37](#) shows. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, ~~making~~ **which results in** a negative voltage of the same magnitude. In the same manner, the amplifier makes negative input voltages positive on the output. ~~In addition, amplification can be added by selecting~~ **Select** the input resistor ( $R_I$ ) and the feedback resistor ( $R_F$ ) **to add amplification.**



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**Figure 37. Application Schematic**

## Typical Application (continued)

### 10.2.1 Design Requirements

The selected supply voltage must be larger than the input voltage range and the desired output range. Consider the limits of the input common-mode range ( $V_{CM}$ ) and the output voltage swing to the rails ( $V_O$ ). For example, this application scales a signal of  $\pm 0.5$  V (1 V) to  $\pm 1.8$  V (3.6 V). Setting the supply at  $\pm 2.5$  V is sufficient to accommodate this application.

### 10.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

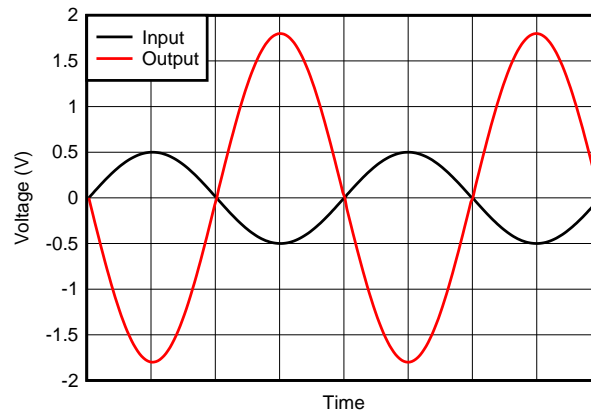
$$A_V = \frac{V_{OUT}}{V_{IN}} \tag{1}$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \tag{2}$$

When the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the  $k\Omega$  range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of  $k\Omega$ ) draw the smallest current but generate the highest noise. Very small resistors (100s of  $\Omega$ ) generate low noise but draw high current. This example uses 10  $k\Omega$  for  $R_I$ , meaning 36  $k\Omega$  is used for  $R_F$ . These values are determined by [Equation 3](#):

$$A_V = -\frac{R_F}{R_I} \tag{3}$$

### 10.2.3 Application Curve



**Figure 38. Inverting Amplifier Input and Output**

## 11 Power Supply Recommendations

The TLV237x family is specified for operation from 2.7 V to 16 V ( $\pm 1.35$  V to  $\pm 8$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ . The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

### CAUTION

Supply voltages larger than 16 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1- $\mu\text{F}$  bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see *Layout*.

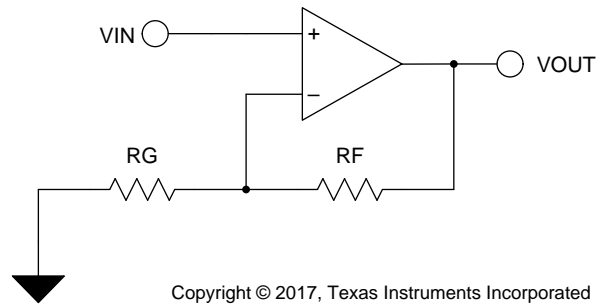
## 12 Layout

### 12.1 Layout Guidelines

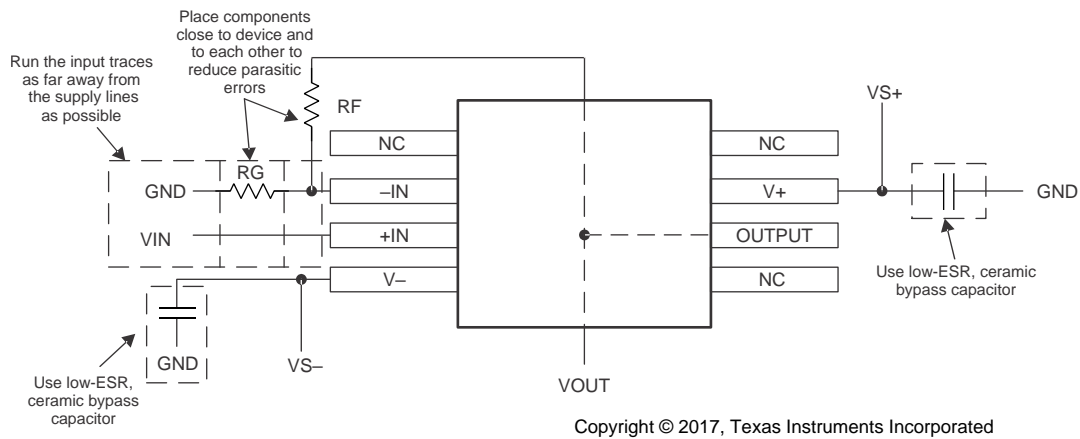
To achieve the levels of high performance of the TLV237x, follow proper printed-circuit board design techniques. A general set of guidelines is shown in the following list:

- Ground planes: TI highly recommends using a ground plane on the board to provide all components with a low inductive ground connection. However, in the areas of the amplifier inputs and output, the ground plane can be removed to minimize the stray capacitance.
- Proper power supply decoupling: Use a 6.8- $\mu\text{F}$  tantalum capacitor in parallel with a 0.1- $\mu\text{F}$  ceramic capacitor on each supply ~~terminal~~ pin. It may be possible to share the tantalum among several amplifiers depending on the application ~~terminal~~, ~~but a 0.1- $\mu\text{F}$  ceramic capacitor must always be used on the supply terminal of every amplifier.~~ Always use a 0.1- $\mu\text{F}$  ceramic capacitor on the supply pin of every amplifier. In addition, the 0.1- $\mu\text{F}$  capacitor must be placed as close ~~to the supply terminal~~ to the supply pin as possible. ~~as possible to the supply terminal~~. As this distance increases, the inductance in the connecting trace makes the capacitor less effective. The designer must strive for distances of less than 0.1 inches between the device power ~~terminals~~ pins and the ceramic capacitors.
- Sockets: Sockets can be used but are not recommended. The additional lead inductance in the socket pins often lead to stability problems. ~~Surface-mount packages soldered directly to the printed-circuit board is the best implementation.~~ For best results, solder the surface mount packages directly to the printed circuit board.
- Short trace runs and compact part placements: Optimum high performance is achieved when stray series inductance are minimized. To realize this, the circuit layout must be made as compact as possible, which minimizes the length of all trace runs. Pay particular attention to the inverting input of the amplifier. The length of the inverting input must be kept as short as possible. This helps to minimize stray capacitance at the input of the amplifier.
- Surface-mount passive components: Using surface-mount passive components is recommended for high performance amplifier circuits for several reasons. First, because of the low lead inductance of surface-mount components, the problem with stray series inductance is reduced. Second, the small size of surface-mount components naturally leads to a more compact layout, which minimizes stray inductance and capacitance. TI recommends that lead lengths are kept as short as possible if leaded components are used.

## 12.2 Layout Example



**Figure 39. Schematic Representation**



**Figure 40. Operational Amplifier Board Layout for Noninverting Configuration**

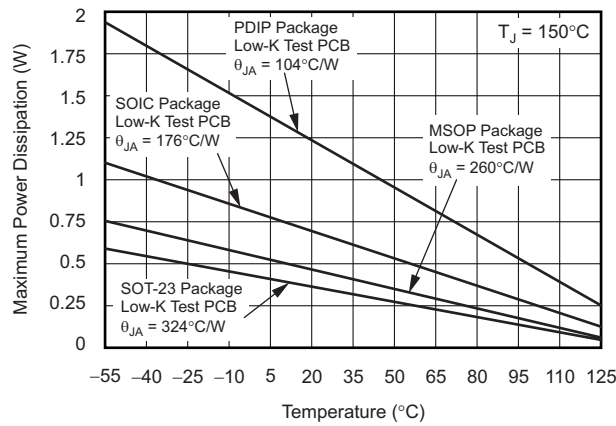
### 12.3 Power Dissipation Considerations

For a given  $\theta_{JA}$  value, the maximum power dissipation is shown in Figure 41 and is calculated by Equation 4:

$$P_D = \left[ \frac{T_{MAX} - T_A}{\theta_{JA}} \right]$$

where

- $P_D$  = Maximum power dissipation of TLV237x IC (watts)
- $T_{MAX}$  = Absolute maximum junction temperature (150°C)
- $T_A$  = Free-ambient air temperature (°C)
- $\theta_{JA} = \theta_{JC}$  (Thermal coefficient from junction to case) +  $\theta_{CA}$  (Thermal coefficient from case to ambient air (°C/W)) (4)



Results are with no air flow and using JEDEC Standard Low-K test PCB.

**Figure 41. Maximum Power Dissipation vs Free-Air Temperature**



## 13 器件和文档支持

### 13.1 文档支持

#### 13.1.1 相关文档

如需相关文档，请参阅：

[《EVM 选择指南》](#) (SLOU060)

### 13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 4. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
TLV2370	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV2371	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV2372	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV2373	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV2374	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>
TLV2375	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>	<a href="#">单击此处</a>

### 13.3 接收文档更新通知

要接收文档更新通知，请导航至 [Ti.com](http://Ti.com) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 13.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 13.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 13.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2370ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2370I	
TLV2370IDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBFI	<a href="#">Samples</a>
TLV2370IDBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBFI	<a href="#">Samples</a>
TLV2370IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2370I	<a href="#">Samples</a>
TLV2370IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	2370I	<a href="#">Samples</a>
TLV2371ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371I	<a href="#">Samples</a>
TLV2371IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBGI	<a href="#">Samples</a>
TLV2371IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VBGI	<a href="#">Samples</a>
TLV2371IDG4	ACTIVE	SOIC	D	8	75	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2371IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2371I	<a href="#">Samples</a>
TLV2371IDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2371IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	2371I	<a href="#">Samples</a>
TLV2371IPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2372ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372I	<a href="#">Samples</a>
TLV2372IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	APG	<a href="#">Samples</a>
TLV2372IDGKG4	ACTIVE	VSSOP	DGK	8	80	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2372IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	APG	<a href="#">Samples</a>
TLV2372IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI   NIPDAU	Level-1-260C-UNLIM	-40 to 125	2372I	<a href="#">Samples</a>
TLV2372IDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2372IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	2372I	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV2372IPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2373IDGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	API	<a href="#">Samples</a>
TLV2373IDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	API	<a href="#">Samples</a>
TLV2373IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2373IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2373I	<a href="#">Samples</a>
TLV2373IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	TLV2373I	<a href="#">Samples</a>
TLV2374ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	<a href="#">Samples</a>
TLV2374IDG4	ACTIVE	SOIC	D	14	50	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2374IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	<a href="#">Samples</a>
TLV2374IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	2374I	<a href="#">Samples</a>
TLV2374IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	<a href="#">Samples</a>
TLV2374IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2374I	<a href="#">Samples</a>
TLV2374IPWRG4	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
TLV2375ID	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	<a href="#">Samples</a>
TLV2375IDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	<a href="#">Samples</a>
TLV2375IN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	2375I	<a href="#">Samples</a>
TLV2375IPW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	<a href="#">Samples</a>
TLV2375IPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2375I	<a href="#">Samples</a>
TLV2375IPWRG4	ACTIVE	TSSOP	PW	16	2000	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV2371, TLV2372, TLV2374 :**

● Automotive : [TLV2371-Q1](#), [TLV2372-Q1](#), [TLV2374-Q1](#)

● Enhanced Product : [TLV2371-EP](#), [TLV2374-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2370IDBVR	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2370IDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2370IDBVT	SOT-23	DBV	6	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TLV2370IDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV2370IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2371IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV2371IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TLV2371IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2372IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2372IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2372IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2373IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2373IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV2373IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2374IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2374IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2375IDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TLV2375IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

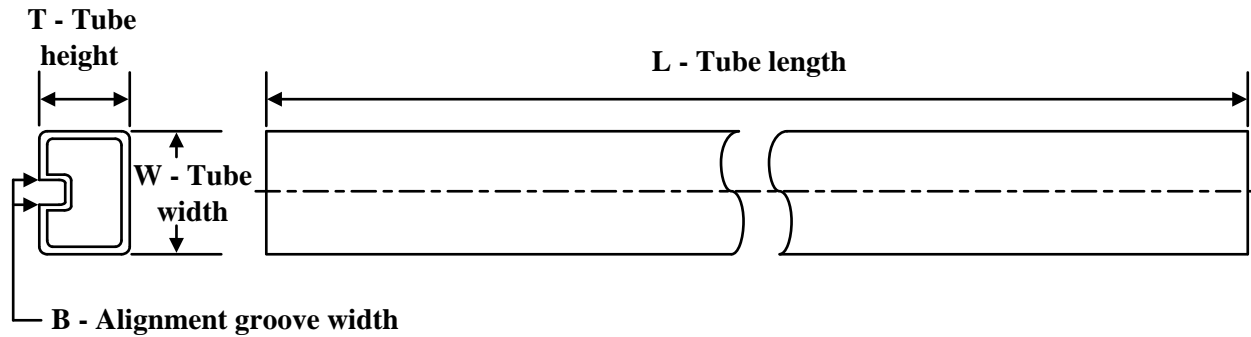
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2370IDBVR	SOT-23	DBV	6	3000	182.0	182.0	20.0
TLV2370IDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV2370IDBVT	SOT-23	DBV	6	250	182.0	182.0	20.0
TLV2370IDBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TLV2370IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2371IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV2371IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TLV2371IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2372IDGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TLV2372IDGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
TLV2372IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV2373IDGSR	VSSOP	DGS	10	2500	364.0	364.0	27.0
TLV2373IDGSR	VSSOP	DGS	10	2500	358.0	335.0	35.0
TLV2373IDR	SOIC	D	14	2500	340.5	336.1	32.0
TLV2374IDR	SOIC	D	14	2500	340.5	336.1	32.0
TLV2374IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TLV2375IDR	SOIC	D	16	2500	340.5	336.1	32.0
TLV2375IPWR	TSSOP	PW	16	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLV2370ID	D	SOIC	8	75	507	8	3940	4.32
TLV2370IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2371ID	D	SOIC	8	75	507	8	3940	4.32
TLV2371IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2372ID	D	SOIC	8	75	507	8	3940	4.32
TLV2372IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
TLV2372IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2373IDGS	DGS	VSSOP	10	80	330	6.55	500	2.88
TLV2373IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2374ID	D	SOIC	14	50	507	8	3940	4.32
TLV2374IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2374IPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2374IPWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
TLV2375ID	D	SOIC	16	40	507	8	3940	4.32
TLV2375IN	N	PDIP	16	25	506	13.97	11230	4.32
TLV2375IPW	PW	TSSOP	16	90	530	10.2	3600	3.5

# DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/J 02/2024

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

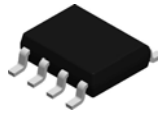
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

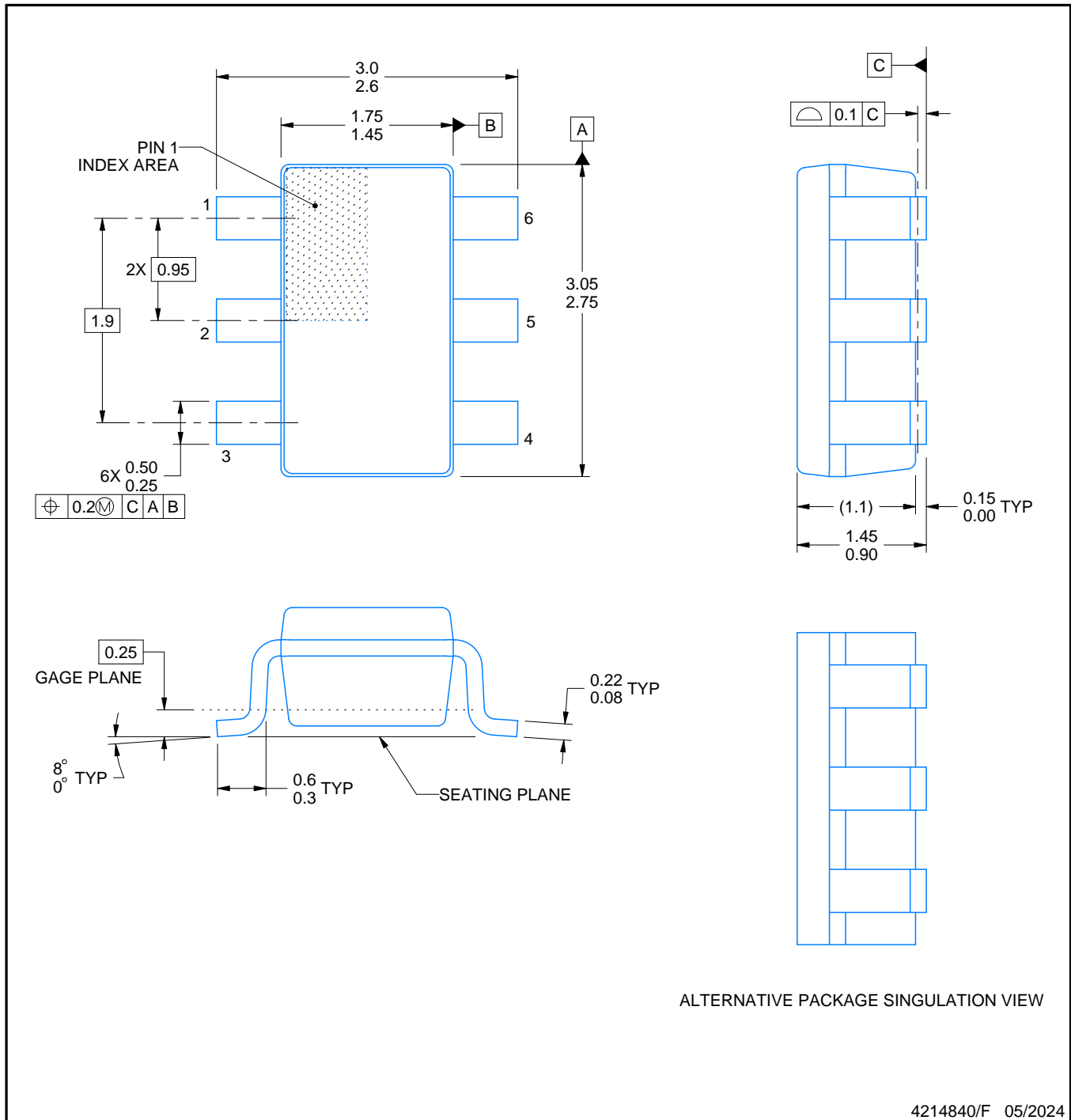
# DBV0006A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

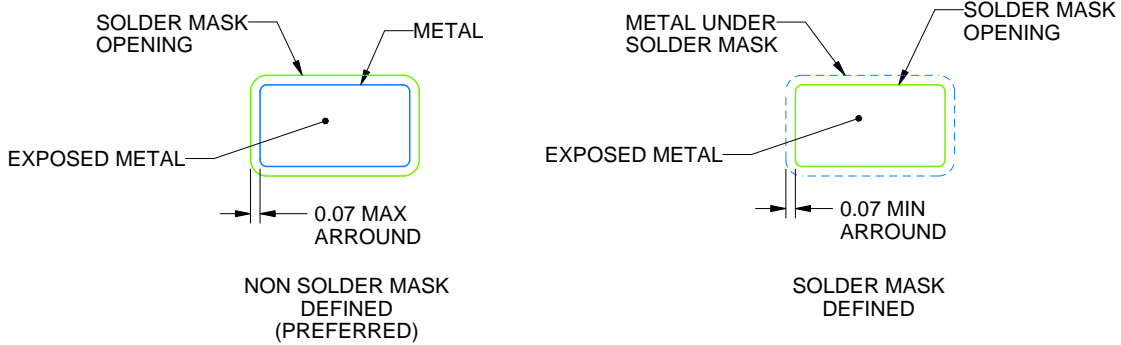
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/F 05/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/F 05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGS0010A



# PACKAGE OUTLINE

## VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4221984/A 05/2015

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

# EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:10X



SOLDER MASK DETAILS  
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



# EXAMPLE BOARD LAYOUT

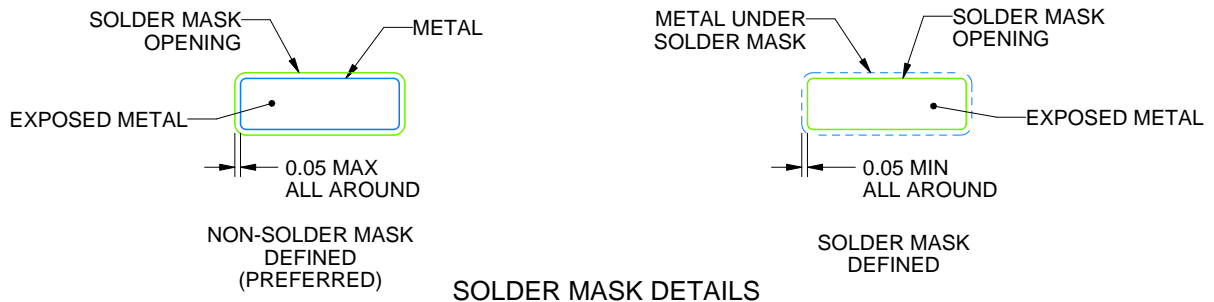
DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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