

# SN74LV21A 双路 4 输入正与门

## 1 特性

- 2V 至 5.5V  $V_{CC}$  运行
- 电压为 5V 时,  $t_{pd}$  最大值为 6ns
- $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时,  $V_{OLP}$  (输出接地反弹) 典型值小于 0.8V
- $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$  时,  $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值大于 2.3V
- $I_{off}$  支持局部关断模式运行
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范

## 2 说明

这些双路 4 输入正与门可在 2V 至 5.5V  $V_{CC}$  电压下运行。

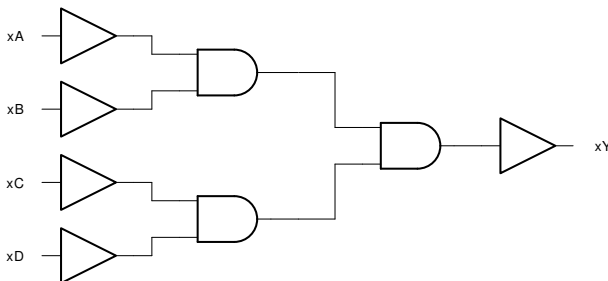
SN74LV21A 器件以正逻辑执行布尔函数  $Y = A \cdot B \cdot C \cdot D$ 。

这些器件专用于使用  $I_{off}$  的局部断电应用。 $I_{off}$  电路会禁用输出, 从而在器件断电时防止电流回流损坏器件。

### 封装信息

器件型号	封装 <sup>1</sup>	封装尺寸 <sup>2</sup>
SN74LV21A	DGV (TVSOP, 14)	3.60 mm x 6.4 mm
	D (SOIC, 14)	8.65 mm x 6 mm
	NS (SO, 14)	10.20 mm x 7.8 mm
	DB (SSOP, 14)	6.20 mm x 7.8 mm
	PW (TSSOP, 14)	5.00 mm x 6.4 mm

- (1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。
- (2) 封装尺寸 (长 x 宽) 为标称值, 并包括引脚 (如适用)。



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### 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

#### Changes from Revision E (April 2005) to Revision F (July 2023)

Page

- |  |          |
|--|----------|
| • 更新了整个文档中的编号、格式、表格、图和交叉参考，以反映当前数据表标准..... | <b>1</b> |
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## 4 Pin Configuration and Functions

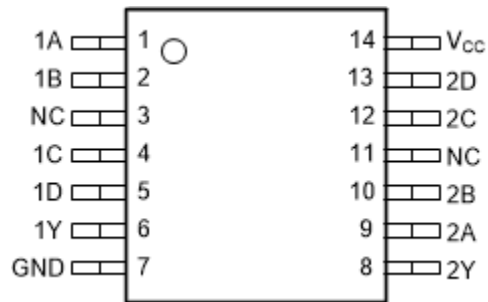


图 4-1. SN74LV21A D, DB, DGV, NS, or PW Package (Top View)

表 4-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
1A	1	I	1A Input
1B	2	I	1B Input
NC	3	—	Not internally connected
1C	4	I	1C Input
1D	5	I	1D Input
1Y	6	O	1Y Output
2Y	8	O	2Y Output
2A	9	I	2A Input
2B	10	I	2B Input
NC	11	—	Not internally connected
2C	12	I	2C Input
2D	13	I	2D Input
GND	7	—	Ground Pin
V <sub>CC</sub>	14	—	Power Pin

(1) Signal Types: I = Input, O = Output.

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage range		- 0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>		- 0.5	7	V
$V_O$	Output voltage range applied in high or low state <sup>(2) (3)</sup>		- 0.5	$V_{CC} + 0.5$	V
$V_O$	Output voltage range applied in power-off state <sup>(2)</sup>		- 0.5	7	V
$I_{IK}$	Input clamp current	$(V_I < 0)$		- 20	mA
$I_{OK}$	Output clamp current	$(V_O < 0)$		- 50	mA
$I_O$	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND			$\pm 50$	mA
$T_{stg}$	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	$\pm 2000$	V
		Charged device model (CDM), per JESD22-C101 <sup>(2)</sup>	$\pm 1000$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage		2	5.5	V
$V_{IH}$	High level input voltage	$V_{CC} = 2 \text{ V}$	1.5		V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$	$V_{CC} \times 0.7$		
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	$V_{CC} \times 0.7$		
$V_{IL}$	Low level input voltage	$V_{CC} = 2 \text{ V}$		0.5	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		$V_{CC} \times 0.3$	
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		$V_{CC} \times 0.3$	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		$V_{CC} \times 0.3$	
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High level output current	$V_{CC} = 2 \text{ V}$		- 50	$\mu\text{A}$
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		- 2	mA
		$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$		- 6	
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$		- 12	

### 5.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
I <sub>OL</sub>	Low level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	mA
		V <sub>CC</sub> = 3 V to 3.6 V	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise and fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	
T <sub>A</sub>	Operating free-air temperature	- 40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#)

### 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LV21A					UNIT
	D	DB	DGV	NS	PW	
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance					°C/W
	86	96	127	76	113	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

### 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = - 50 μA	2 V to 5.5 V	V <sub>CC</sub> - 0.1		V
			2.3 V	2		
			3 V	2.48		
			4.5 V	3.8		
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 50 μA	2 V to 5.5 V		0.1	V
			2.3 V		0.4	
			3 V		0.44	
			4.5 V		0.55	
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V		±1	μA
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V		20	μA
I <sub>off</sub>	Off-state leakage current	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V		5	μA
C <sub>i</sub>	Input capacitance	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.9		pF

### 5.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A, B, C or D	Y	C <sub>L</sub> = 15 pF		7	12	1	14	ns
t <sub>pd</sub>	A, B, C or D	Y	C <sub>L</sub> = 50 pF		9.2	15.7	1	19	

### 5.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#) )

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, C, or D	Y	$C_L = 15\text{ pF}$		5.1	7	1	8.5	ns
$t_{pd}$	A, B, C, or D	Y	$C_L = 50\text{ pF}$		6.6	10.5	1	12	

### 5.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#) )

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74LV21A		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, C, or D	Y	$C_L = 15\text{ pF}$		3.8	5	1	6	ns
$t_{pd}$	A, B, C, or D	Y	$C_L = 50\text{ pF}$		4.9	7	1	8	

### 5.9 Noise Characteristics

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER <sup>(1)</sup>		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		0	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

### 5.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ ,	$f = 10\text{ MHz}$	3.3 V	17.4	pF
				5 V	20.2	

## 6 Parameter Measurement Information

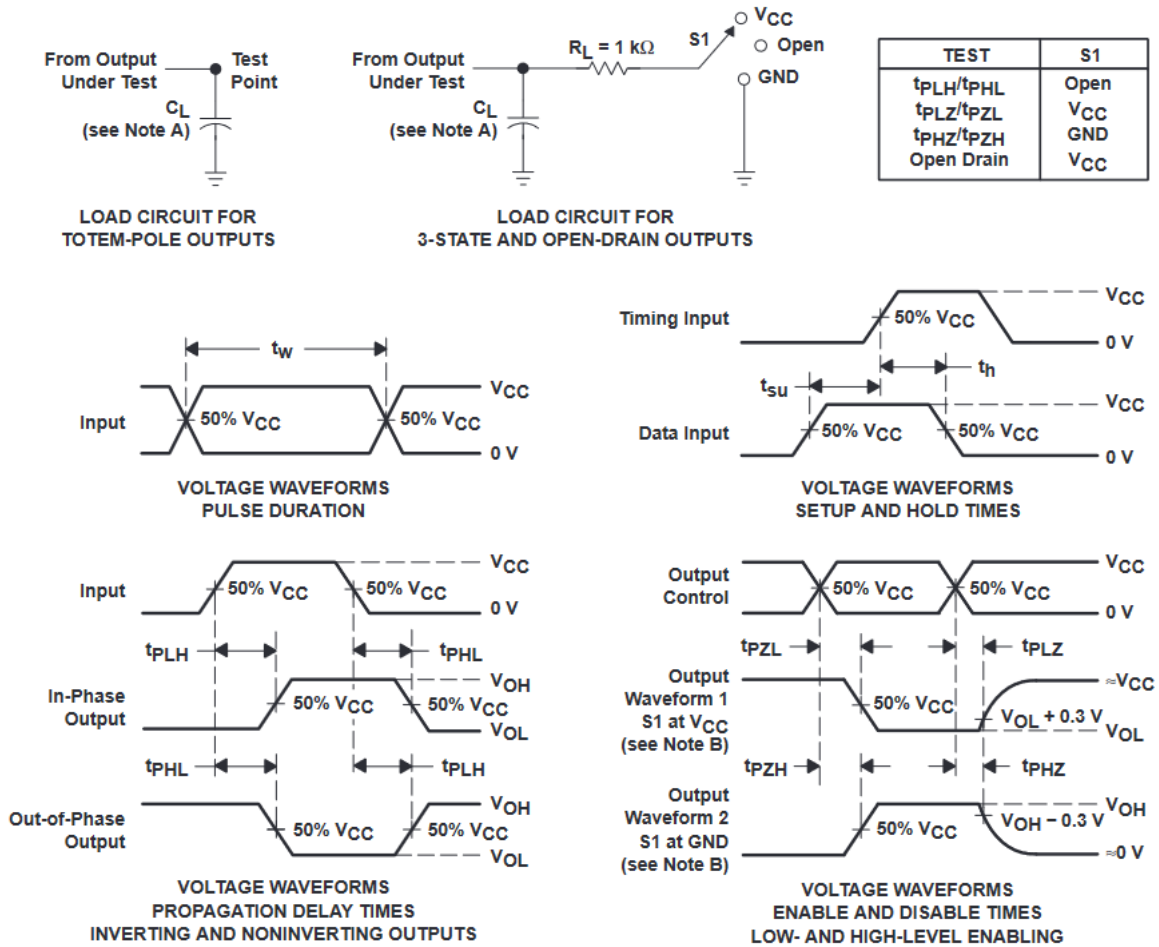


图 6-1. Load Circuit and Voltage Waveforms

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

## 7 Detailed Description

### 7.1 Overview

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The SN74LV21A devices perform the Boolean function  $Y = A \cdot B \cdot C \cdot D$  in positive logic. These dual 4-input positive-AND gates are designed for 2-V to 5.5-V  $V_{CC}$  operation.

### 7.2 Functional Block Diagram

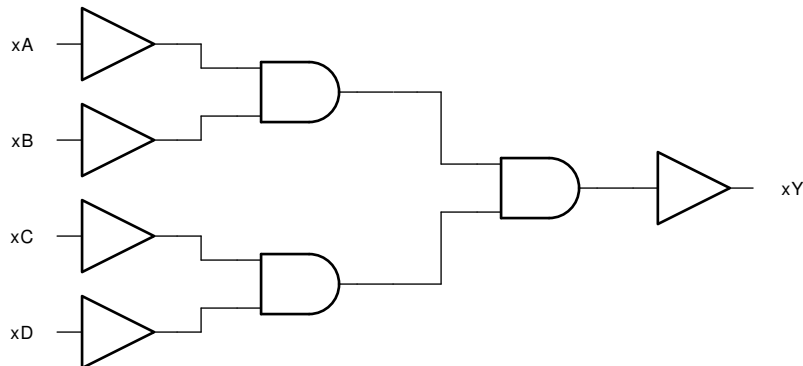


图 7-1. logic diagram (positive logic)

### 7.3 Device Functional Modes

Function Table  
(each gate)

INPUTS <sup>(1)</sup>				OUTPUT <sup>(2)</sup>
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

(1) H = High Voltage Level, L = Low Voltage Level, X = Do not Care, Z = High Impedance

(2) H = Driving High, L = Driving Low, Z = High Impedance State



## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Documentation

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV21A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 8.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

#### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

#### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV21AD	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	LV21A	
SN74LV21ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV21A	Samples
SN74LV21APW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	LV21A	
SN74LV21APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples
SN74LV21APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV21A	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

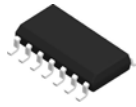
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV21ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV21ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV21ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV21ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV21ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV21APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV21APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV21ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV21ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV21ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV21ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV21ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV21APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV21APWR	TSSOP	PW	14	2000	356.0	356.0	35.0

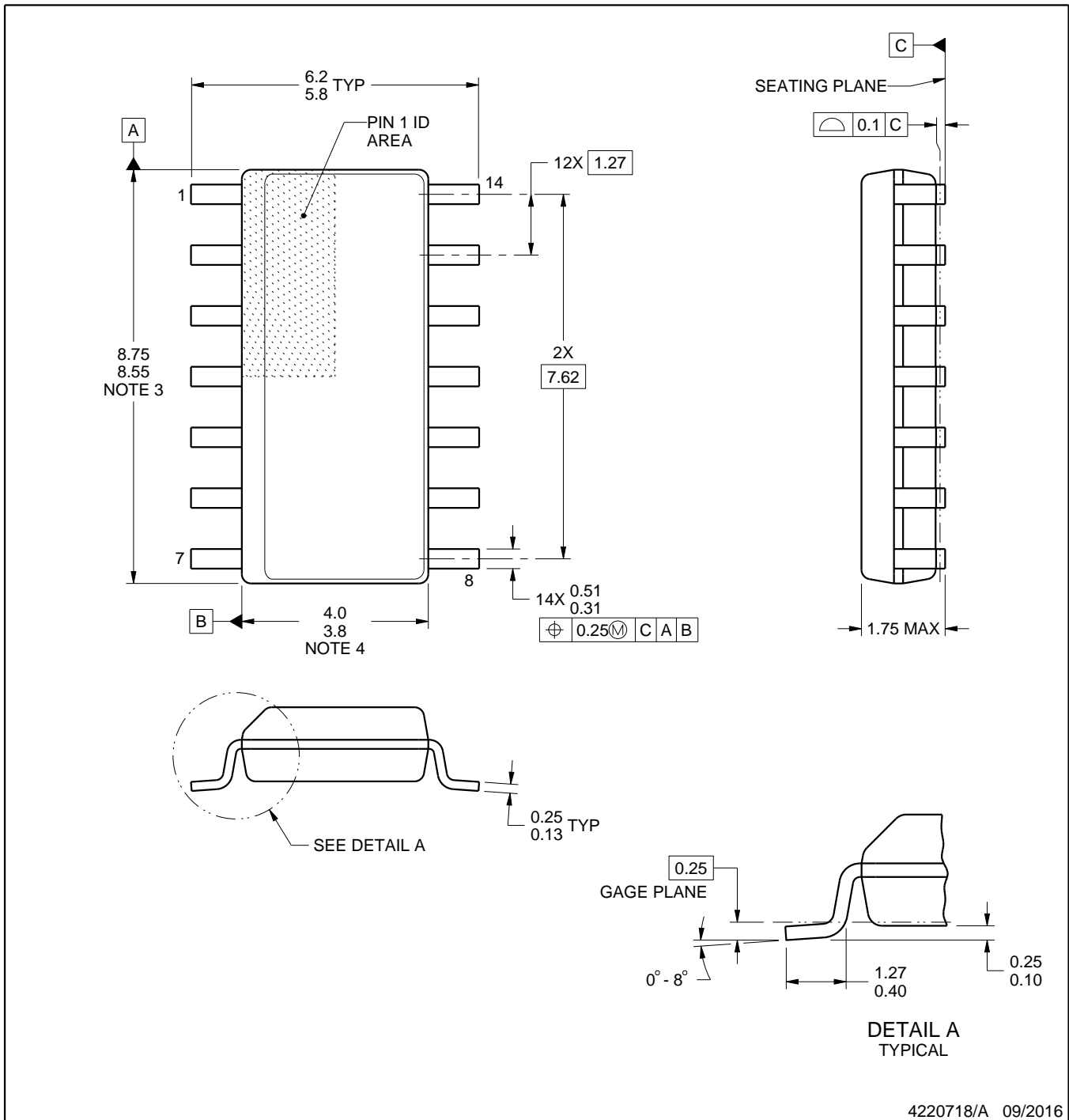
D0014A



# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

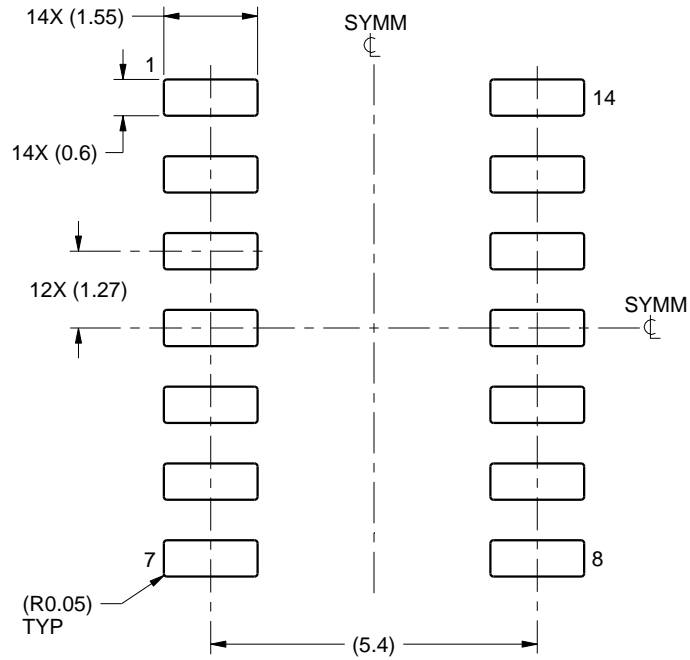
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

# EXAMPLE BOARD LAYOUT

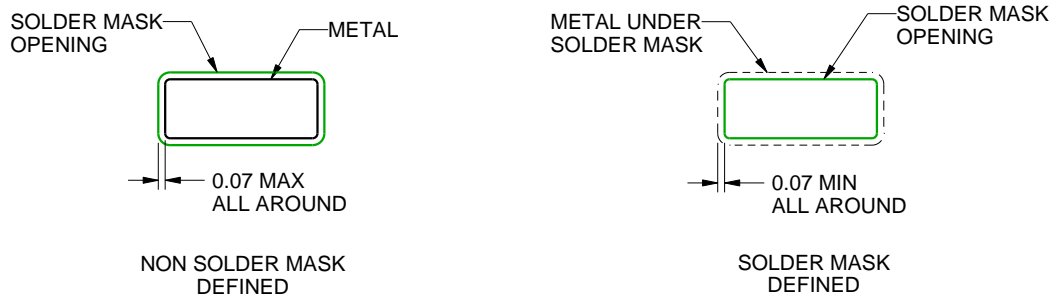
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

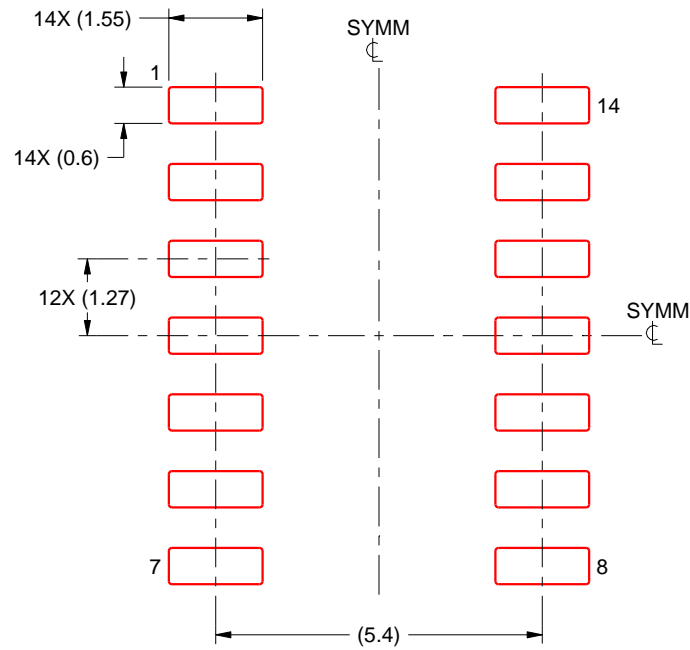
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

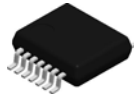
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

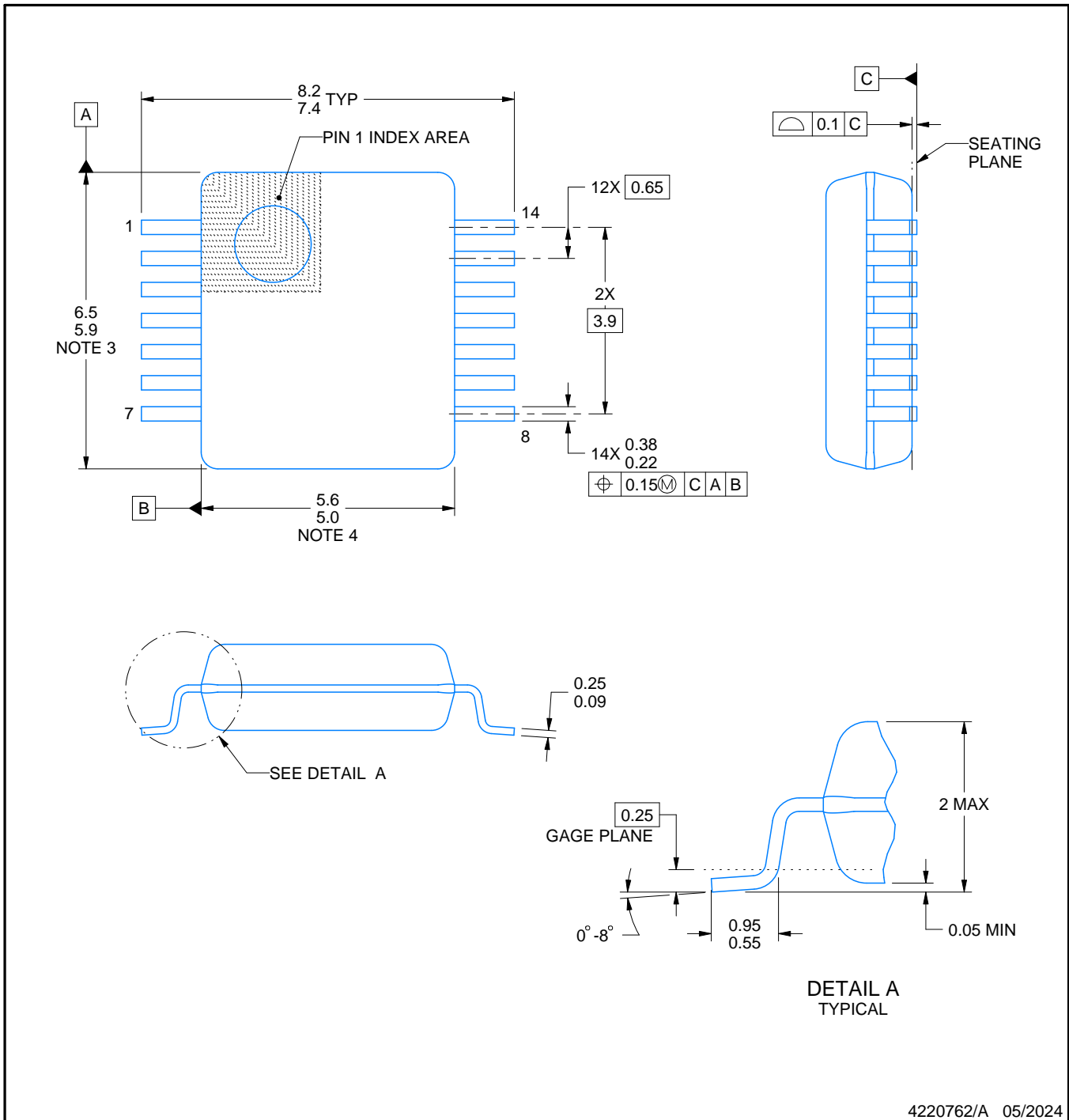
# DB0014A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



### NOTES:

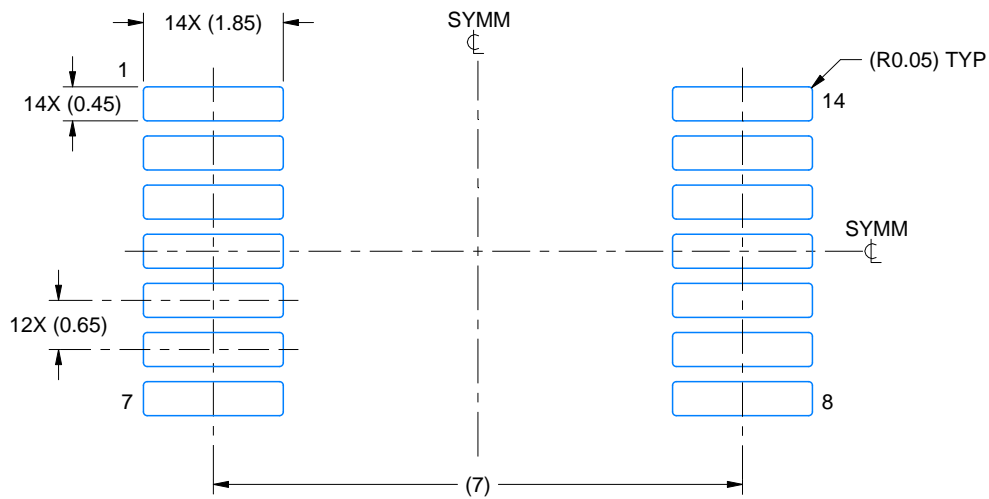
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

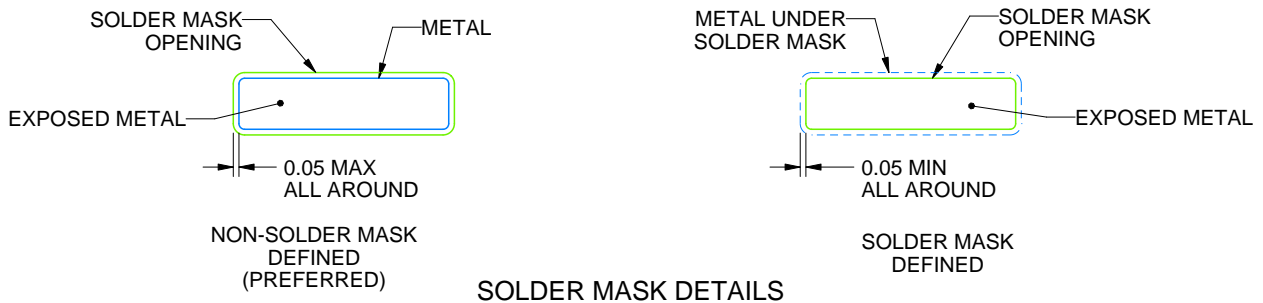
DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

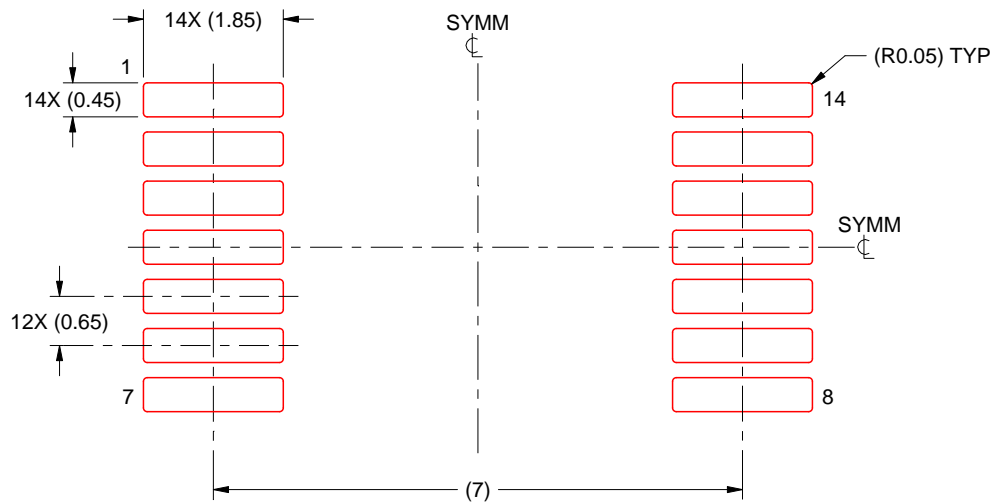
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



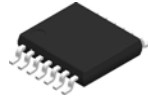
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

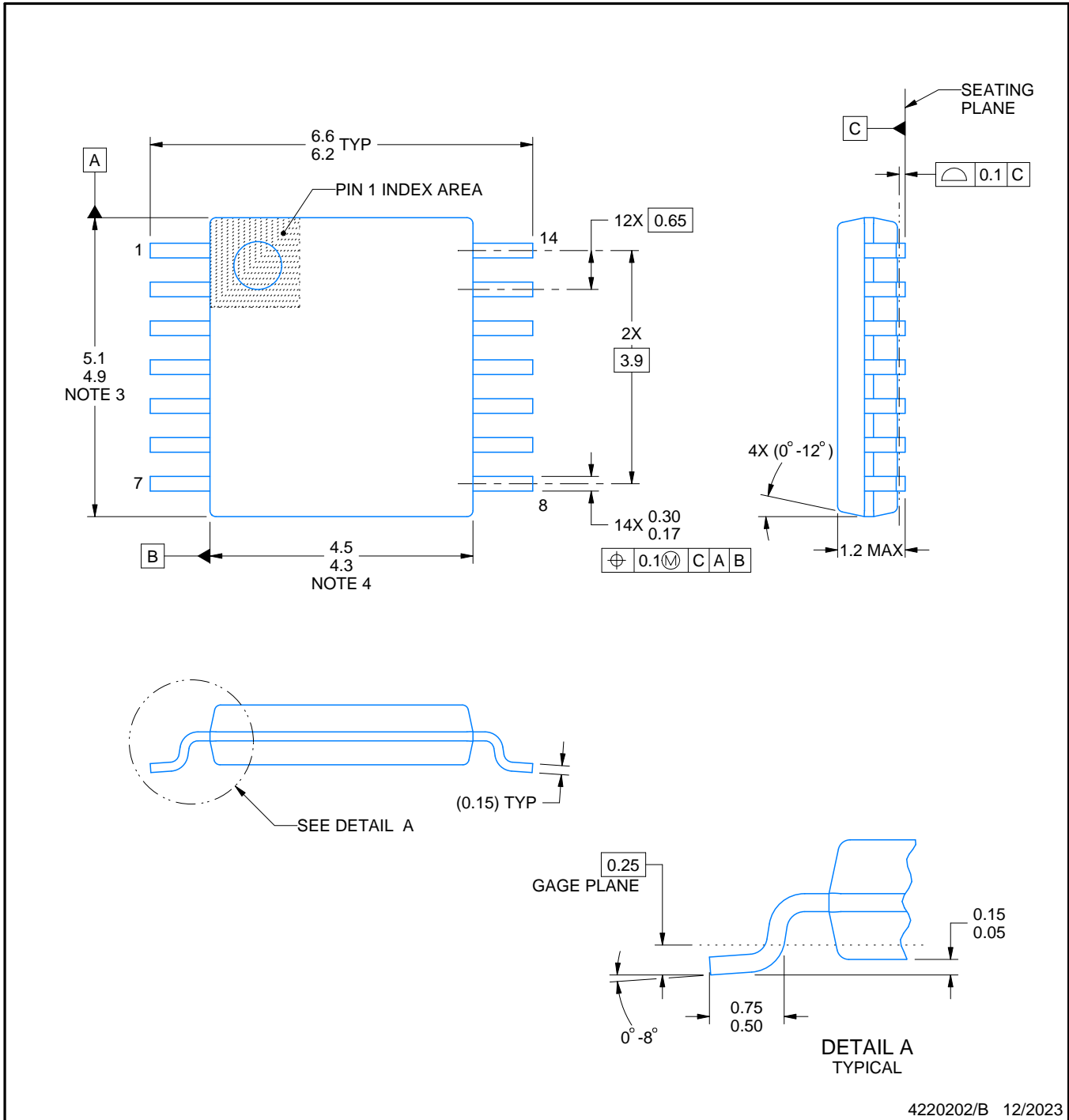
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

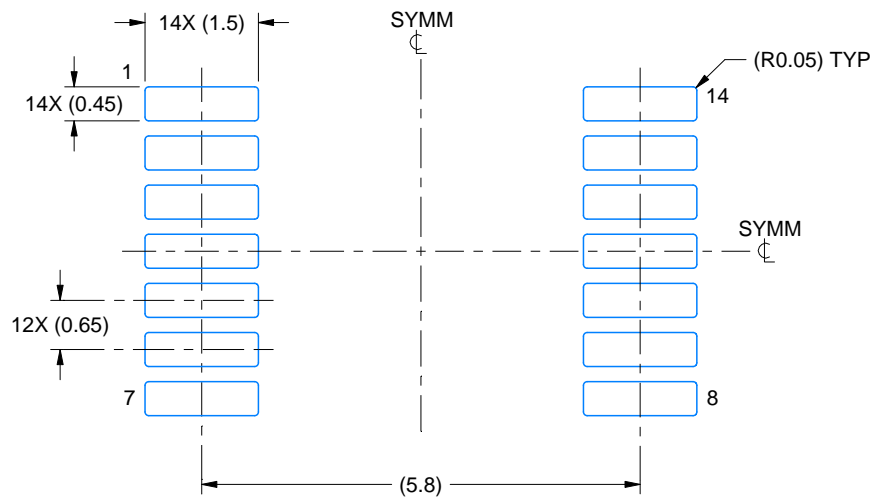
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

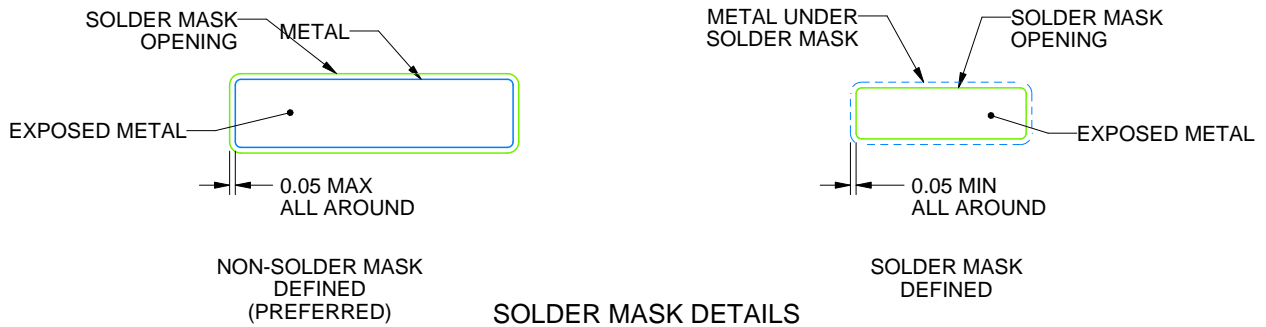
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

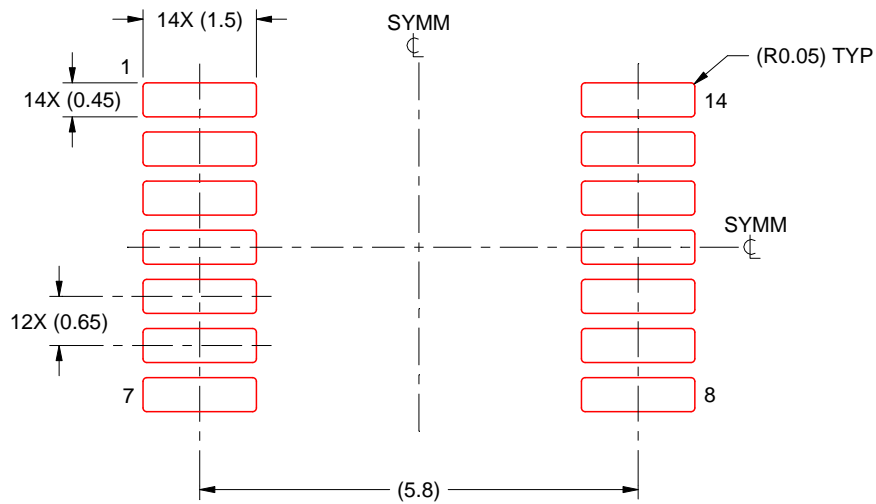
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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