

SN65ALS1176 差分总线收发器

1 特性

- 符合或超出 TIA/EIA-422-B、TIA/EIA-485-A 和 ITU 建议 V.11 和 X.27 的要求
- 在高达 35MBaud 的数据速率下运行
- 工作温度范围：-25°C 至 85°C
- 适用于嘈杂环境中的长距离总线线路上的多点传输
- 低电源电流要求：30 mA (最大值)
- 宽正负输入/输出总线电压范围
- 热关断保护
- 驱动器正负电流限制
- 接收器输入迟滞
- 无干扰上电和断电保护
- 接收器开路失效防护设计
- 封装选项包括塑料小外形尺寸 (D) 封装和 (P) 突降

2 应用

- PROFIBUS

3 说明

SN65ALS1176 差分总线收发器旨在实现多点总线传输线路上的双向数据通信。该器件专为平衡传输线路而设计，符合 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 ITU 建议 V.11 和 X.27。

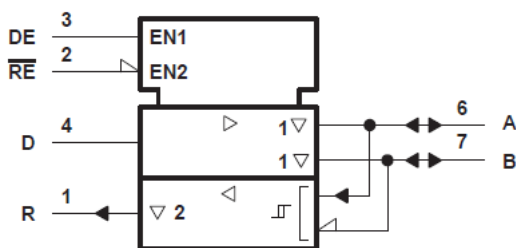
SN65ALS1176 将一个三态差分线路驱动器和一个差分输入线路接收器组合在一起，这两个器件由一个 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，这些端口用于在禁用驱动器或 $V_{CC} = 0$ 时为总线提供最小负载。该端口具有正负宽共模电压范围，使得该器件非常适用于合用线应用。

SN65ALS1176 的额定工作温度范围是 -25°C 至 85°C。

封装信息

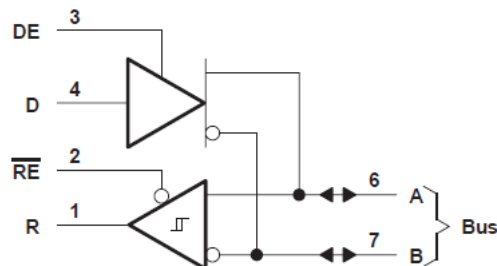
器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN65ALS1176	D (SOIC)	4.9 mm x 3.91 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



A. 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

逻辑符号



逻辑图 (正逻辑)



Table of Contents

1 特性	1	8 Detailed Description	11
2 应用	1	8.1 Functional Block Diagram.....	11
3 说明	1	8.2 Device Functional Modes.....	11
4 Revision History	2	9 Application and Implementation	12
5 Pin Configuration and Functions	3	9.1 Application Information.....	12
6 Specifications	4	10 Device and Documentation Support	13
6.1 Absolute Maximum Ratings	4	10.1 Documentation Support.....	13
6.2 Recommended Operating Conditions.....	4	10.2 接收文档更新通知.....	13
6.3 Thermal Information.....	4	10.3 支持资源.....	13
6.4 Electrical Characteristics - Driver	5	10.4 Trademarks.....	13
6.5 Switching Characteristics - Driver.....	5	10.5 静电放电警告.....	13
6.6 Symbol Equivalents.....	6	10.6 术语表.....	13
6.7 Electrical Characteristics - Receiver.....	7	11 Mechanical, Packaging, and Orderable Information	13
6.8 Switching Characteristics - Receiver.....	7		
7 Parameter Measurement Information	8		

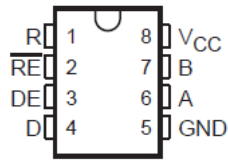
4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 1999) to Revision B (January 2023)	Page
• 将文档更改为了最新 TI 格式.....	1
• Deleted the P package option.....	3
• Deleted the Package thermal impedance from the <i>Absolute Maximum Ratings</i>	4
• Added the <i>Thermal Information</i> table.....	4

Changes from Revision * (April 1998) to Revision A (December 1999)	Page
• 将文档从“产品预发布”更改为量产数据.....	1

5 Pin Configuration and Functions



A. The D package is available taped and reeled. Add the suffix R to the device type (for example, SN65ALS1176DR).

图 5-1. D Package (Top View)

表 5-1. Pin Functions

NO	Name	Type	Description
1	R	O	Receive data output
2	\overline{RE}	I	Receiver enable, active low
3	DE	I	Driver enable, active high
4	D	I	Driver data input
5	GND	GND	Local device ground
6	A	I/O	Driver output or receiver input (complementary to B)
7	B	I/O	Driver output or receiver input (complementary to A)
8	V_{CC}	SUPPLY	4.75-V to 5.25-V supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾		7	V
	Voltage range at any bus terminal	-7	12	V
V _I	Enable input voltage		5.5	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds)		260	°C
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	4.75	5	5.25	V
V _I or V _{IC}	Input voltage at any bus terminal (separately or common mode)			12	V
				-7	
V _{IH}	High-level input voltage	D, DE, and RE		2	V
V _{IL}	Low-level input voltage	D, DE, and RE		0.8	V
V _{ID}	Differential input voltage ⁽¹⁾			± 12	V
I _{OH}	High-level output current	Driver		-60	mA
		Receiver		-400	μA
I _{OL}	Low-level output current	Driver		60	mA
		Receiver		8	
T _A	Operating free-air temperature	-25		85	°C

- (1) Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

6.3 Thermal Information

THERMAL METRIC ⁽¹⁾		D (SOIC)	UNIT
		8-Pins	
R _{θJA}	Junction-to-ambient thermal resistance	116.7	°C/W
R _{θJC(top)}	Junction-to-case thermal resistance	56.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	63.4	°C/W
ψ _{JT}	Junction-to-top characterization parameter	8.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	62.6	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.4 Electrical Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾		MIN	TYP ⁽²⁾	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = - 18 mA				- 1.5	V
V _O	Output voltage	I _O = 0		0		6	V
V _{OD1}	Differential output voltage	I _O = 0		1.5		6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω	See 图 7-1	½ V _{OD1} or 2 ⁽³⁾			V
		R _L = 54 Ω	See 图 7-1	2.1	2.5	5	V
V _{OD3}	Differential output voltage	V _{test} = - 7 V to 12 V	See 图 7-2	1.5		5	V
Δ V _{OD}	Change in magnitude of differential output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω See 图 7-1				± 0.2	V
V _{OC}	Common-mode output voltage					3 - 1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage ⁽⁴⁾					± 0.2	V
I _O	Output current	Outputs disabled ⁽⁶⁾		V _O = 12 V		1	mA
				V _O = - 7 V		- 0.8	
I _{IH}	High-level input current	V _I = 2.4 V				20	μ A
I _{IL}	Low-level input current	V _I = 0.4 V				- 400	μ A
I _{OS}	Short-circuit output current ⁽⁵⁾	V _O = - 4 V				- 250	mA
		V _O = 0				- 150	
		V _O = V _{CC}				250	
		V _O = 8 V				250	
I _{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

- (1) The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
- (2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
- (3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
- (4) Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from one logic state to the other.
- (5) Duration of the short circuit should not exceed one second for this test.
- (6) This applies for both power on and power off; refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal

6.5 Switching Characteristics - Driver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω See 图 7-3	C _L = 50 pF,			15	ns
t _{sk(p)}	Pulse skew ⁽²⁾				0	2	ns
t _{t(OD)}	Differential output transition time				8		ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω See 图 7-4	C _L = 50 pF,			80	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω See 图 7-5	C _L = 50 pF,			30	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω See 图 7-4	C _L = 50 pF,			50	ns

6.5 Switching Characteristics - Driver (continued)

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
t_{PLZ}	Output disable time from low level	$R_L = 110 \Omega$ See 图 7-5	$C_L = 50 \text{ pF}$			30	ns

(1) All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

(2) Pulse skew is defined as the $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

6.6 Symbol Equivalents

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{Oa}, V_{Ob}	V_{Oa}, V_{Ob}
$ V_{OD1} $	V_o	V_o
$ V_{OD2} $	$V_t (R_L = 100 \Omega)$	$V_t (R_L = 54 \Omega)$
$ V_{OD3} $	None	V_t (test termination measurement 2)
$\Delta V_{OD} $	$ V_t - V_t $	$ V_t - V_t $
V_{OC}	$ V_{os} $	$ V_{os} $
$\Delta V_{OC} $	$ V_{os} - V_{os} $	$ V_{os} - V_{os} $
I_{OS}	$ I_{sa} , I_{sb} $	None
I_O	$ I_{xa} , I_{xb} $	I_{ia}, I_{ib}

6.7 Electrical Characteristics - Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IT+}	Positive-going input threshold voltage	V _O = 2.7 V,	I _O = - 0.4 mA			0.2	V
V _{IT-}	Negative-going input threshold voltage	V _O = 0.5 V,	I _O = 8 mA	- 0.2 ⁽²⁾			V
V _{hys}	Hysteresis voltage (V _{IT+} - V _{IT-})				60		mV
V _{IK}	Enable-input clamp voltage	I _I = - 18 mA				- 1.5	V
V _{OH}	High-level output voltage	V _{ID} = 200 mV, See Figure 6	I _{OH} = - 400 μA,	2.7			V
V _{OL}	Low-level output voltage	V _{ID} = - 200 mV, See 图 7-6	I _{OL} = 8 mA,			0.45	V
I _{OZ}	High-impedance-state output current	V _O = 0.4 V to 2.4 V				± 20	μA
V _I	Line input current	Other input = 0 V ⁽³⁾	V _I = 12 V			1	mA
			V _I = - 7 V			- 0.8	
I _{IH}	High-level-enable input current	V _{IH} = 2.7 V				20	m μA
I _{IL}	Low-level-enable input current	V _{IL} = 0.4 V				- 100	μA
r _I	Input resistance			12	20		kΩ
I _{OS}	Short-circuit output current	V _{ID} = 200 mV,	V _O = 0	- 15		- 85	mA
I _{CC}	Supply current	No load	Outputs enabled		23	30	mA
			Outputs disabled		19	26	

- (1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
- (2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
- (3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions.

6.8 Switching Characteristics - Receiver

over recommended ranges of supply voltage and operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽¹⁾	MAX	UNIT	
t _{pd}	Propagation time	V _{ID} = - 1.5 V to 1.5 V, See 图 7-7	C _L = 15 pF,			25	ns	
t _{sk(p)}	Pulse skew ⁽²⁾					0	2	ns
t _{PZH}	Output enable time to high level	C _L = 15 pF,	See 图 7-8		11	18	ns	
t _{PZL}	Output enable time to low level				11	18	ns	
t _{PHZ}	Output disable time from high level						50	ns
t _{PLZ}	Output disable time from low level						30	ns

- (1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
- (2) Pulse skew is defined as the |t_{PLH} - t_{PHL}| of each channel of the same device.

7 Parameter Measurement Information

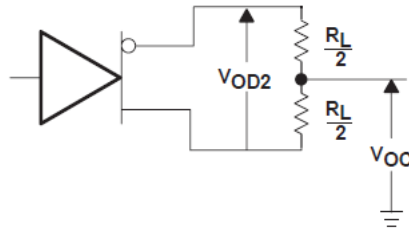


图 7-1. Driver V_{OD2} and V_{OC} Test Circuit

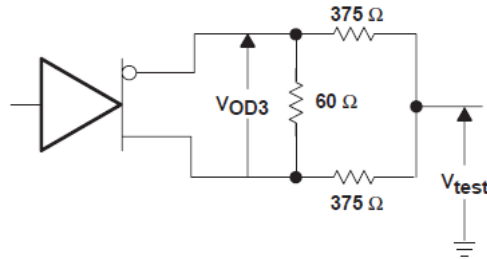
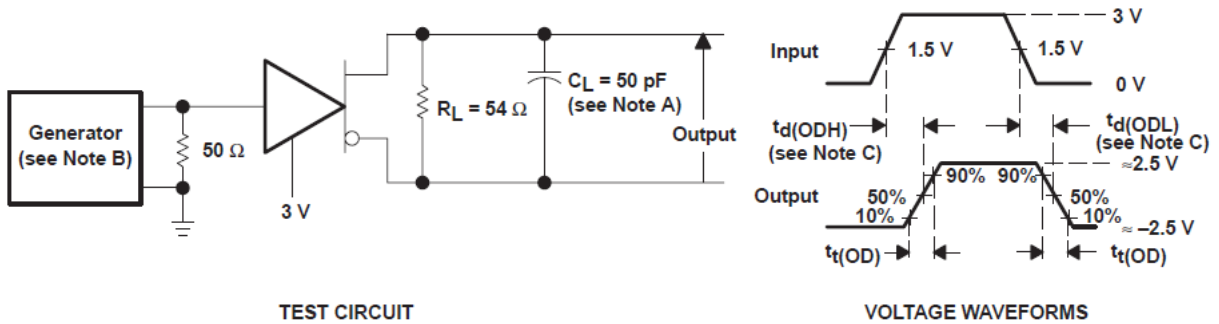
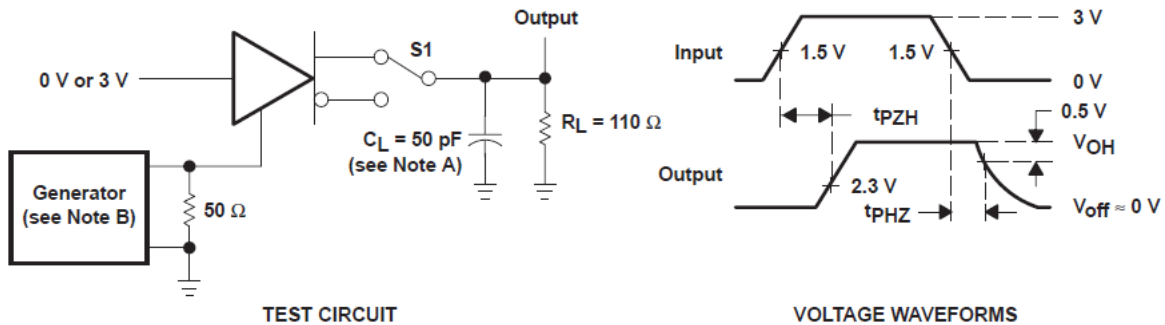


图 7-2. Driver V_{OD3} Test Circuit



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
- C. $t_{d(OD)} = t_{d(ODH)}$ or $t_{d(ODL)}$.

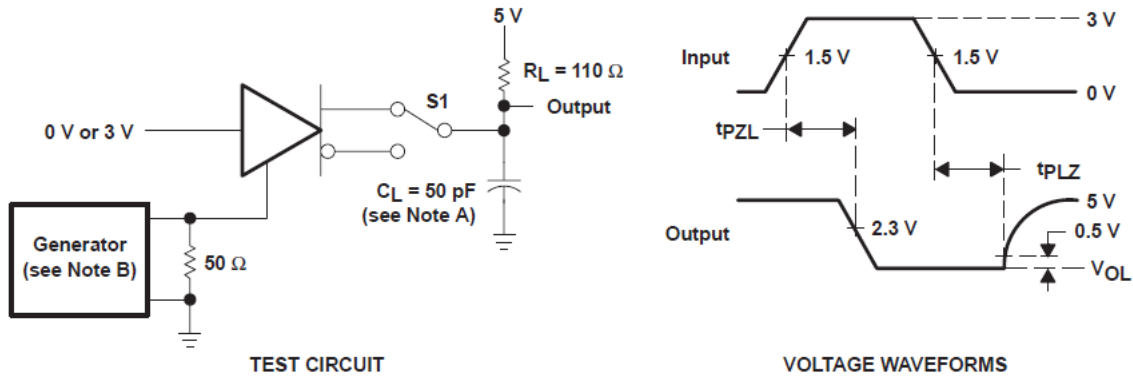
图 7-3. Driver Differential-Output Delay and Transition Times



- A. C_L includes probe and jig capacitance.

- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_o = 50 \Omega$.

图 7-4. Driver Enable and Disable Times



- A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_o = 50 \Omega$.

图 7-5. Driver Enable and Disable Times

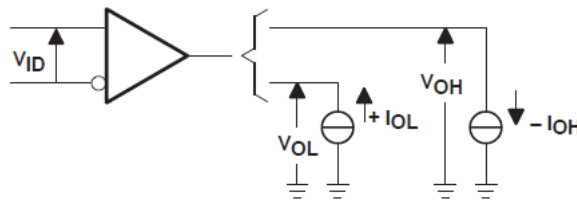
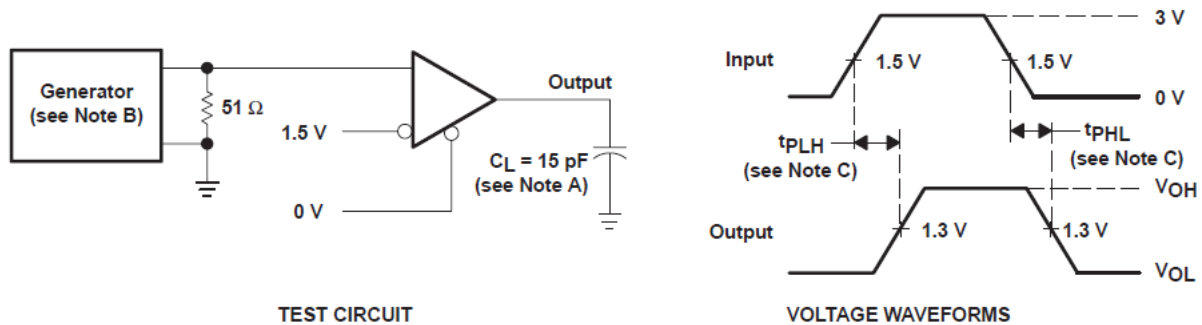
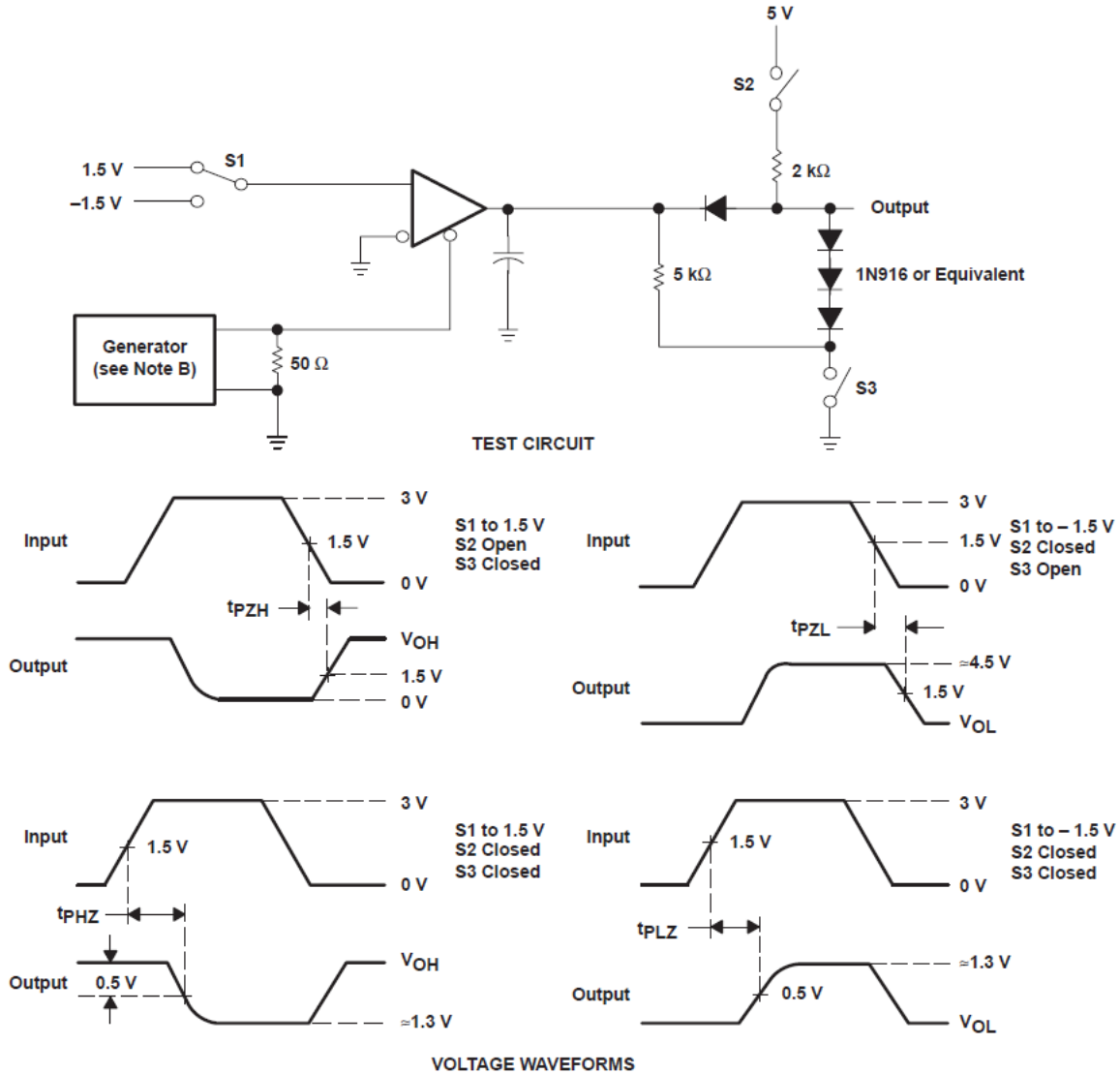


图 7-6. Receiver V_{OH} and V_{OL} Test Circuit



- A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_o = 50 \Omega$.
C. $t_{pd} = t_{PLH}$ or t_{PHL} .

图 7-7. Receiver Propagation-Delay Times



- A. C_L includes probe and jig capacitance.
- B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

图 7-8. Receiver Output Enable and Disable Times

8 Detailed Description

8.1 Functional Block Diagram

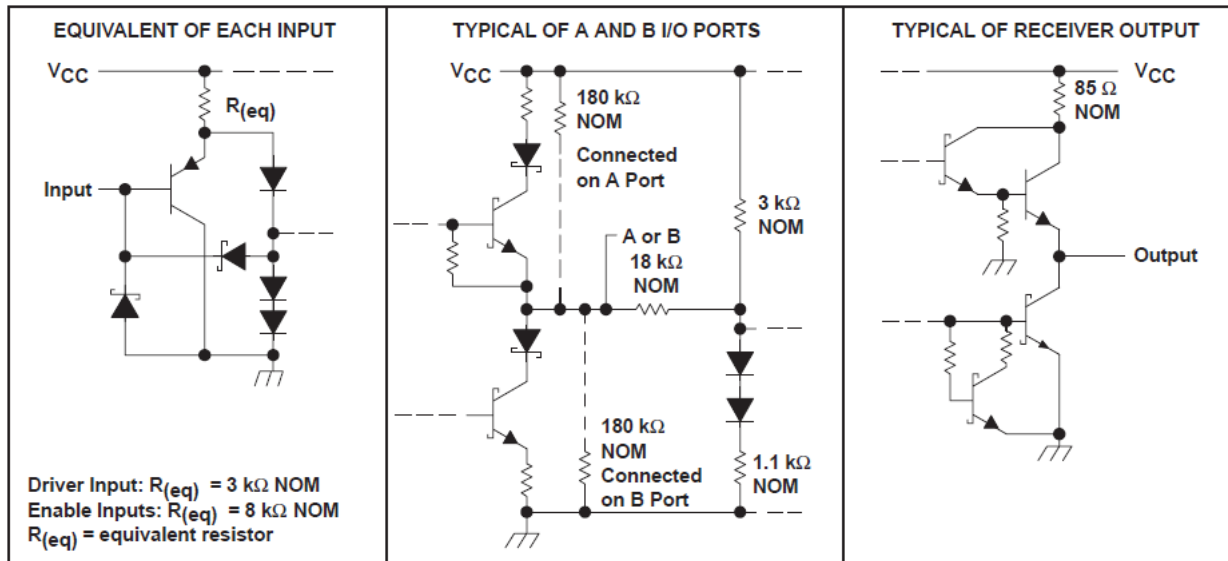


图 8-1. Schematics of Inputs and Outputs

8.2 Device Functional Modes

Function Tables

表 8-1. Driver⁽¹⁾

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off).

表 8-2. Receiver⁽¹⁾

DIFFERENTIAL INPUTS A - B	ENABLE RE	OUTPUT R
$V_{ID} \geq 0.2\text{ V}$	L	H
$-0.2\text{ V} < V_{ID} < 0.2\text{ V}$	L	?
$V_{ID} \leq -0.2\text{ V}$	L	L
X	H	Z
Inputs open	L	H

(1) H = high level, L = low level, X = irrelevant, ? = indeterminate, Z = high impedance (off).

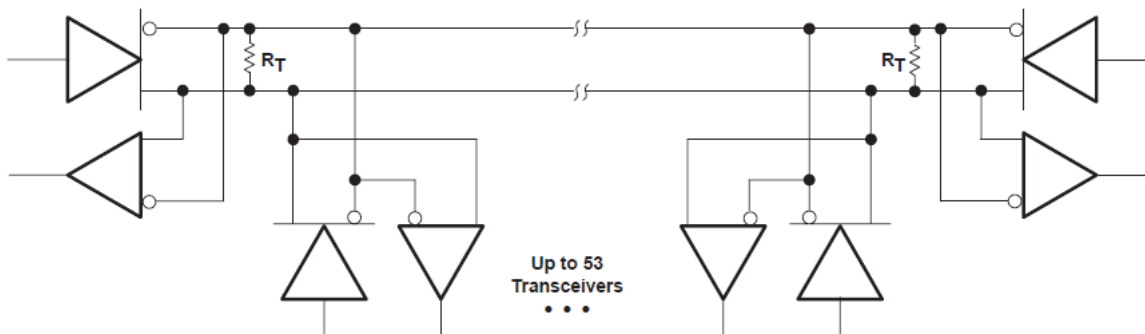
9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

9.1 Application Information

9.1.1 Typical Application



- A. The line should terminate at both ends in its characteristic impedance ($R_T = Z_0$). Stub lengths off the main line should be kept as short as possible.

图 9-1. Typical Application Circuit

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65ALS1176D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 85	6A1176	
SN65ALS1176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	6A1176	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65ALS1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65ALS1176DR	SOIC	D	8	2500	356.0	356.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司