OPA2188 0.03μV/°C 漂移、低噪声、轨到轨输出、36V、零漂移运算放大器

1 特性

- 低偏移电压：25μV（最大）
- 零漂移：0.03μV/°C
- 低噪声：8.8 nV/√Hz
  0.1Hz 至 10Hz 噪声：0.25μV_{PP}
- 出色的直流精度：
  电源抑制比 (PSRR)：142dB
  共模抑制比 (CMRR)：146dB
  开环路增益：136dB
- 增益带宽：2MHz
- 静态电流：475μA（最大值）
- 宽电源电压：±2V 至 ±18V
- 轨到轨输出：
  输入包括负电源轨
- 已过滤射频干扰 (RFI) 的输入
- 微型尺寸封装

2 应用范围

- 桥式放大器
- 应力计
- 测试设备
- 传感器 应用
- 温度测量
- 电子称
- 医疗仪表
- 电阻式温度检测器
- 精密有源滤波器

3 说明

OPA2188 运算放大器采用 TI 专有的自动归零技术，可在时间和温度范围内提供低偏移电压（25μV，最大值）以及近似为零的漂移。这些微型的、高精度、低静态电流放大器提供高输入阻抗和摆幅为电源轨 15mV 之内的轨到轨输出。输入共模范围包括负电源轨。单电源或双电源可在 4V 至 36V（±2V 至 ±18V）范围内使用。

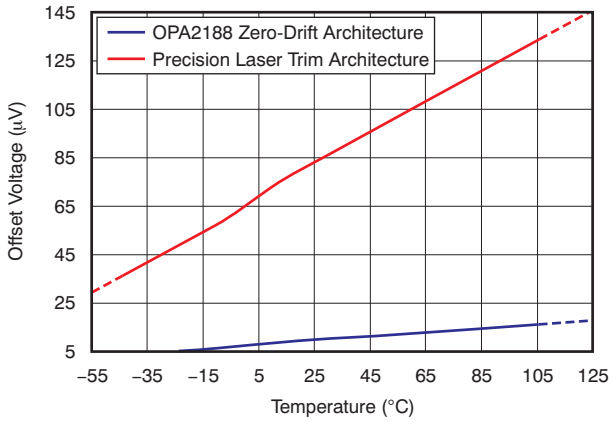
OPA2188 器件采用微型小外形尺寸 (MSOP)-8 和小外形尺寸 (SO)-8 封装。此器件的额定工作温度范围为 —40°C 至 +105°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA2188	SOIC (8)	4.90mm x 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

偏移电压与温度间的关系



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (September 2012) to Revision C — **Page**

- 已添加 *ESD 额定值表，特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- Changed Input Bias Current, I_B and I_{OS} parameters overtemperature maximum specification in *Electrical Characteristics: High-Voltage Operation* table ... 5
- Changed Noise, *Input voltage noise density* parameter units in *Electrical Characteristics: High-Voltage Operation* table ... 5
- Changed Power Supply, I_Q parameter maximum specifications in *Electrical Characteristics: High-Voltage Operation* table ... 6
- Changed Input Bias Current, I_B and I_{OS} parameters overtemperature maximum specification in *Electrical Characteristics: Low-Voltage Operation* table ... 7
- Changed Noise, *Input voltage noise density* parameter units in *Electrical Characteristics: Low-Voltage Operation* table ... 7
- Changed Power Supply, I_Q parameter maximum specifications in *Electrical Characteristics: Low-Voltage Operation* table ... 8

Changes from Revision A (June 2012) to Revision B — **Page**

- 已更改 第二个至最后一个 应用 要点） ... 1

Changes from Original (August 2011) to Revision A — **Page**

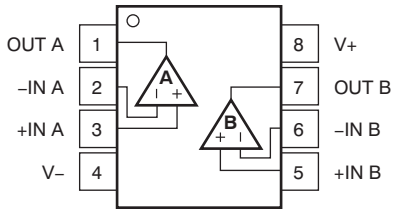
- 已删除 通篇所有对 OPA188 和 OPA4188 的引用 ... 1
- 已按当前标准更改文档 ... 1
- 已更改 文档状态至*量产数据* ... 1

5 Zero-Drift Amplifier Portfolio

VERSION	PRODUCT	OFFSET VOLTAGE (µV)	OFFSET VOLTAGE DRIFT (µV/°C)	BANDWIDTH (MHz)
Single	OPA188 (4 V to 36 V)	25	0.085	2
	OPA333 (5 V)	10	0.05	0.35
	OPA378 (5 V)	50	0.25	0.9
	OPA735 (12 V)	5	0.05	1.6
Dual	OPA2188 (4 V to 36 V)	25	0.085	2
	OPA2333 (5 V)	10	0.05	0.35
	OPA2378 (5 V)	50	0.25	0.9
	OPA2735 (12 V)	5	0.05	1.6
Quad	OPA4188 (4 V to 36 V)	25	0.085	2
	OPA4330 (5 V)	50	0.25	0.35

6 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and MSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN A	2	I	Negative (inverting) input signal, channel A
–IN B	6	I	Negative (inverting) input signal, channel B
+IN A	3	I	Positive (noninverting) input signal, channel A
+IN B	5	I	Positive (noninverting) input signal, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V–	4	—	Negative (lowest) power supply
V+	8	—	Positive (highest) power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Supply voltage		±20, 40 (single supply)	V
	Signal input terminals, voltage(2)	(V–) – 0.5	(V+) + 0.5	V
Current	Signal input terminals, current(2)	–10	10	mA
	Output short-circuit(3)	Continuous		
Temperature	Operating, T_A	–55	125	°C
	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current-limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	4 (±2)		36 (±18)	V
T_A	Specified temperature range	-40		+105	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPA2188ID D (SOIC) 8 PINS	OPA2188IDGK DGK (VSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111	159.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.9	37.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.7	48.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	1.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.1	77.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

7.5 Electrical Characteristics: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			6	25	µV
		T_A = –40°C to +105°C		0.03	0.085	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.075	0.3	µV/V
		V_S = 4 V to 36 V, V_{CM} = V_S / 2, T_A = –40°C to +105°C			0.3	µV/V
	Long-term stability			4 (1)		µV
	Channel separation, DC			1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±160	±850	pA
		T_A = –40°C to +105°C			±18	nA
I_{OS}	Input offset current			±320	±1700	pA
		T_A = –40°C to +105°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.25		μV_{PP}
e_n	Input voltage noise density	f = 1 kHz		8.8		nV/√Hz
i_n	Input current noise density	f = 1 kHz		7		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage		V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	120	134		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V	130	146		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±18 V, T_A = –40°C to +105°C	120	126		dB
INPUT IMPEDANCE						
	Differential			100 || 6		MΩ || pF
	Common-mode			6 || 9.5		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	130	136		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ, T_A = –40°C to +105°C	120	126		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/µs
	Settling time, 0.1%	V_S = ±18 V, G = 1, 10-V step		20		µs
	Settling time, 0.01%	V_S = ±18 V, G = 1, 10-V step		27		µs
	Overload recovery time	V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

Electrical Characteristics: High-Voltage Operation, V_S = ±4 V to ±18 V (V_S = 8 V to 36 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		R_L = 10 kΩ, T_A = –40°C to +105°C		310	350	mV
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage		4 to 36 (±2 to ±18)			V
I_Q	Quiescent current (per amplifier)	V_S = ±4 V to V_S = ±18 V		415	510	μA
		I_O = 0 mA, T_A = –40°C to +105°C			600	μA

7.6 Electrical Characteristics: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage			6	25	µV
		T_A = –40°C to +105°C		0.03	0.085	µV/°C
PSRR	Power-supply rejection ratio	V_S = 4 V to 36 V, V_{CM} = V_S / 2		0.075	0.3	µV/V
		V_S = 4 V to 36 V, V_{CM} = V_S / 2, T_A = –40°C to +105°C			0.3	µV/V
	Long-term stability			4(1)		µV
	Channel separation, dc			1		µV/V
INPUT BIAS CURRENT						
I_B	Input bias current	V_{CM} = V_S / 2		±160	±850	pA
		T_A = –40°C to +105°C			±18	nA
I_{OS}	Input offset current			±320	±1700	pA
		T_A = –40°C to +105°C			±6	nA
NOISE						
e_n	Input voltage noise	f = 0.1 Hz to 10 Hz		0.25		μV_{PP}
	Input voltage noise density	f = 1 kHz		8.8		nV/√Hz
i_n	Input current noise density	f = 1 kHz		7		fA/√Hz
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	T_A = –40°C to +105°C	V–		(V+) – 1.5	V
CMRR	Common-mode rejection ratio	(V–) < V_{CM} < (V+) – 1.5 V	106	114		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V	114	120		dB
		(V–) + 0.5 V < V_{CM} < (V+) – 1.5 V, V_S = ±2 V, T_A = –40°C to +105°C	110	120		dB
INPUT IMPEDANCE						
	Differential			100 || 6		MΩ || pF
	Common-mode			6 || 95		10^{12} Ω || pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 5 kΩ, V_S = 5 V	110	120		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ	120	130		dB
		(V–) + 500 mV < V_O < (V+) – 500 mV, R_L = 10 kΩ, T_A = –40°C to +105°C	114	120		dB
FREQUENCY RESPONSE						
GBW	Gain-bandwidth product			2		MHz
SR	Slew rate	G = +1		0.8		V/µs
	Overload recovery time	V_{IN} × G = V_S		1		µs
THD+N	Total harmonic distortion + noise	1 kHz, G = 1, V_{OUT} = 1 V_{RMS}		0.0001		%

(1) 1000-hour life test at +125°C demonstrated randomly distributed variation in the range of measurement limits—approximately 4 µV.

Electrical Characteristics: Low-Voltage Operation, V_S = ±2 V to < ±4 V (V_S = +4 V to < +8 V) (continued)

at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, and V_{COM} = V_{OUT} = V_S/2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
	Voltage output swing from rail	No load		6	15	mV
		R_L = 10 kΩ		220	250	mV
		R_L = 10 kΩ, T_A = –40°C to +105°C		310	350	mV
I_{SC}	Short-circuit current			±18		mA
R_O	Open-loop output resistance	f = 1 MHz, I_O = 0		120		Ω
C_{LOAD}	Capacitive load drive			1		nF
POWER SUPPLY						
V_S	Operating voltage range		4 to 36 (±2 to ±18)			V
I_Q	Quiescent current (per amplifier)	V_S = ±2 V to V_S = ±4 V		385	485	μA
		I_O = 0 mA, T_A = –40°C to +105°C			590	μA
TEMPERATURE RANGE						
	Specified temperature range		–40		105	°C
T_A	Operating temperature range		–40		125	°C
T_{stg}	Storage temperature		–65		150	°C

7.7 Typical Characteristics: Table of Graphs

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE NO.
Offset Voltage Production Distribution	Figure 1
Offset Voltage Drift Distribution	Figure 2
Offset Voltage vs Temperature	Figure 3
Offset Voltage vs Common-Mode Voltage	Figure 4, Figure 5
Offset Voltage vs Power Supply	Figure 6
I_B and I_{OS} vs Common-Mode Voltage	Figure 7
Input Bias Current vs Temperature	Figure 8
Output Voltage Swing vs Output Current (Maximum Supply)	Figure 9
CMRR and PSRR vs Frequency (Referred-to-Input)	Figure 10
CMRR vs Temperature	Figure 11, Figure 12
PSRR vs Temperature	Figure 13
0.1-Hz to 10-Hz Noise	Figure 14
Input Voltage Noise Spectral Density vs Frequency	Figure 15
THD+N Ratio vs Frequency	Figure 16
THD+N vs Output Amplitude	Figure 17
Quiescent Current vs Supply Voltage	Figure 18
Quiescent Current vs Temperature	Figure 19
Open-Loop Gain and Phase vs Frequency	Figure 20
Closed-Loop Gain vs Frequency	Figure 21
Open-Loop Gain vs Temperature	Figure 22
Open-Loop Output Impedance vs Frequency	Figure 23
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	Figure 24, Figure 25
No Phase Reversal	Figure 26
Positive Overload Recovery	Figure 27
Negative Overload Recovery	Figure 28
Small-Signal Step Response (100 mV)	Figure 29, Figure 30
Large-Signal Step Response	Figure 31, Figure 32
Large-Signal Settling Time (10-V Positive Step)	Figure 33
Large-Signal Settling Time (10-V Negative Step)	Figure 34
Short-Circuit Current vs Temperature	Figure 35
Maximum Output Voltage vs Frequency	Figure 36
Channel Separation vs Frequency	Figure 37
EMIRR IN+ vs Frequency	Figure 38

7.8 Typical Characteristics

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

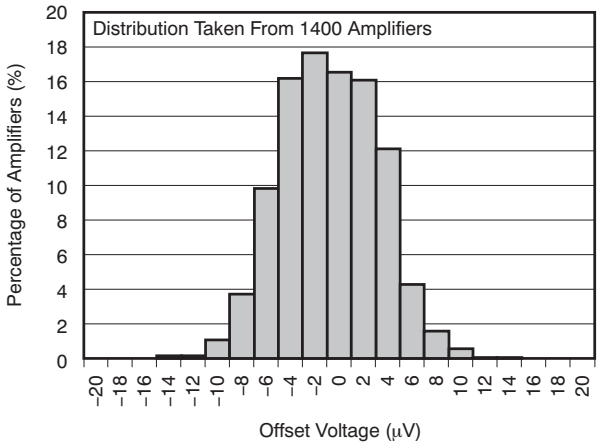


Figure 1. Offset Voltage Production Distribution

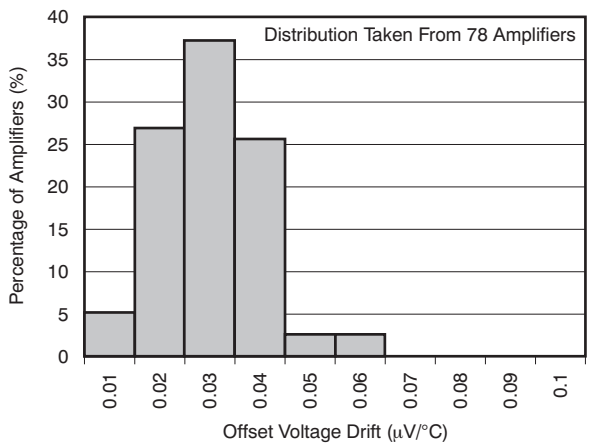


Figure 2. Offset Voltage Drift Distribution

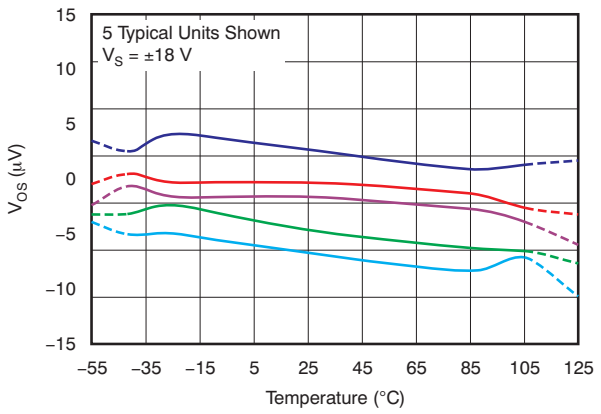


Figure 3. Offset Voltage vs Temperature

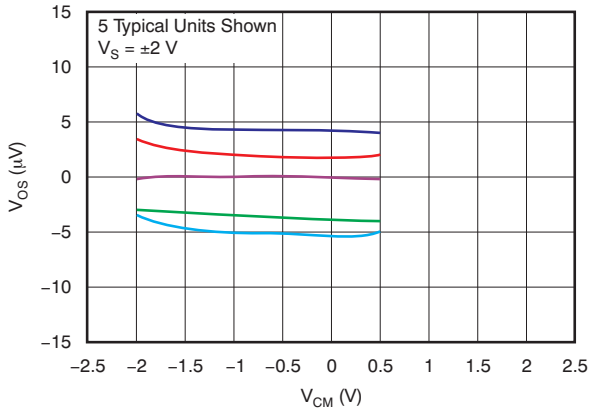


Figure 4. Offset Voltage vs Common-Mode Voltage

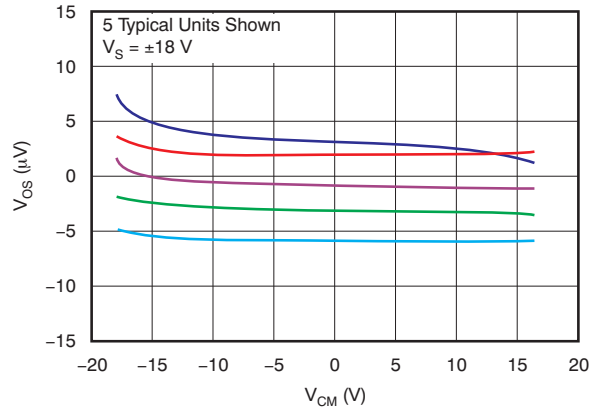


Figure 5. Offset Voltage vs Common-Mode Voltage

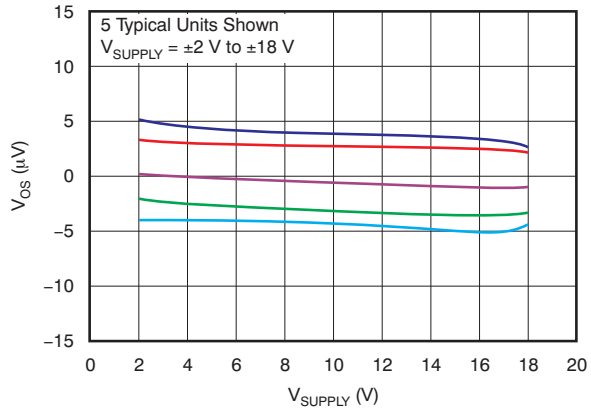


Figure 6. Offset Voltage vs Power Supply

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

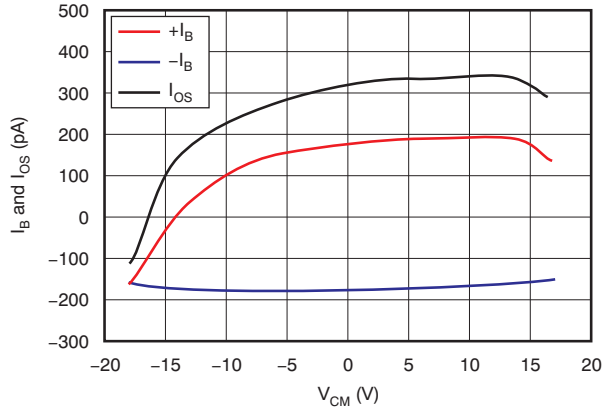


Figure 7. I_B and I_{OS} vs Common-Mode Voltage

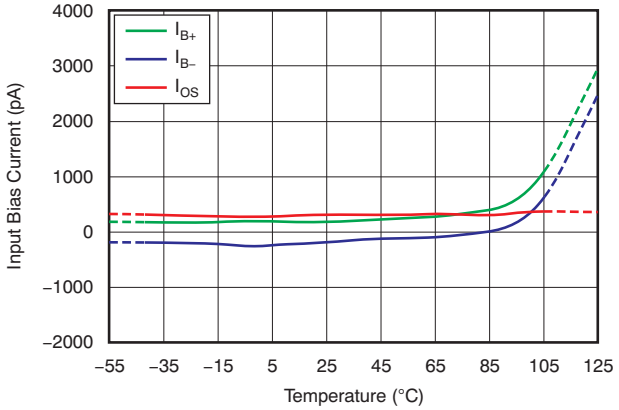


Figure 8. Input Bias Current vs Temperature

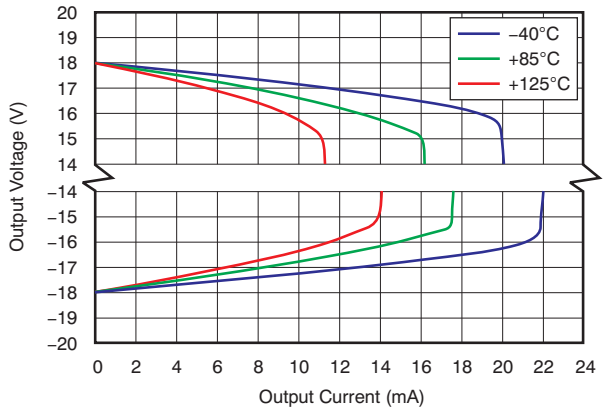


Figure 9. Output Voltage Swing vs Output Current (Maximum Supply)

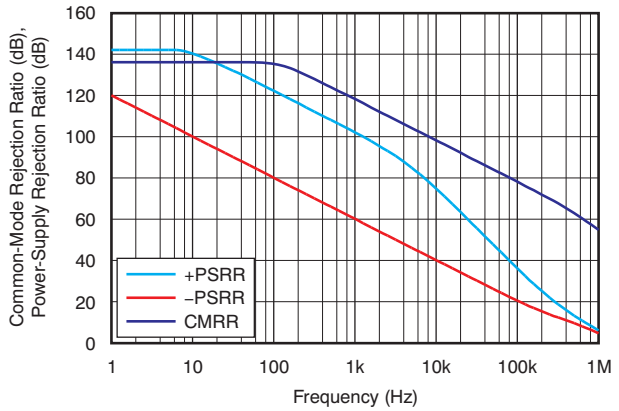


Figure 10. CMRR and PSRR vs Frequency (Referred-to-Input)

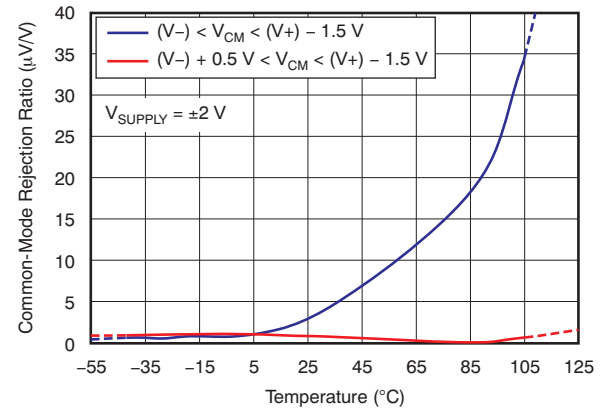


Figure 11. CMRR vs Temperature

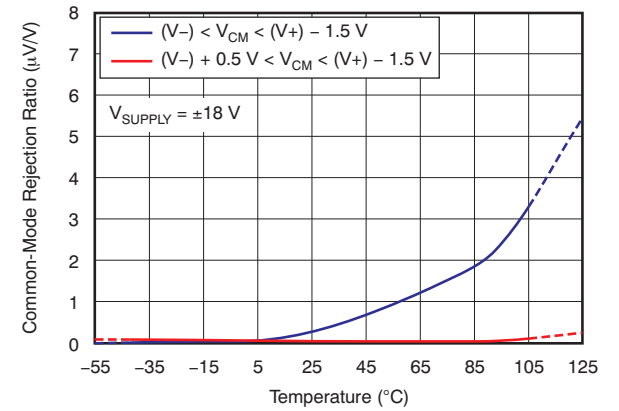


Figure 12. CMRR vs Temperature

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

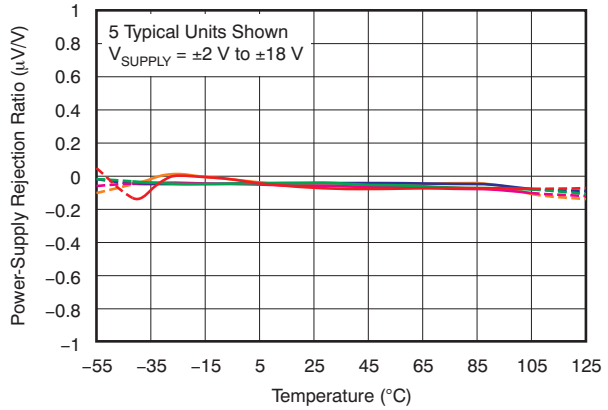


Figure 13. PSRR vs Temperature

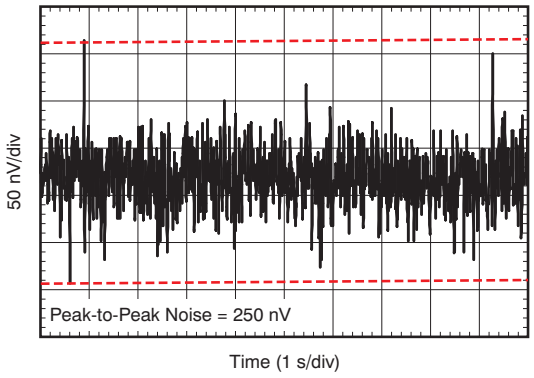


Figure 14. 0.1-Hz to 10-Hz Noise

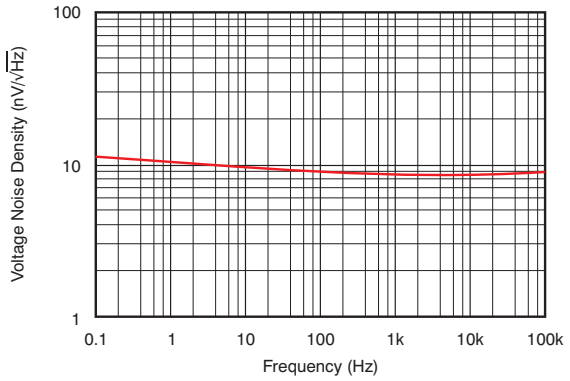


Figure 15. Input Voltage Noise Spectral Density vs Frequency

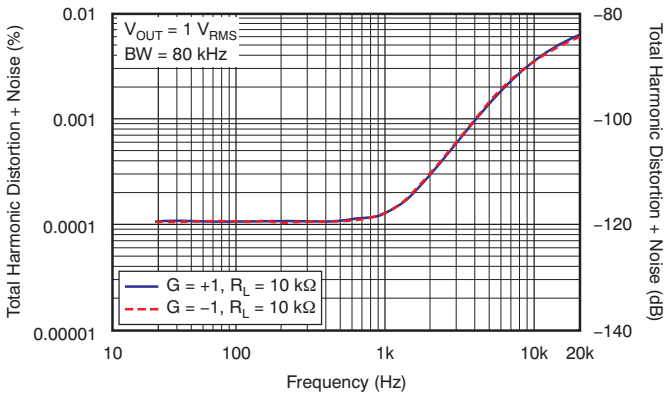


Figure 16. THD+N Ratio vs Frequency

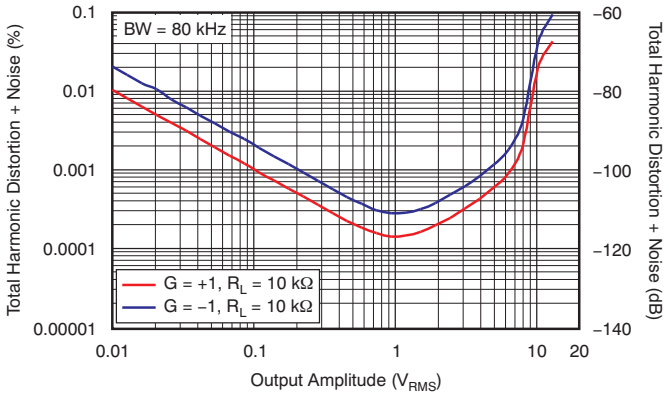


Figure 17. THD+N vs Output Amplitude

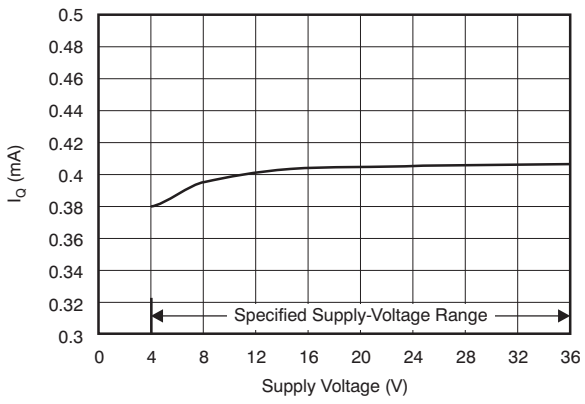


Figure 18. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

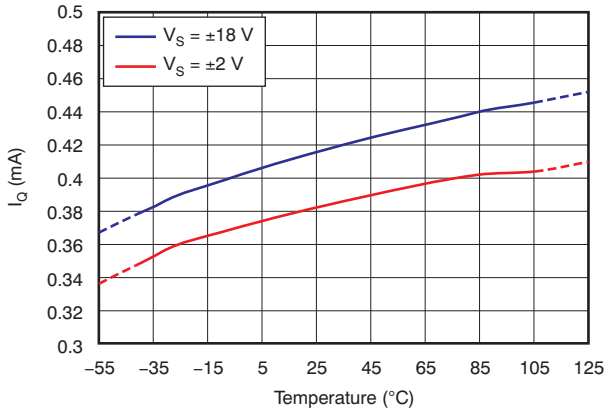


Figure 19. Quiescent Current vs Temperature

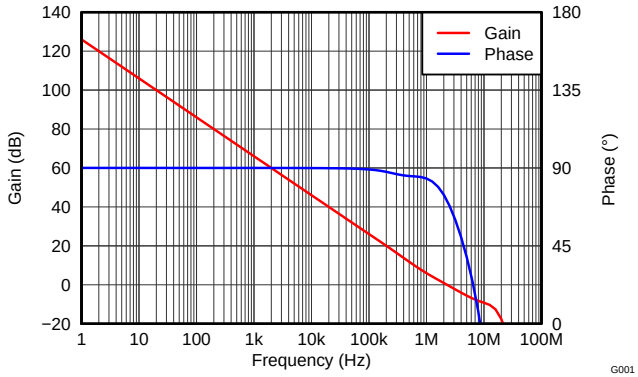


Figure 20. Open-Loop Gain and Phase vs Frequency

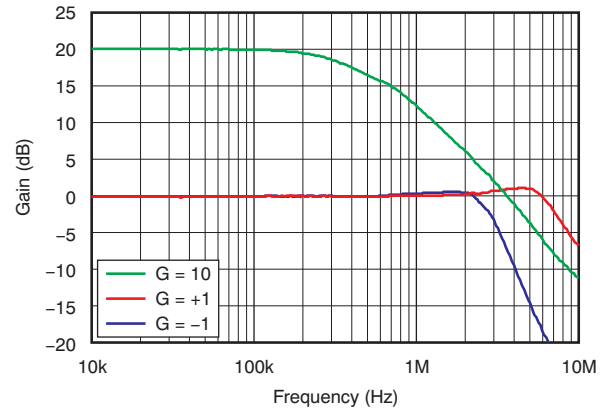


Figure 21. Closed-Loop Gain vs Frequency

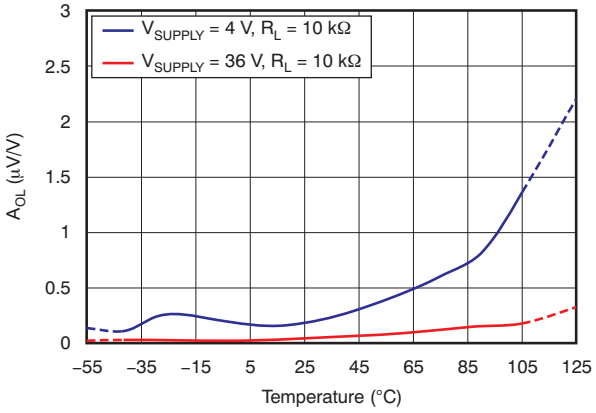


Figure 22. Open-Loop Gain vs Temperature

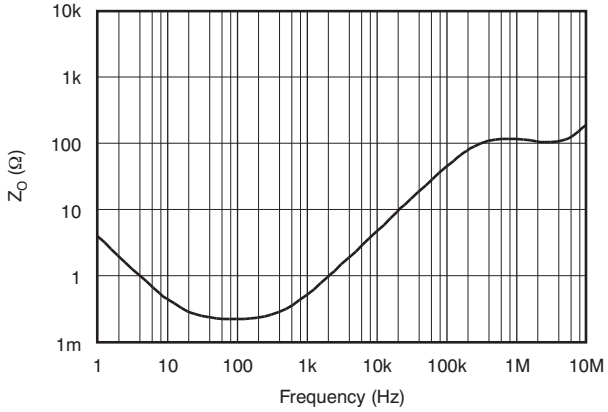


Figure 23. Open-Loop Output Impedance vs Frequency

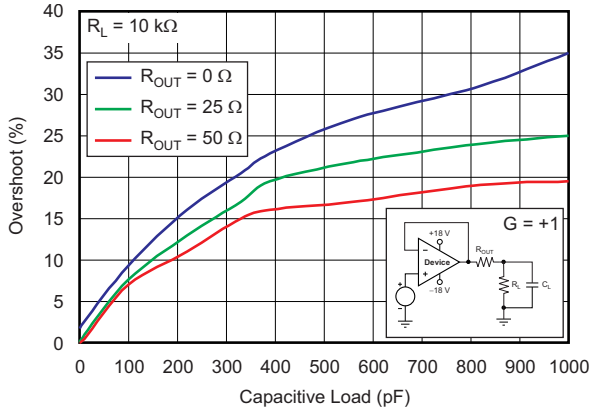


Figure 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

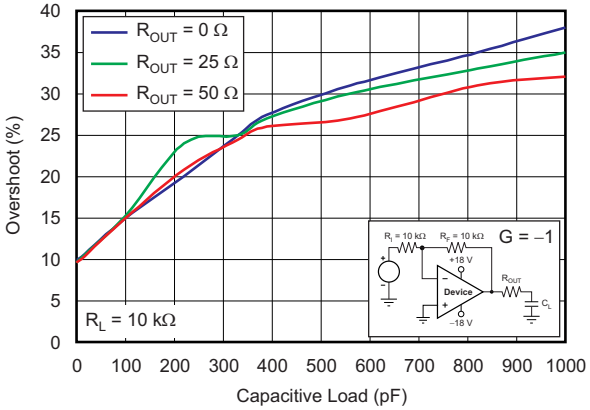


Figure 25. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

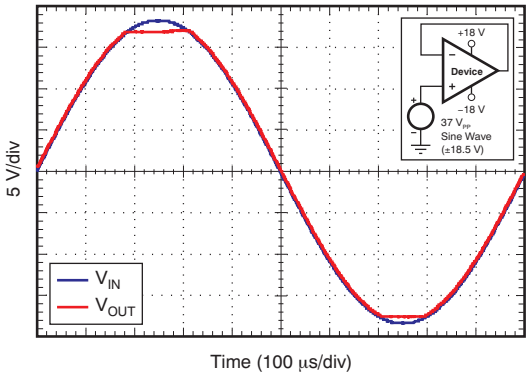


Figure 26. No Phase Reversal

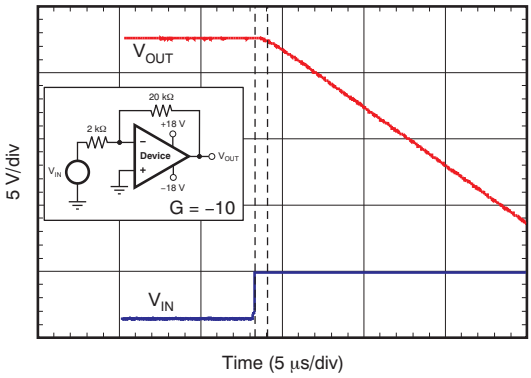


Figure 27. Positive Overload Recovery

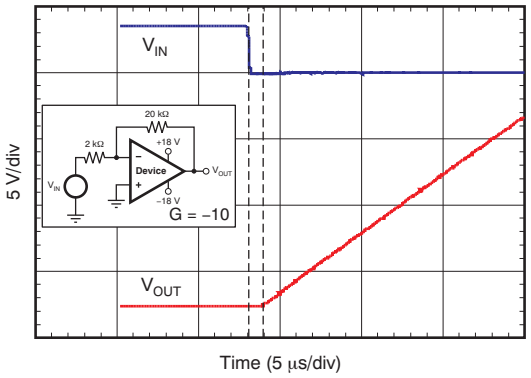


Figure 28. Negative Overload Recovery

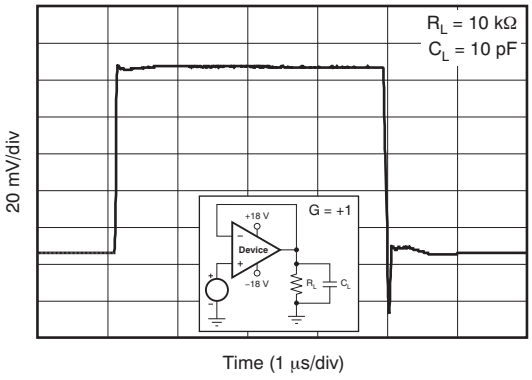


Figure 29. Small-Signal Step Response (100 mV)

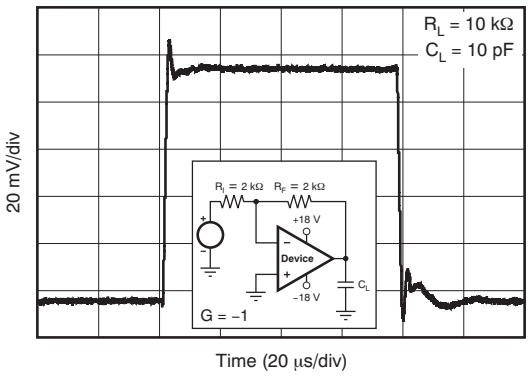


Figure 30. Small-Signal Step Response (100 mV)

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

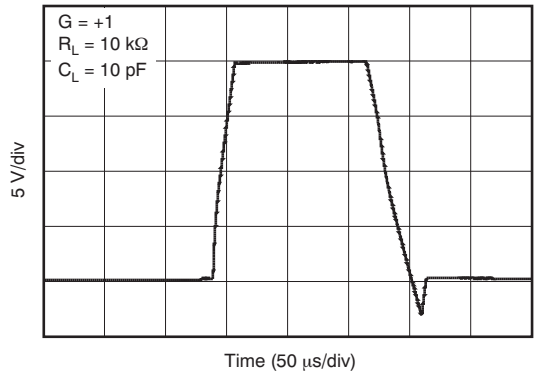


Figure 31. Large-Signal Step Response

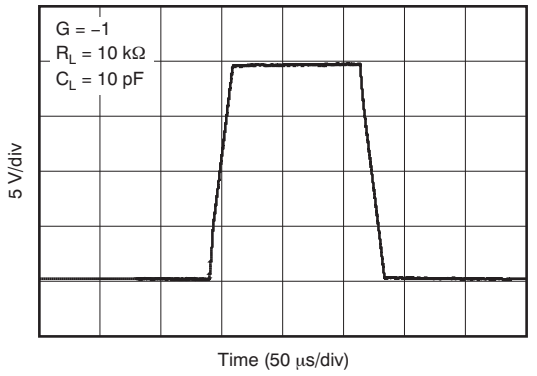


Figure 32. Large-Signal Step Response

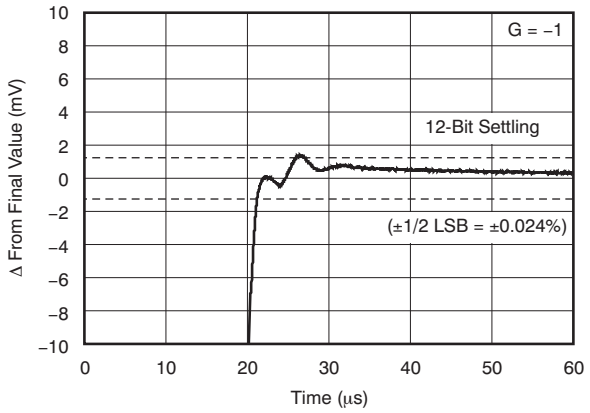


Figure 33. Large-Signal Settling Time (10-V Positive Step)

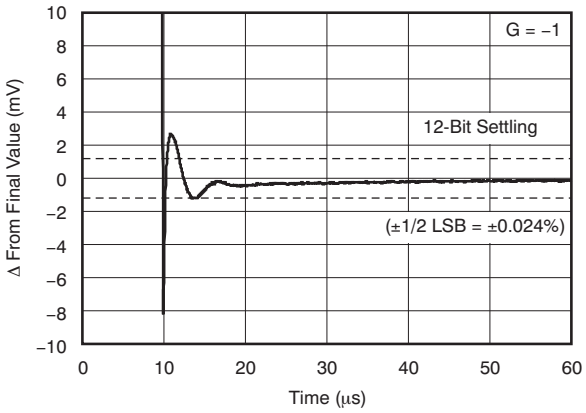


Figure 34. Large-Signal Settling Time (10-V Negative Step)

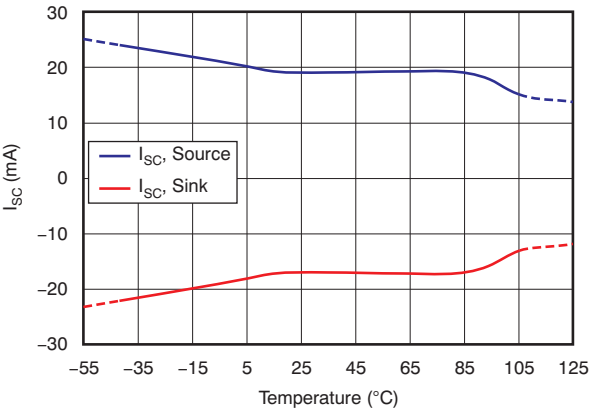


Figure 35. Short-Circuit Current vs Temperature

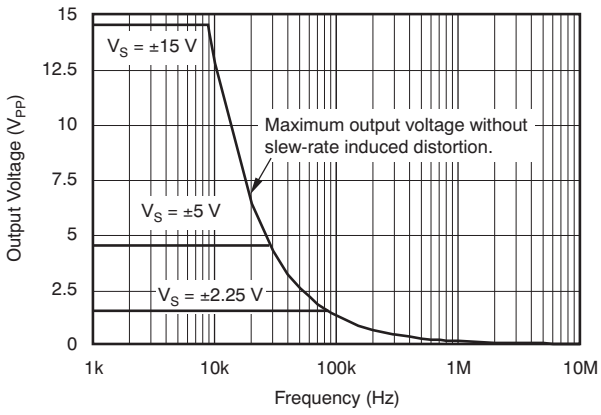


Figure 36. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

V_S = ±18 V, V_{CM} = V_S/2, R_{LOAD} = 10 kΩ connected to V_S/2, and C_L = 100 pF, unless otherwise noted.

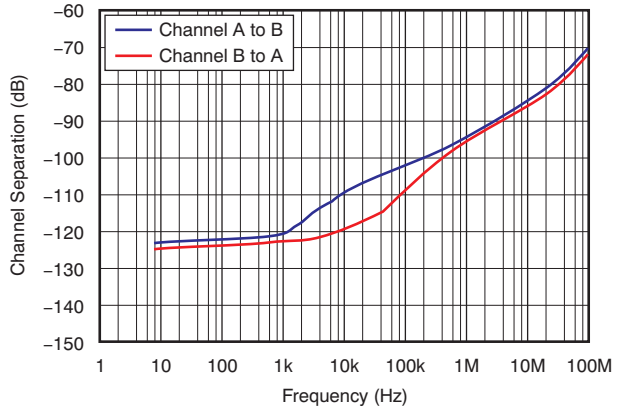


Figure 37. Channel Separation vs Frequency

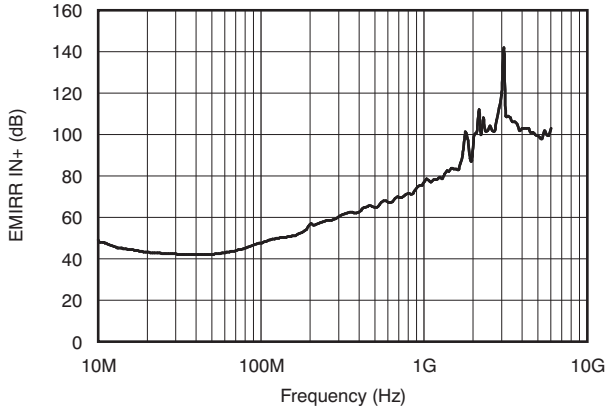


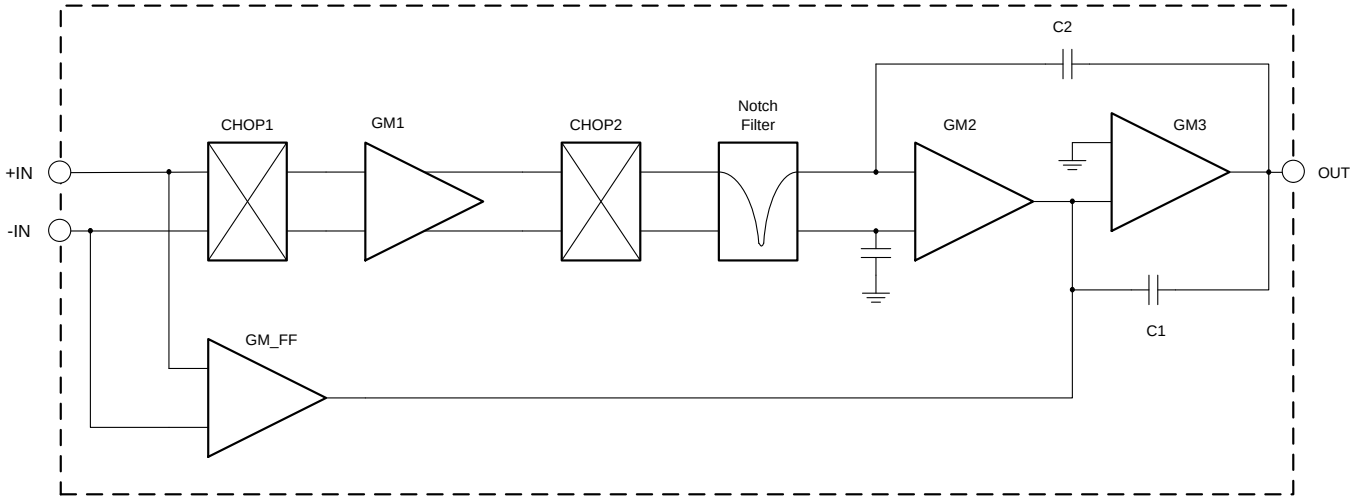
Figure 38. EMIRR IN+ vs Frequency

8 Detailed Description

8.1 Overview

The OPA2188 operational amplifier combines precision offset and drift with excellent overall performance, making the device ideal for many precision applications. The precision offset drift of only 0.085 µV/°C provides stability over the entire temperature range. In addition, the device offers excellent overall performance with high CMRR, PSRR, and A_{OL}. As with all amplifiers, applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1-µF capacitors are adequate.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Characteristics

The OPA2188 is specified for operation from 4 V to 36 V (±2 V to ±18 V). Many of the specifications apply from –40°C to +105°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

8.3.2 EMI Rejection

The OPA2188 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI interference from sources such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx188 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 39 shows the results of this testing on the OPA2188. Detailed information can also be found in the application report *EMI Rejection Ratio of Operational Amplifiers* (SBOA128), available for download from the TI website.

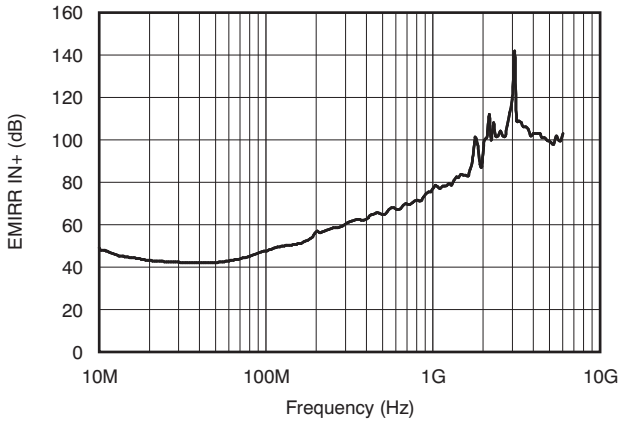


Figure 39. EMIRR Testing

8.3.3 Phase-Reversal Protection

The OPA2188 device has an internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPA2188 input prevents phase reversal with excessive common-mode voltage. Instead, the output limits into the appropriate rail. This performance is shown in Figure 40.

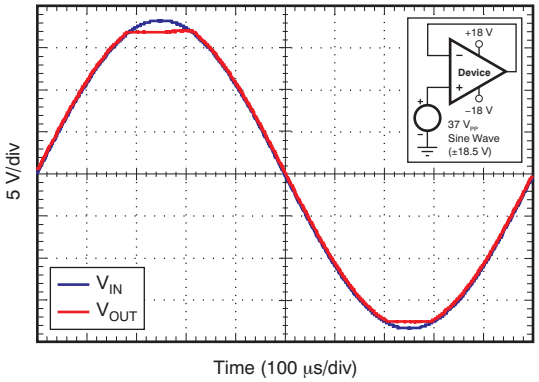


Figure 40. No Phase Reversal

Feature Description (continued)

8.3.4 Capacitive Load and Stability

The dynamic characteristics of the OPA2188 have been optimized for a range of common operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} equal to 50 Ω) in series with the output. Figure 41 and Figure 42 illustrate graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Also, refer to the applications report, *Feedback Plots Define Op Amp AC Performance* (SBOA015), available for download from the TI website, for details of analysis techniques and application circuits.

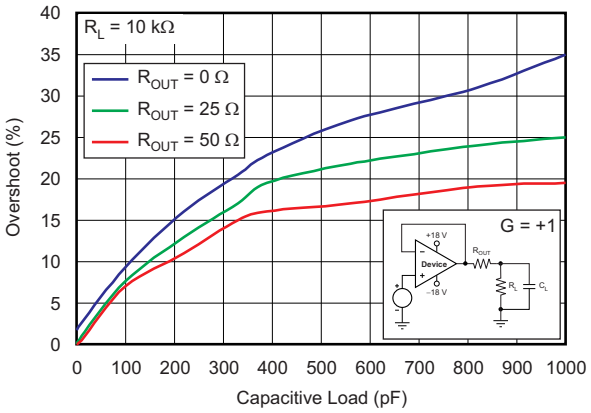


Figure 41. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

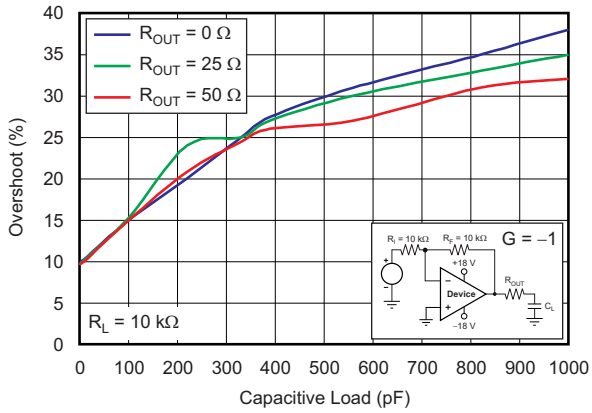


Figure 42. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.3.5 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

These ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. Figure 43 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and its value should be kept to a minimum in noise-sensitive applications.

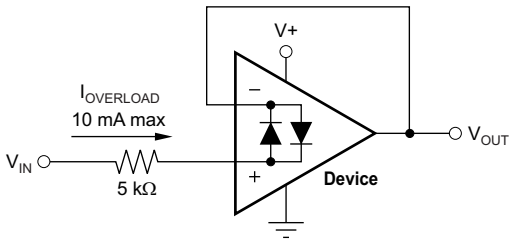


Figure 43. Input Current Protection

Feature Description (continued)

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When the operational amplifier connects into a circuit, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through ESD cells and rarely involves the absorption device.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage must be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.

8.4 Device Functional Modes

The OPA2188 device has a single functional mode. The device is powered on as long as the power supply voltage is between 4 V (±2 V) and 36 V (±18 V).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Applications

9.2.1 High-Side Voltage-to-Current (V-I) Converter

The circuit shown in Figure 44 is a high-side voltage-to-current (V-I) converter. It translates in input voltage of 0 V to 2 V to and output current of 0 mA to 100 mA. Figure 45 shows the measured transfer function for this circuit. The low offset voltage and offset drift of the OPA2188 facilitate excellent dc accuracy for the circuit.

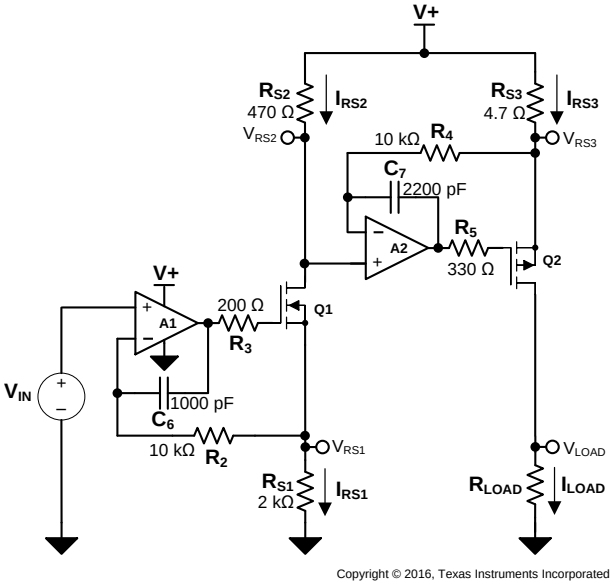


Figure 44. High-Side Voltage-to-Current (V-I) Converter

Typical Applications (continued)

9.2.1.1 Design Requirements

The design requirements are as follows:

- Supply Voltage: 5 V DC
- Input: 0 V to 2 V DC
- Output: 0 mA to 100 mA DC

9.2.1.2 Detailed Design Procedure

The V-I transfer function of the circuit is based on the relationship between the input voltage, V_{IN}, and the three current sensing resistors, R_{S1}, R_{S2}, and R_{S3}. The relationship between V_{IN} and R_{S1} determines the current that flows through the first stage of the design. The current gain from the first stage to the second stage is based on the relationship between R_{S2} and R_{S3}.

For a successful design, pay close attention to the dc characteristics of the operational amplifier chosen for the application. To meet the performance goals, this application benefits from an operational amplifier with low offset voltage, low temperature drift, and rail-to-rail output. The OPA2188 CMOS operational amplifier is a high-precision, ultra-low offset, ultra-low drift amplifier optimized for low-voltage, single-supply operation with an output swing to within 15 mV of the positive rail. The OPA2188 family uses chopping techniques to provide low initial offset voltage and near-zero drift over time and temperature. Low offset voltage and low drift reduce the offset error in the system, making these devices appropriate for precise dc control. The rail-to-rail output stage of the OPA2188 ensures that the output swing of the operational amplifier is able to fully control the gate of the MOSFET devices within the supply rails.

A detailed error analysis, design procedure, and additional measured results are given in TIPD102.

9.2.1.3 Application Curve

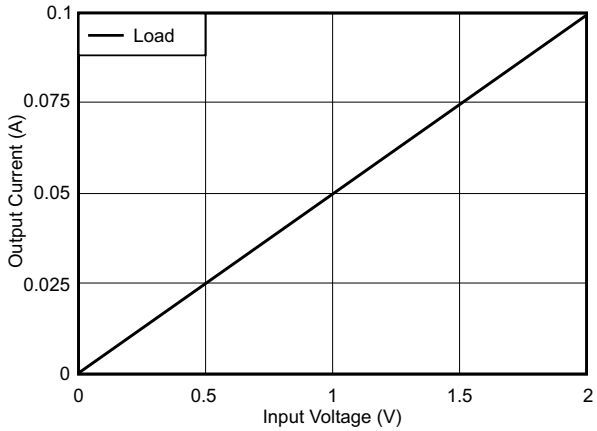


Figure 45. Measured Transfer Function for High-Side V-I Converter

9.3 System Examples

9.3.1 Discrete INA + Attenuation for ADC With 3.3-V Supply

The application examples of Figure 46 and Figure 47 highlight only a few of the circuits where the OPA2188 can be used.

System Examples (continued)

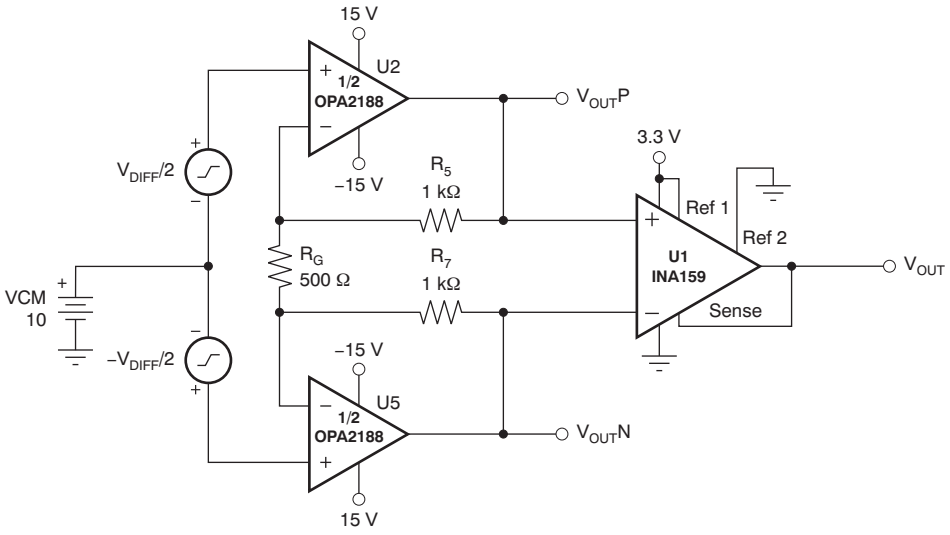
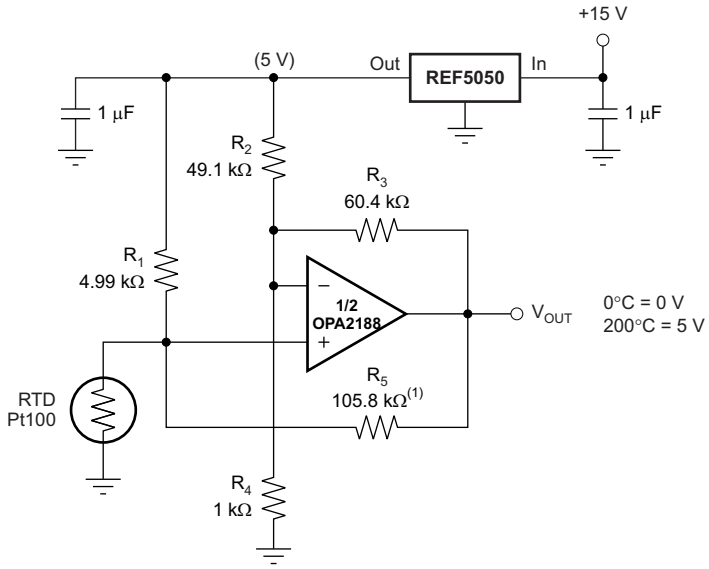


Figure 46. Discrete INA + Attenuation for ADC with 3.3-V Supply

9.3.2 RTD Amplifier with Linearization



(1) R_5 provides positive-varying excitation to linearize output.

Figure 47. RTD Amplifier with Linearization

10 Power Supply Recommendations

The OPA2188 is specified for operation from 4 V to 36 V (±2 V to ±18 V); many specifications apply from –40°C to 105°C. The *Typical Characteristics* presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 40 V can permanently damage the device (see the *Absolute Maximum Ratings*).

TI recommends placing 0.1-μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

Pay attention to good layout practices. Keep traces short and when possible, use a printed-circuit-board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1-μF capacitor closely across the supply pins. Apply these guidelines throughout the analog circuit to improve performance and provide benefits, such as reducing the electromagnetic interference (EMI) susceptibility.

Operational amplifiers vary in susceptibility to radio frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or DC signal levels with changes in the interfering RF signal. The OPA2188 is specifically designed to minimize susceptibility to RFI and demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may still cause varying offset levels.

11.2 Layout Example

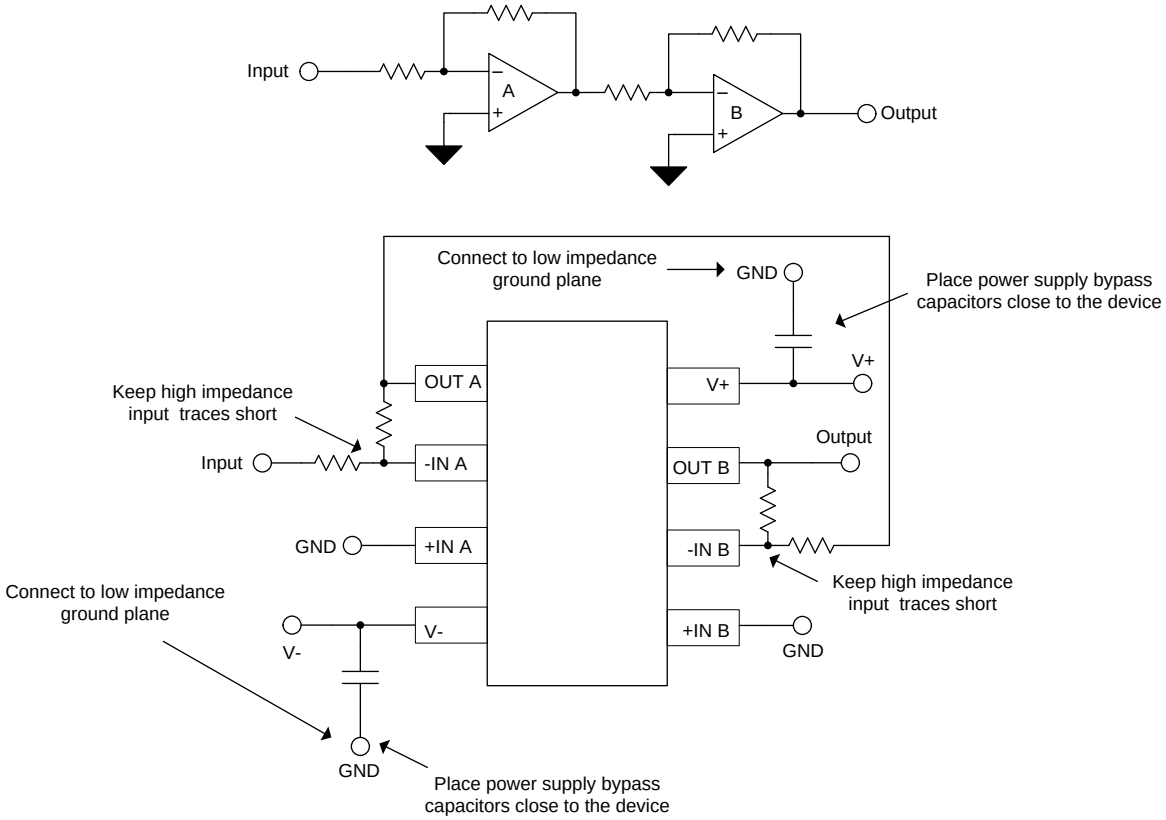


Figure 48. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。 TINA-TI™ 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

12.1.1.2 DIP 适配器 EVM

DIP 适配器 EVM 工具提供了一种简单而低成本的方式来针对小型表面贴装 IC 进行原型设计。评估工具适用于以下 TI 封装：D 或 U (SOIC-8)、PW (TSSOP-8)、DGK (MSOP-8)、DBV（SOT23-6、SOT23-5 和 SOT23-3）、DCK（SC70-6 和 SC70-5）和 DRL (SOT563-6)。DIP 适配器 EVM 也可搭配引脚排使用或直接与现有电路相连。

12.1.1.3 通用运放 EVM

通用运放 EVM 是一系列通用空白电路板，可简化采用各种 IC 封装类型的电路板原型设计。借助评估模块电路板设计，可以轻松快速地构造多种不同电路。共有 5 个模型可供选用，每个模型都对应一种特定封装类型。支持 PDIP、SOIC、MSOP、TSSOP 和 SOT23 封装。

注

这些电路板均为空白电路板，用户必须自行提供 IC。TI 建议您在订购通用运放 EVM 时申请几个运放器件样品。

12.1.1.4 TI 高精度设计

TI 高精度设计是由 TI 公司的高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整 PCB 电路原理图和布局布线、物料清单以及性能测量结果。欲获取 TI 高精度设计，请访问 http://www.ti.com.cn/ww/analog/precision-designs/。

12.1.1.5 WEBENCH® 滤波器设计器

WEBENCH® 滤波器设计器是一款简单、功能强大且便于使用的有源滤波器设计程序。WEBENCH Filter Designer 通过选择 TI 运算放大器以及 TI 供应商合作伙伴的无源组件来构建优化滤波器设计方案。

WEBENCH® 设计中心以基于网络的工具形式提供 WEBENCH® Filter Designer。用户通过该工具可在短时间内完成多级有源滤波器解决方案的设计、优化和仿真。

12.2 文档支持

12.2.1 相关文档

使用 OPA2188 时，建议参考下列相关文档。可从 www.ti.com 下载，除非另外注明。

- *《运算放大器的电磁干扰 (EMI) 抑制比》*。
- *《反馈曲线图定义运算放大器交流性能》*
- *运算放大器性能分析*.
- *运算放大器的单电源操作*

文档支持 (continued)

- *调优放大器*.

12.3 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2188AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)	Samples
OPA2188AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	2188	Samples
OPA2188AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	2188	Samples
OPA2188AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	(2188, OPA2188)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

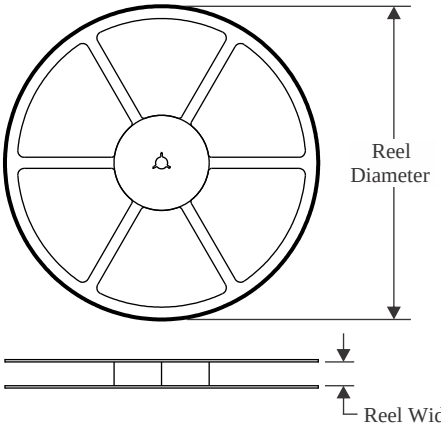
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

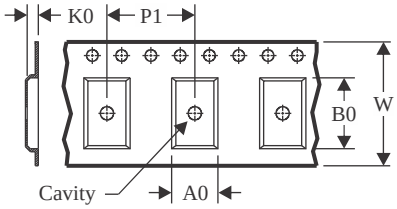
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

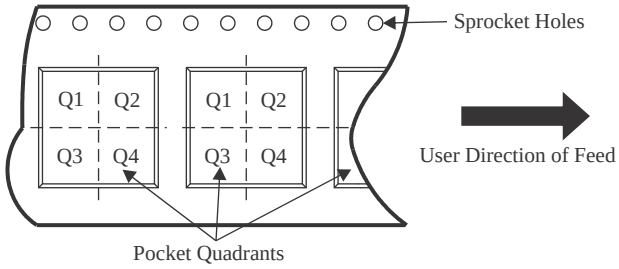


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

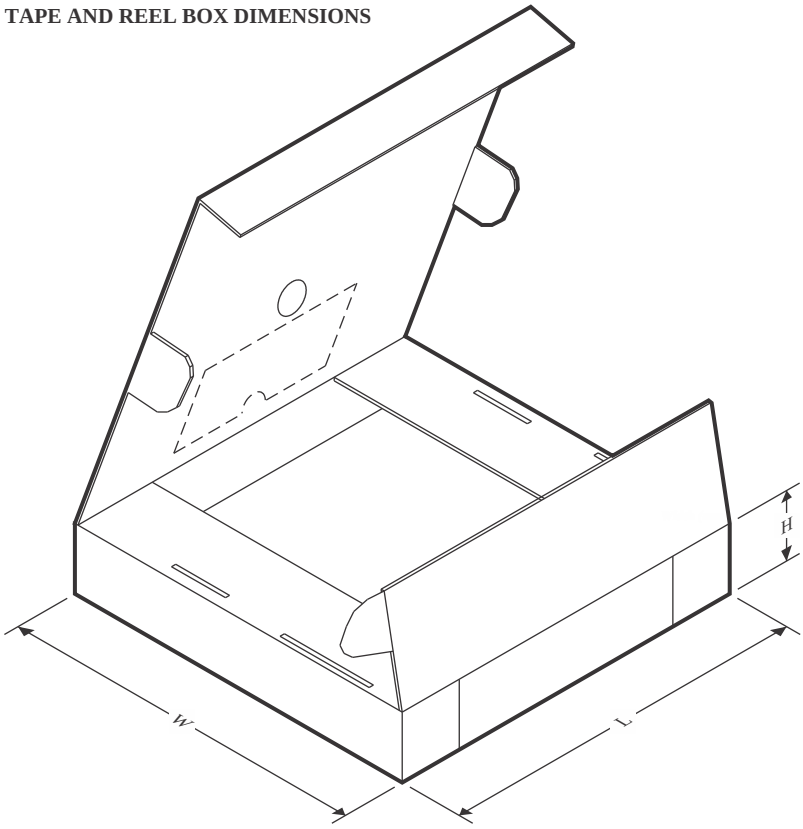
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2188AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2188AIDGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

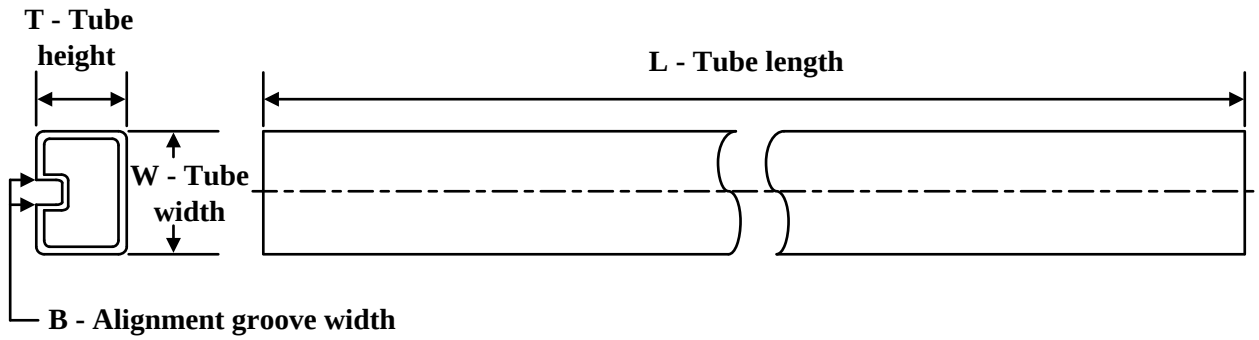
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2188AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2188AIDGKT	VSSOP	DGK	8	250	353.0	353.0	32.0
OPA2188AIDGKT	VSSOP	DGK	8	250	223.0	270.0	35.0

TUBE



*All dimensions are nominal

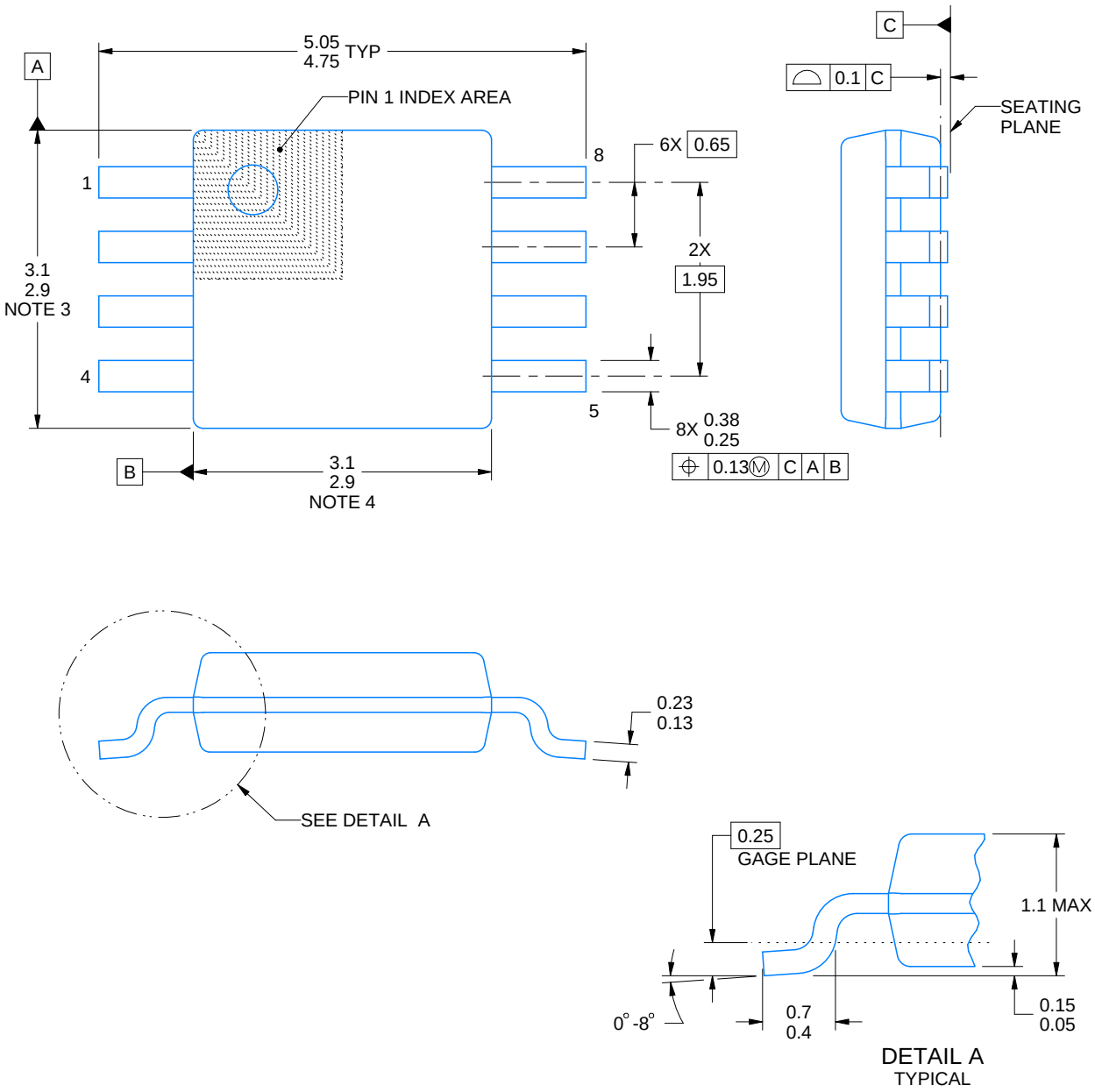
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2188AID	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

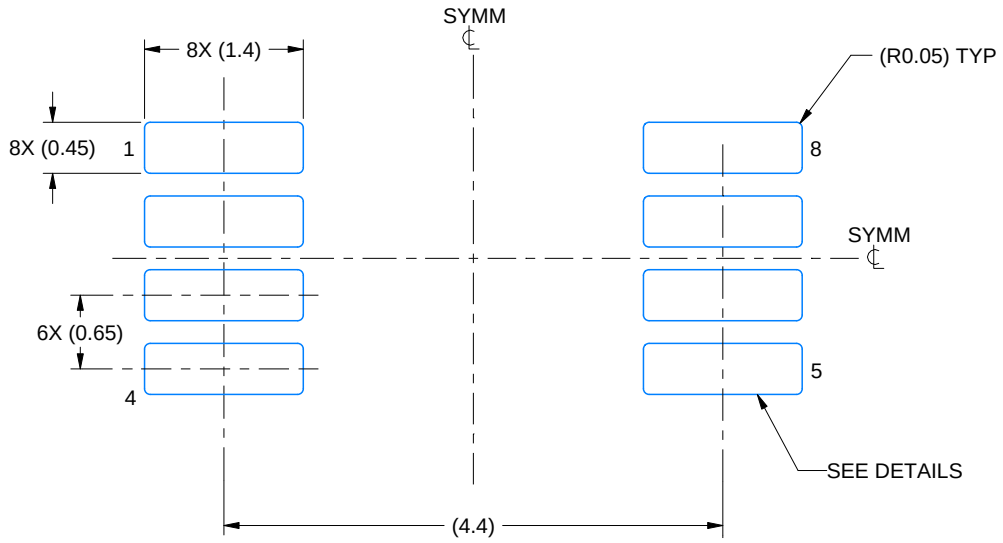
SMALL OUTLINE PACKAGE



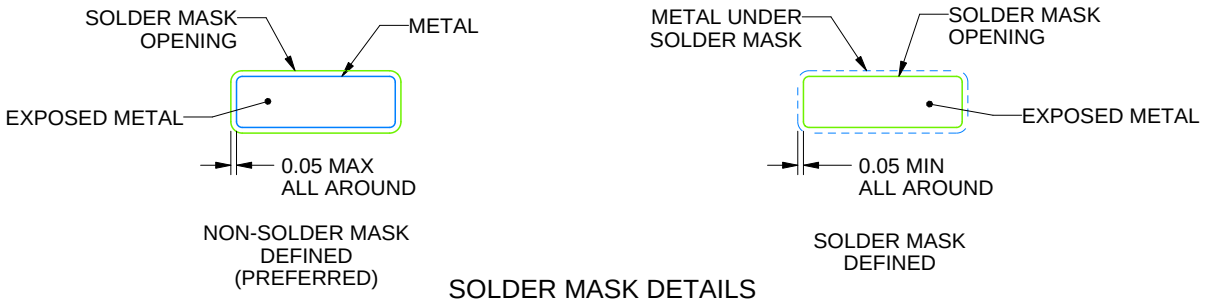
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

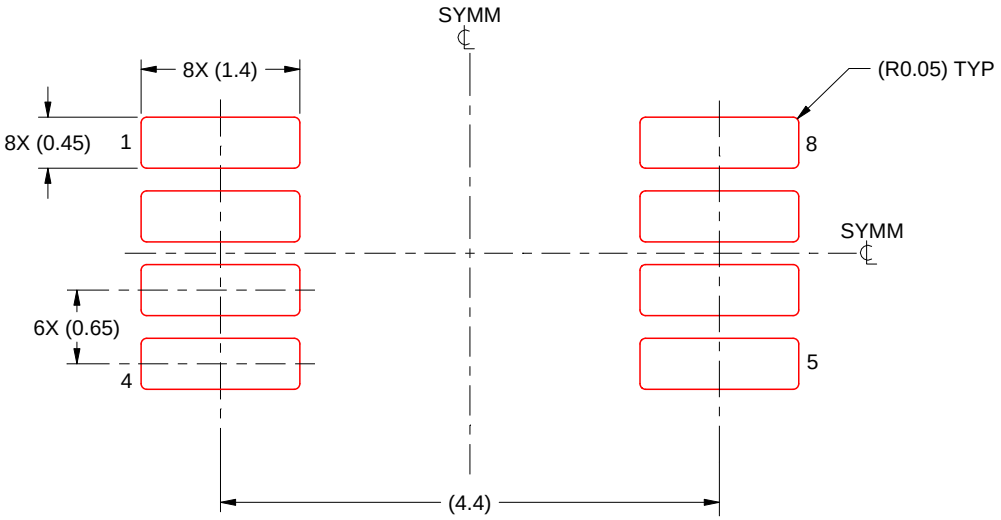


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

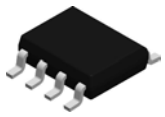


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

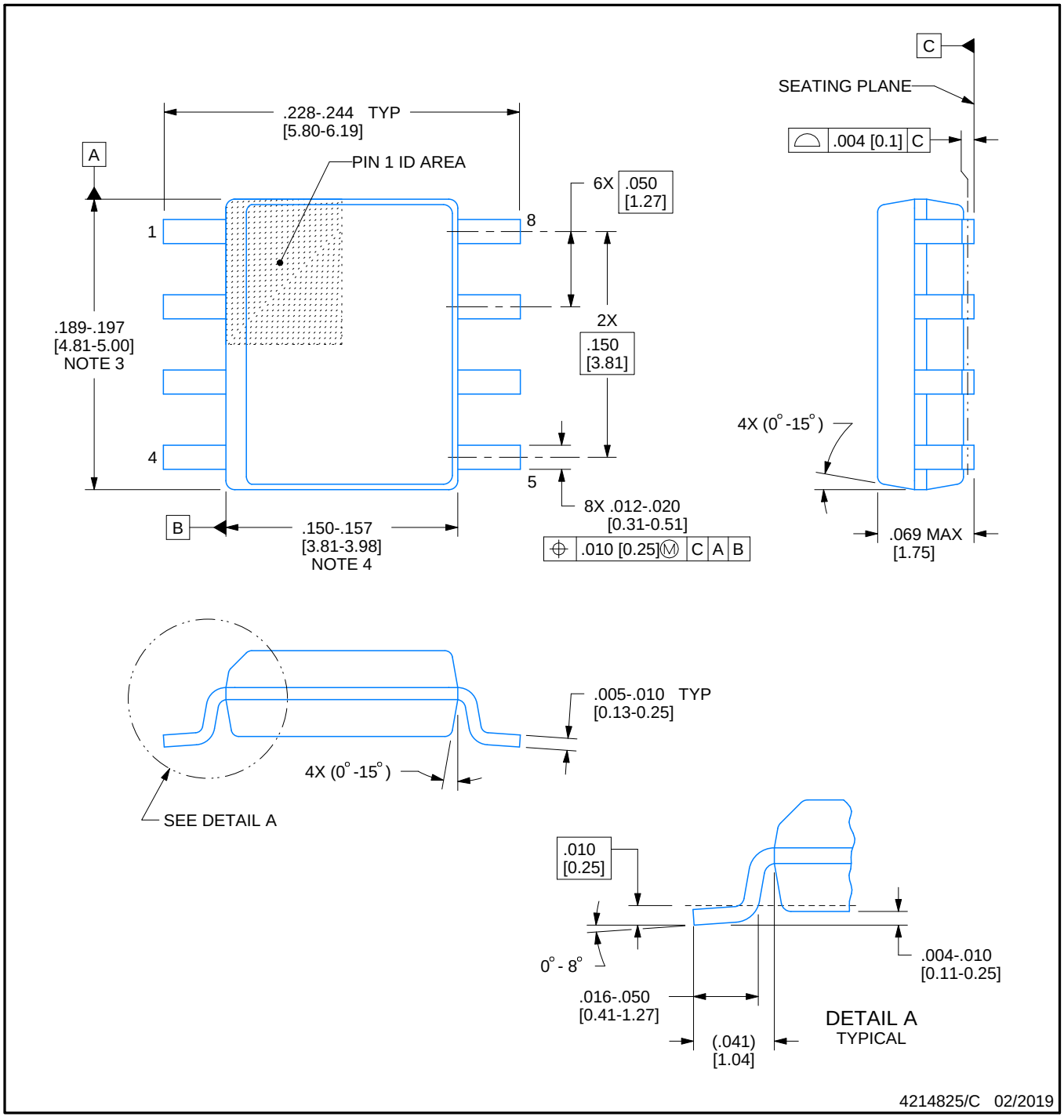


PACKAGE OUTLINE

D0008A

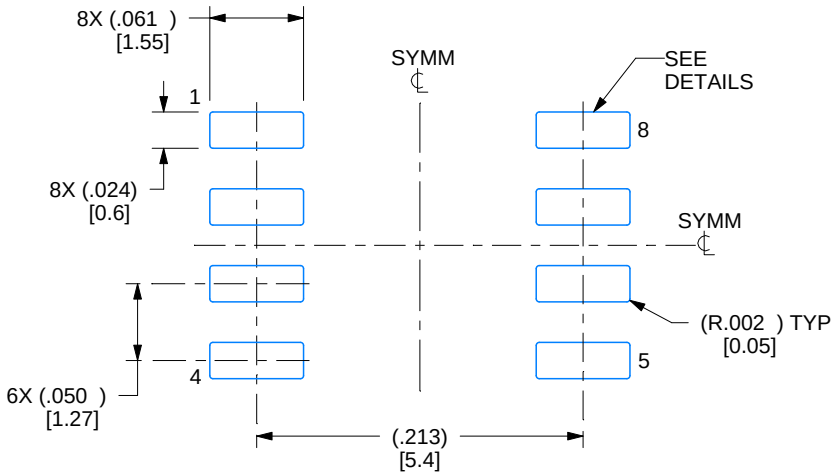
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

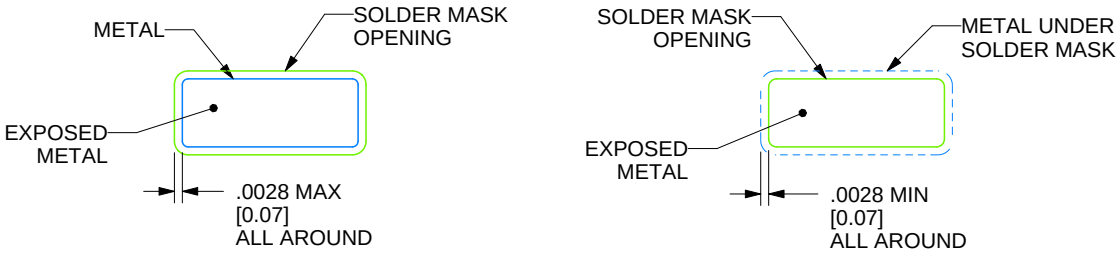


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

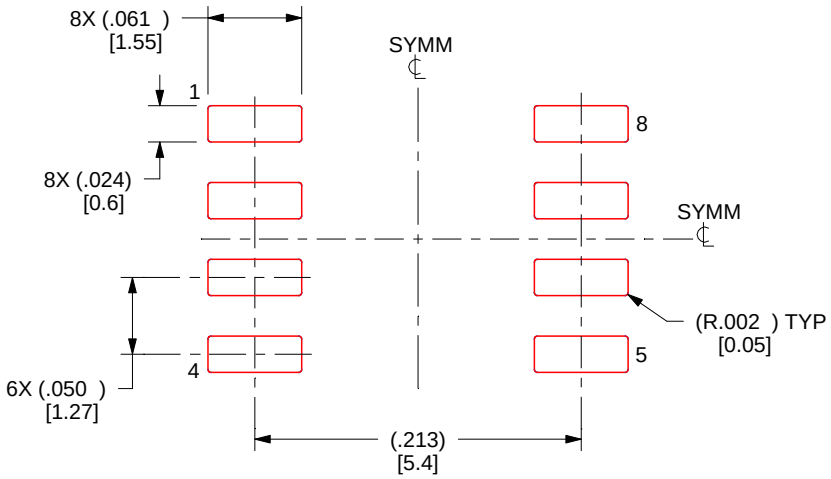
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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