OPAx131 通用 FET 输入运算放大器

1 特性

- FET 输入：I_B = 50pA（最大值）
- 低失调电压：最大 750μV
- 宽电源电压范围：±4.5V 至 ±18V
- 压摆率：10V/μs
- 高带宽：4MHz
- 出色的容性负载驱动
- 单通道、双通道、四通道版本

2 应用

- 数据采集 (DAQ)
- 流量变送器
- 实验室和现场仪表
- 心电图 (ECG)

3 说明

OPAx131 系列 FET 输入运算放大器以低成本提供高性能。OPA131 单通道、OPA2131 双通道和 OPA4131 四通道版本采用业界通用引脚排列，可提供具有成本效益的设计选项。

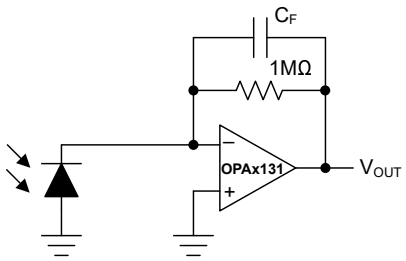
OPAx131 系列提供出色的通用性能，包括低失调电压、偏移和良好的动态特性。

单通道和双通道版本采用 8 引脚 SOIC 表面贴装封装。四通道版本采用 14 引脚和 16 引脚 SOIC 表面贴装封装以及 14 引脚 PDIP 封装。

器件信息

器件型号	通道数	封装(1)
OPA131	单通道	D（SOIC，8）
OPA2131	双通道	D（SOIC，8）
OPA4131	四通道	D（SOIC，14）
		DW（SOIC，16）
		N（PDIP，14）

(1) 有关更多信息，请参阅节 9。



简化版跨阻放大器

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4 Pin Configuration and Functions

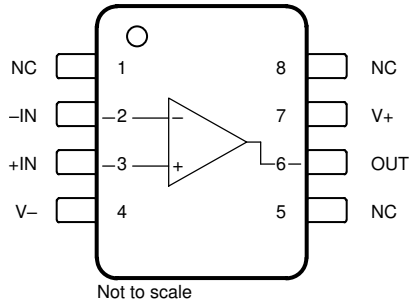


图 4-1. OPA131 D Package, 8-Pin SOIC (Top View)

表 4-1. Pin Functions: OPA131

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input, channel A
– IN	2	Input	Inverting input, channel A
NC	1, 5	—	Do not connect these pins(1)
NC	8	—	No internal connection. Float this pin.
OUT	6	Output	Output
V+	7	Power	Positive (highest) power supply
V –	4	Power	Negative (lowest) power supply

(1) Existing layouts for the OPA131 D package before revision B of this data sheet do not need to be redesigned.

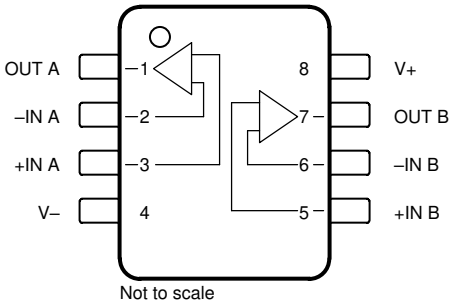


图 4-2. OPA2131 D Package, 8-Pin SOIC (Top View)

表 4-2. Pin Functions: OPA2131

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
– IN A	2	Input	Inverting input, channel A
– IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	Power	Positive (highest) power supply
V –	4	Power	Negative (lowest) power supply

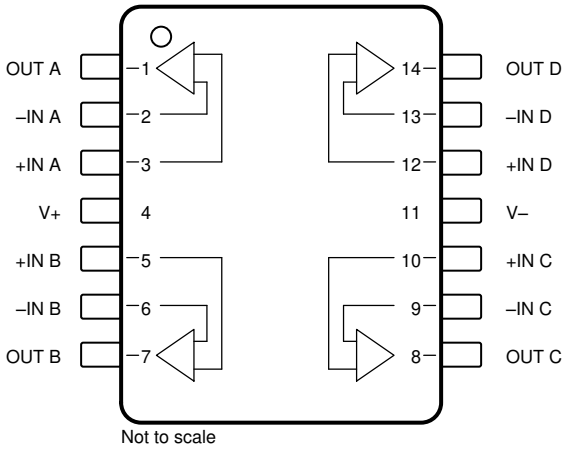


图 4-3. OPA4131 D Package, 14-Pin SOIC, and N Package, 14-Pin PDIP (Top View)

表 4-3. Pin Functions: OPA4131 D and N packages

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	9	Input	Inverting input, channel C
–IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V –	11	Power	Negative (lowest) power supply

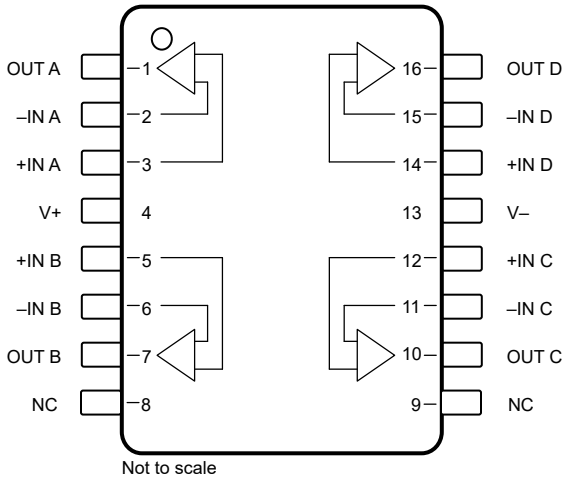


图 4-4. OPA4131 DW Package, 16-Pin SOIC (Top View)

表 4-4. Pin Functions: OPA4131 DW Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	12	Input	Noninverting input, channel C
+IN D	14	Input	Noninverting input, channel D
–IN A	2	Input	Inverting input, channel A
–IN B	6	Input	Inverting input, channel B
–IN C	11	Input	Inverting input, channel C
–IN D	15	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	10	Output	Output, channel C
OUT D	16	Output	Output, channel D
V+	4	Power	Positive (highest) power supply
V–	13	Power	Negative (lowest) power supply
NC	8, 9	—	No internal connection. Float this pin.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply		±18	V
		Single supply		36	
	Input voltage(2)		(V–) – 0.5	(V+) + 0.5	V
	Input current(2)			±10	mA
I_{SC}	Output short-circuit(3)		Continuous		
T_A	Operating temperature		–55	125	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–55	125	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails must be current limited to 10mA or less.
(3) Short-circuit to ground, one amplifier per package.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_S	Supply voltage, (V+) – (V–)	Dual supply	±4.5	±15	±18	V
		Single supply	9	30	36	
T_A	Ambient temperature		–40		+85	°C

5.3 Thermal Information - OPA131

THERMAL METRIC(1)		OPA131 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.4 Thermal Information - OPA2131

THERMAL METRIC(1)		OPA2131 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	62.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Thermal Information - OPA4131

THERMAL METRIC(1)		OPA4131 D (SOIC) 14 PINS	OPA4131 DW (SOIC) 16 PINS	OPA4131 N (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	110	80	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56	N/A	N/A	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	53	N/A	N/A	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19	N/A	N/A	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	46	N/A	N/A	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	OPAx131UA			±0.2	±1	mV
		OPA2131U, OPA4131U			±0.2	±1.5	
		OPA131U			±0.2	±0.75	
dV_{OS}/dT	Input offset voltage drift	T_A = – 40°C to +85°C			±2	±10	µV/°C
PSRR	Power-supply rejection ratio	9V ≤ V_S ≤ 36V	OPAx131UA, OPA2131U, OPA4131U		±50	±200	µV/V
			OPA131U		±50	±100	
INPUT BIAS CURRENT							
I_B	Input bias current(1)				±5	±50	pA
		T_A = – 40°C to +85°C			See *Typical Characteristics*		
I_{OS}	Input offset current(1)				±1	±50	pA
NOISE							
e_n	Input voltage noise density	f = 10Hz			21		nV/√Hz
		f = 100Hz			16		
		f = 1kHz			15		
		f = 10kHz			15		
I_n	Input current noise density	f = 1kHz			3		fA/√Hz
INPUT VOLTAGE							
V_{CM}	Common-mode voltage			(V –) + 3		(V+) – 3.5	V
CMRR	Common-mode rejection ratio	– 12V ≤ V_{CM} ≤ 11.5V	OPAx131UA, OPA2131U, OPA4131U	70	80		dB
			OPA131U	80	86		
INPUT IMPEDANCE							
	Differential				10^{10} || 5		Ω || pF
	Common-mode	– 13V ≤ V_{CM} ≤ 11.5V			10^{12} || 4.3		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	– 12V ≤ V_O ≤ 12V	OPAx131UA, OPA2131U, OPA4131U	94	110		dB
			OPA131U	100	110		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product				4		MHz
SR	Slew rate				10		V/µs
	Settling time	10V step, G = 1	0.1%		1.5		µs
			0.01%		2		
THD+N	Total harmonic distortion plus noise	f = 1kHz, G = 1, V_O = 3.5V_{rms}			0.0008%		
OUTPUT							
V_O	Voltage output	R_L = 2kΩ	Positive	(V+) – 3	(V+) – 2.5		V
			Negative		(V –) + 2.5	(V –) + 3	
I_{SC}	Short-circuit current				±20		mA
POWER SUPPLY							
I_Q	Quiescent current (per amplifier)	I_O = 0mA	OPAx131UA		±1.5	±1.75	mA
			OPAx131U		±1.5	±2	

(1) High-speed test at T_J = 25°C.

5.7 Typical Characteristics

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

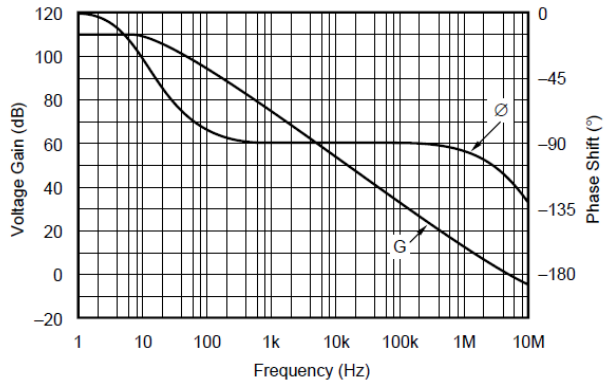


图 5-1. Open-Loop Gain and Phase vs Frequency

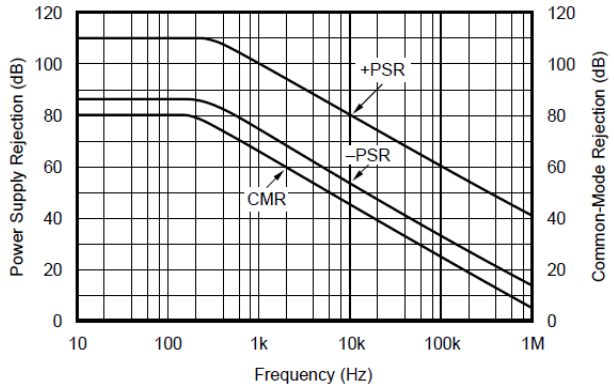


图 5-2. Power Supply and Common-Mode Rejection vs Frequency

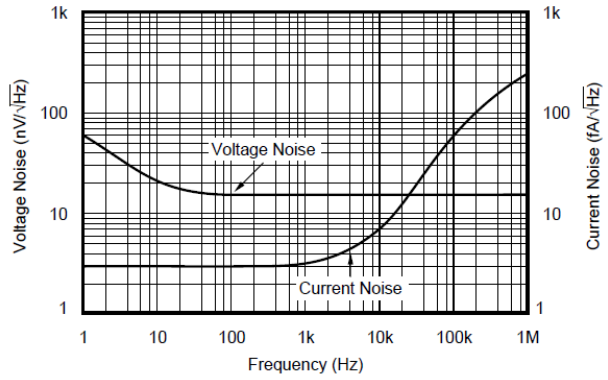


图 5-3. Input Voltage and Current Noise Spectral Density vs Frequency

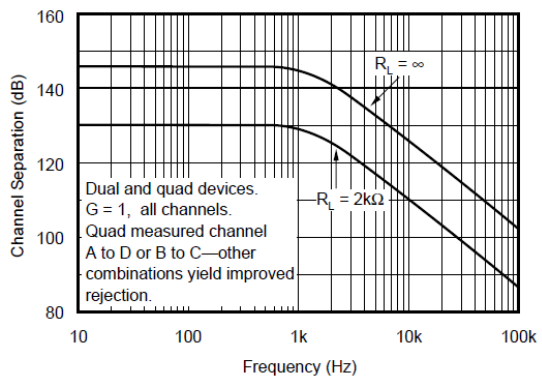


图 5-4. Channel Separation vs Frequency

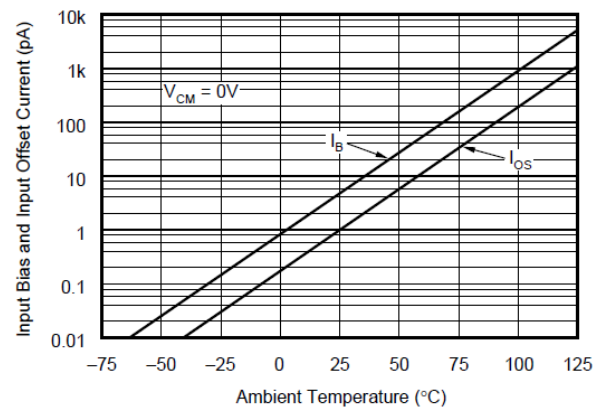


图 5-5. Input Bias and Input Offset Current vs Temperature

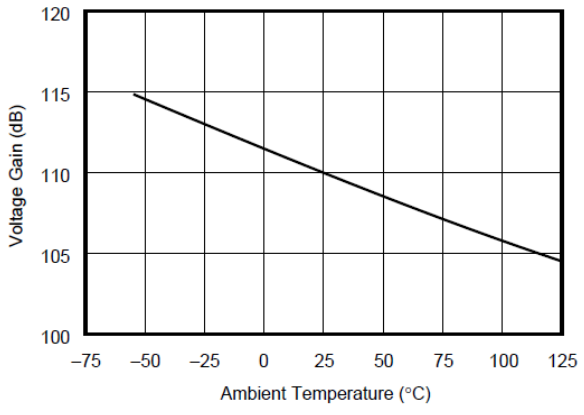


图 5-6. Open-Loop Gain vs Temperature

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

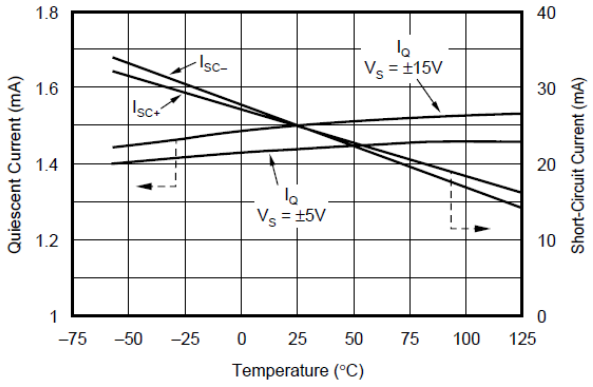


图 5-7. Quiescent Current and Short-Circuit Current vs Temperature

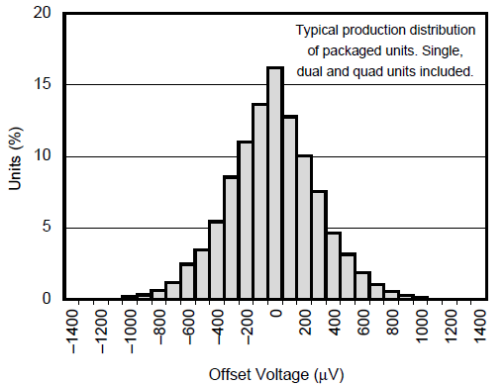


图 5-8. Offset Voltage Production Distribution

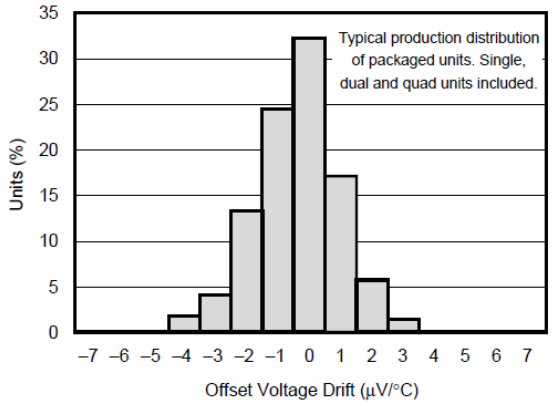


图 5-9. Offset Voltage Drift Production Distribution

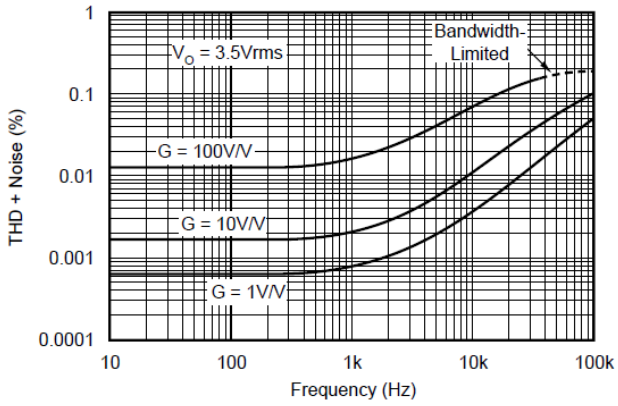


图 5-10. Total Harmonic Distortion + Noise vs Frequency

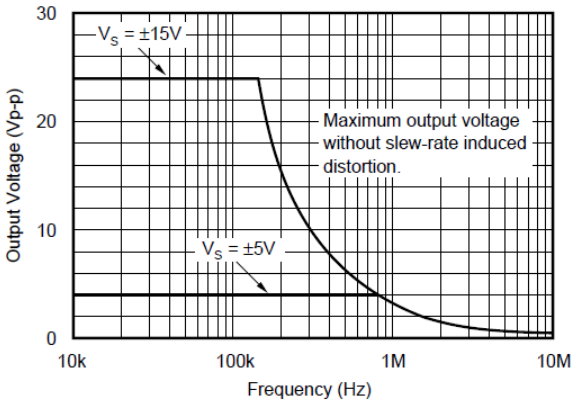


图 5-11. Maximum Output Voltage vs Frequency

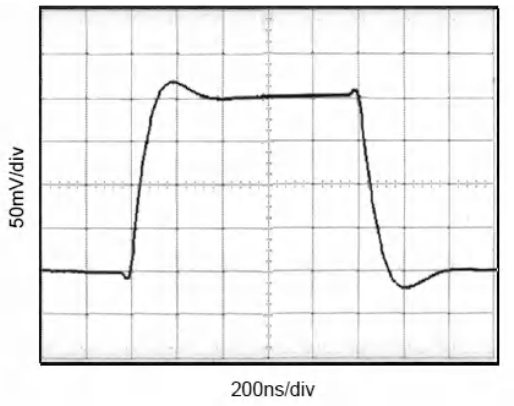


图 5-12. Small-Signal Step Response G = 1, C_L = 300pF

5.7 Typical Characteristics (continued)

at T_A = 25°C, V_S = ±15V, R_L = 10kΩ connected to midsupply, and V_{CM} = V_{OUT} = midsupply (unless otherwise noted)

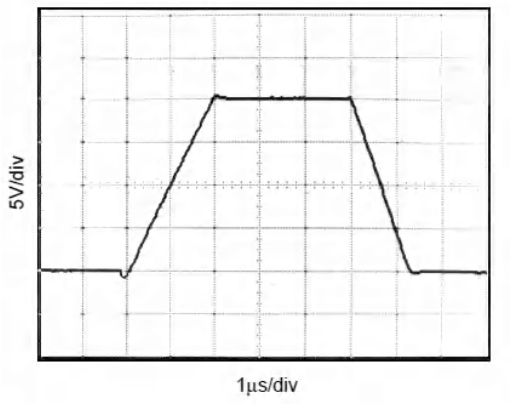


图 5-13. Large-Signal Step Response G = 1, C_L = 300pF

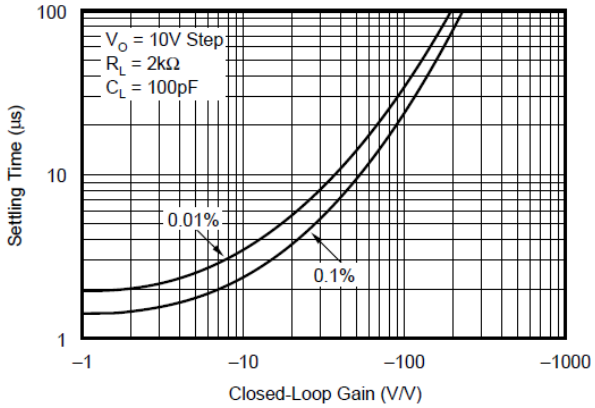


图 5-14. Settling Time vs Closed-Loop Gain

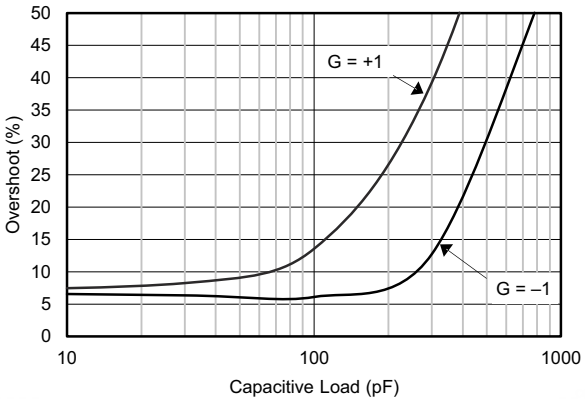


图 5-15. Small-Signal Overshoot vs Load Capacitance

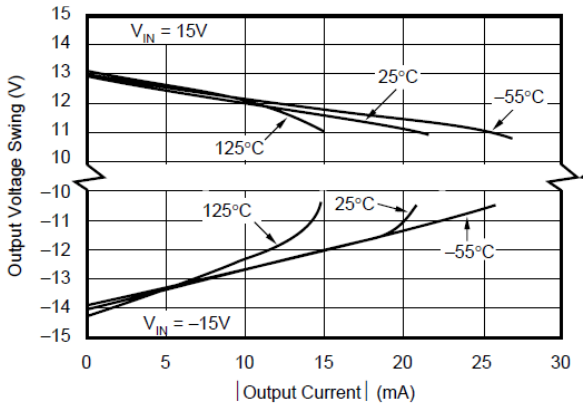


图 5-16. Output Voltage Swing vs Output Current

6 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

6.1 Application Information

The OPAx131 series op amps are unity-gain stable and an excellent choice for a wide range of general-purpose applications. Bypass power-supply pins with 10nF ceramic capacitors or larger.

The OPAx131 series op amps are free from unexpected output phase-reversal common with FET op amps. Many FET-input op amps exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control-loop applications. All circuitry is completely independent in dual and quad versions, and normal behavior can be expected when one amplifier in a package is overdriven or short-circuited.

6.1.1 Offset Voltage Trim

The offset voltage of the OPAx131 amplifiers is laser trimmed and usually requires no user adjustment. The OPAx131 provide less than ±1mV of input offset voltage and less than 10µV/°C of input offset voltage drift over the operating temperature range.

6.2 Typical Application

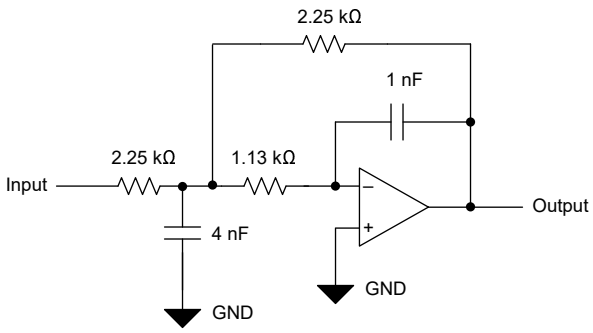


图 6-1. Second-Order Low-Pass Filter

6.2.1 Input Bias Current

The input bias current is approximately 5pA at room temperature and increases with temperature (see also 图 5-5). Input bias current also varies with common-mode voltage and power-supply voltage. This variation depends on the voltage between the negative power supply and the common-mode input voltage.

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

8 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (December 2002) to Revision B (July 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 添加了*器件信息* 表和*应用*、*引脚配置和功能*、*规格*、*建议运行条件*、*热性能信息*、*应用和实施*、*典型应用*、*器件和文档支持* 以及*机械*、*封装和可订购信息* 部分	1
• 更新了*说明*	1
• Deleted obsolete PDIP packages for OPA131 and OPA2131	3
• Updated input voltage in *Absolute Maximum Ratings*	6
• Added input current and related footnote to *Absolute Maximum Ratings*	6
• Changed format of *Electrical Characteristics* to latest standard	8
• Updated nominal conditions in the header of *Electrical Characteristics*	8
• Deleted channel separation specification	8
• Updated common-mode voltage MAX value	8
• Updated common-mode rejection ratio and common-mode input impedance test conditions	8
• Changed differential input impedance from $10^{10}\Omega$ || 1pF to $10^{10}\Omega$ || 5pF	8
• Changed common-mode input impedance from $10^{10}\Omega$ || 3pF to $10^{10}\Omega$ || 4.3pF	8
• Updated open loop voltage gain MIN and TYP values for R_L = 10kΩ and R_L = 2kΩ	8
• Updated settling time test condition	8
• Moved voltage output negative MIN values to MAX values	8
• Deleted note 1 from *Electrical Characteristics*	8

- Updated Figure 5-15, *Small-Signal Overshoot vs Load Capacitance* 9
- Updated text in *Offset Voltage Trim* 12
- Changed Figure 1, OPA130 Offset Voltage Trim Circuit, to Figure 6-1, Second-Order Low-Pass Filter..... 12
- Updated *Input Bias Current* description..... 12

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA131U	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131U, OPA) 131U	Samples
OPA131UA	ACTIVE	SOIC	D	8	75	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131U, OPA) 131U A	Samples
OPA131UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	Call TI | NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131U, OPA) 131U A	Samples
OPA131UJ	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131UJ, OPA) 131UJ	Samples
OPA131UJ/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	(O131UJ, OPA) 131UJ	Samples
OPA2131UA	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	(2131UA, OPA)	Samples
OPA2131UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	(2131UA, OPA)	Samples
OPA2131UJ	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		(2131UJ, OPA)	Samples
OPA2131UJ/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		(2131UJ, OPA)	Samples
OPA4131NA	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131NA	Samples
OPA4131NJ	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131NJ	Samples
OPA4131PA	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4131PA	Samples
OPA4131PAG4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4131PA	Samples
OPA4131PJ	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	OPA4131PJ	Samples
OPA4131UA	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131UA	Samples
OPA4131UA/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4131UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

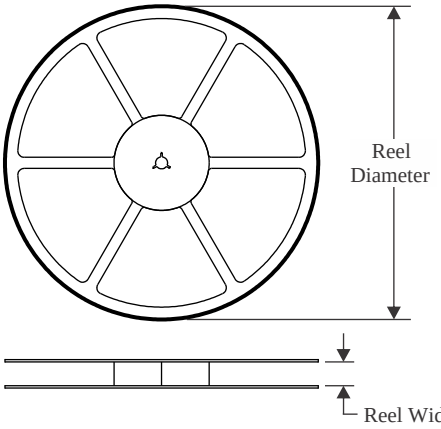
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

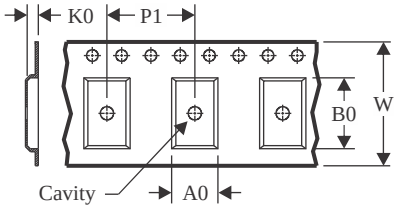
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

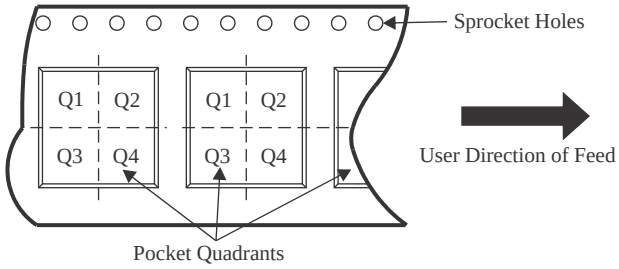


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

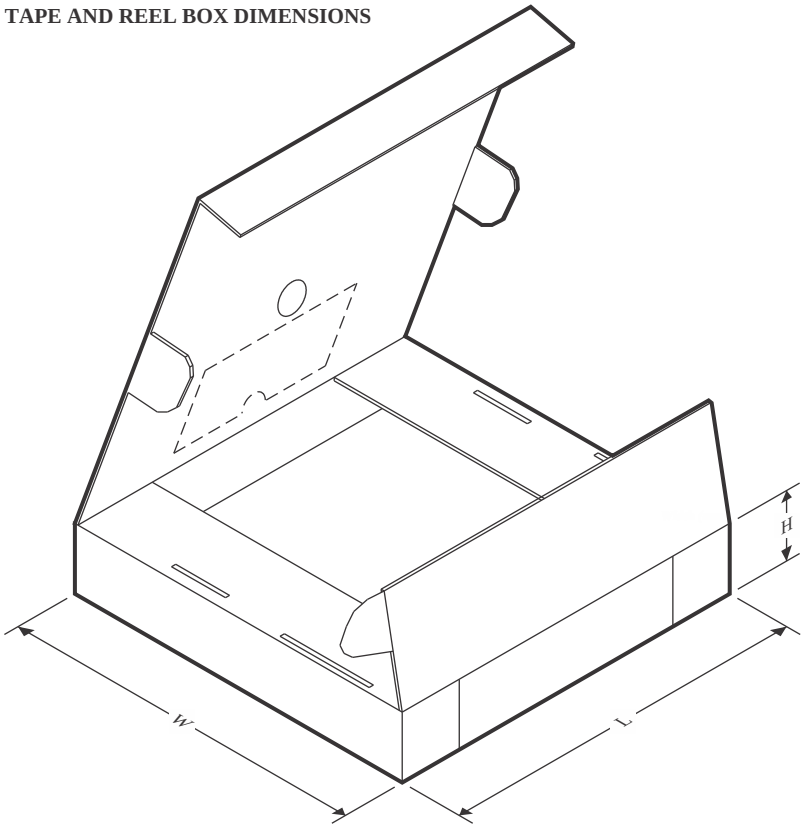
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2131UJ/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4131UA/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

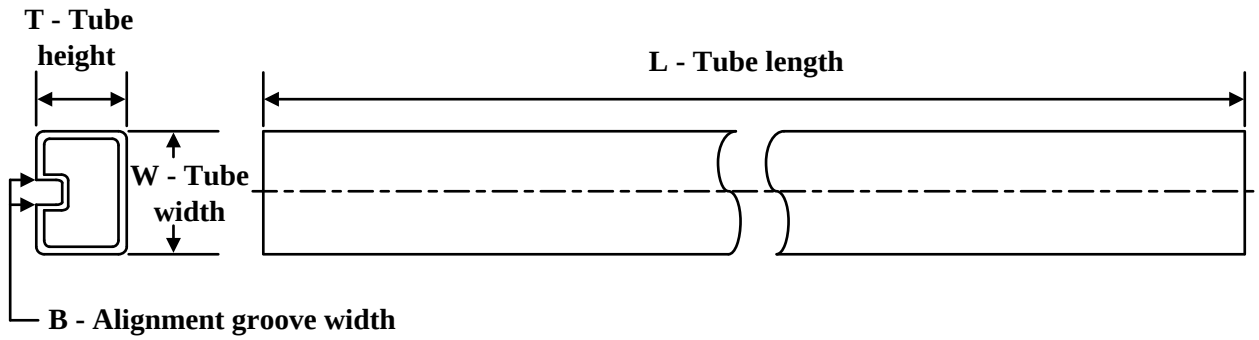
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA131UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA131UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA131UJ/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA131UJ/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2131UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2131UA/2K5	SOIC	D	8	2500	353.0	353.0	32.0
OPA2131UJ/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA2131UJ/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4131UA/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA131U	D	SOIC	8	75	506.6	8	3940	4.32
OPA131UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA131UJ	D	SOIC	8	75	506.6	8	3940	4.32
OPA2131UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2131UJ	D	SOIC	8	75	506.6	8	3940	4.32
OPA4131NA	D	SOIC	14	50	506.6	8	3940	4.32
OPA4131NJ	D	SOIC	14	50	506.6	8	3940	4.32
OPA4131PA	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131PAG4	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131PJ	N	PDIP	14	25	506	13.97	11230	4.32
OPA4131UA	DW	SOIC	16	40	507	12.83	5080	6.6

GENERIC PACKAGE VIEW

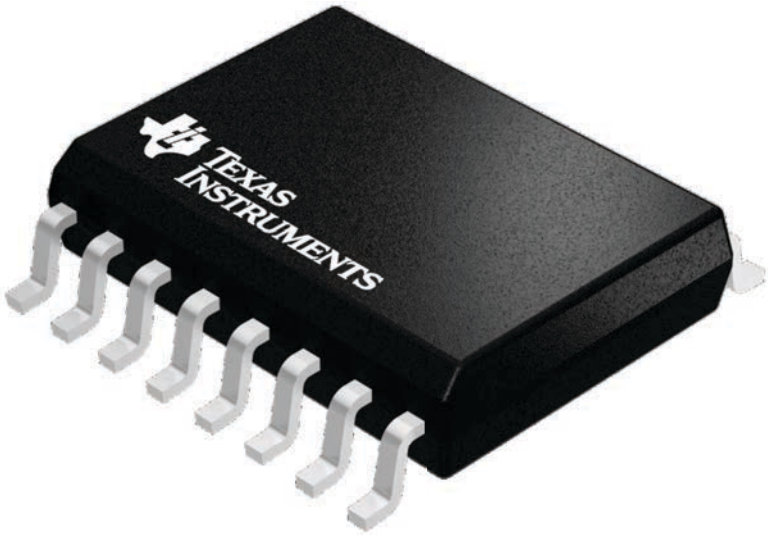
DW 16

SOIC - 2.65 mm max height

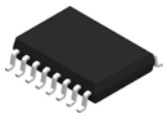
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

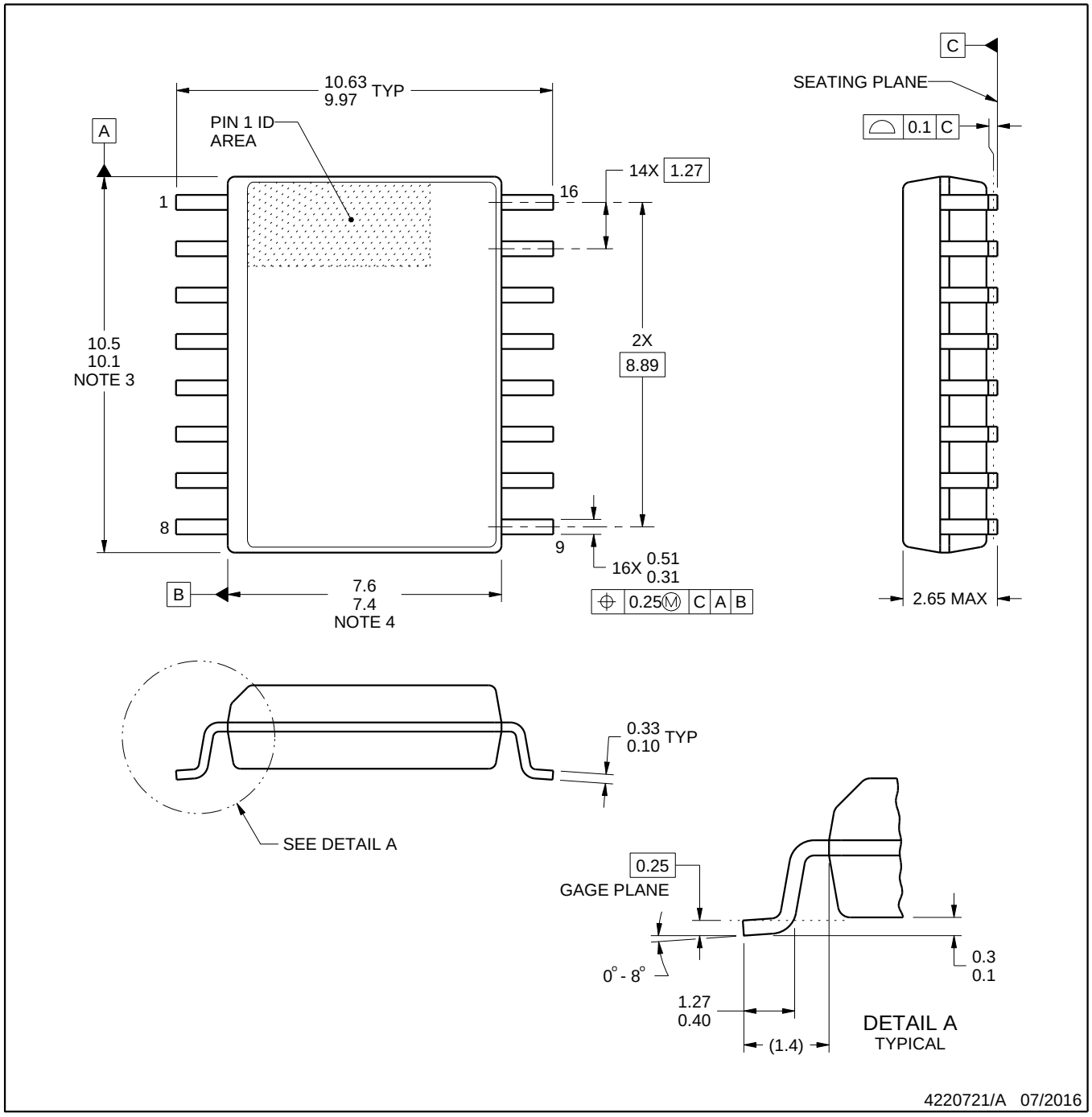


PACKAGE OUTLINE

DW0016A

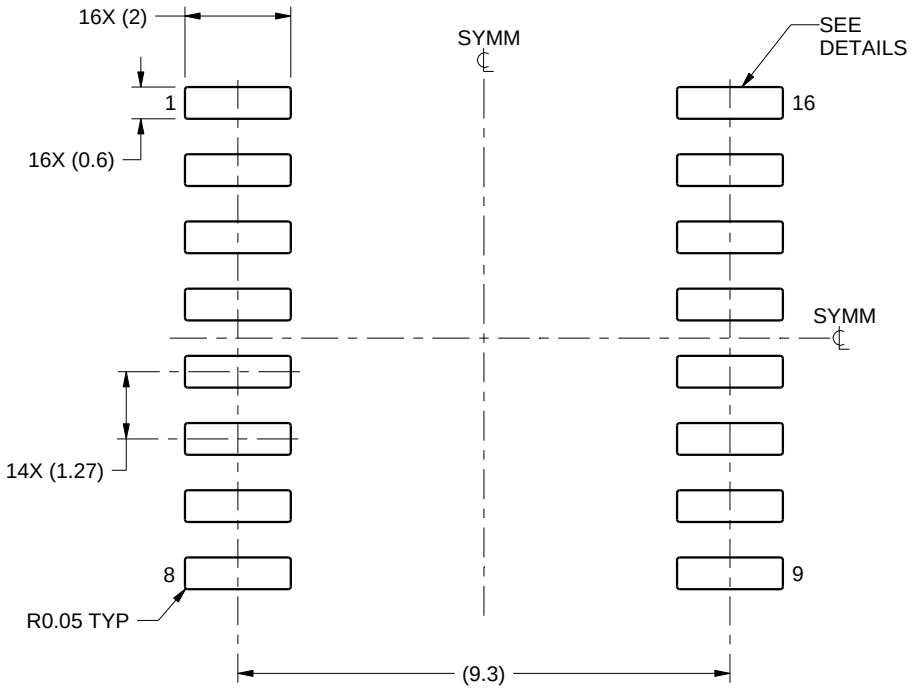
SOIC - 2.65 mm max height

SOIC

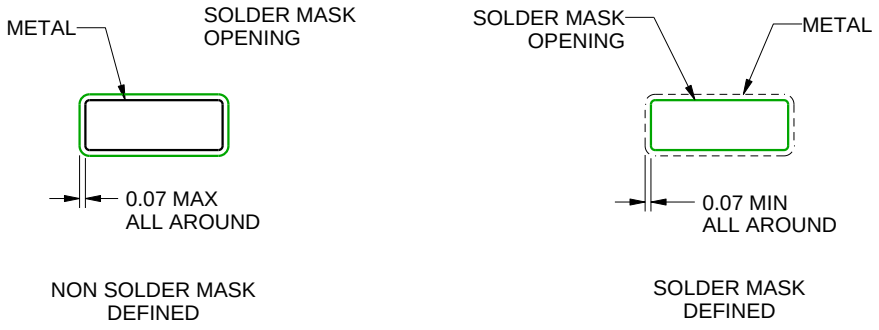


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

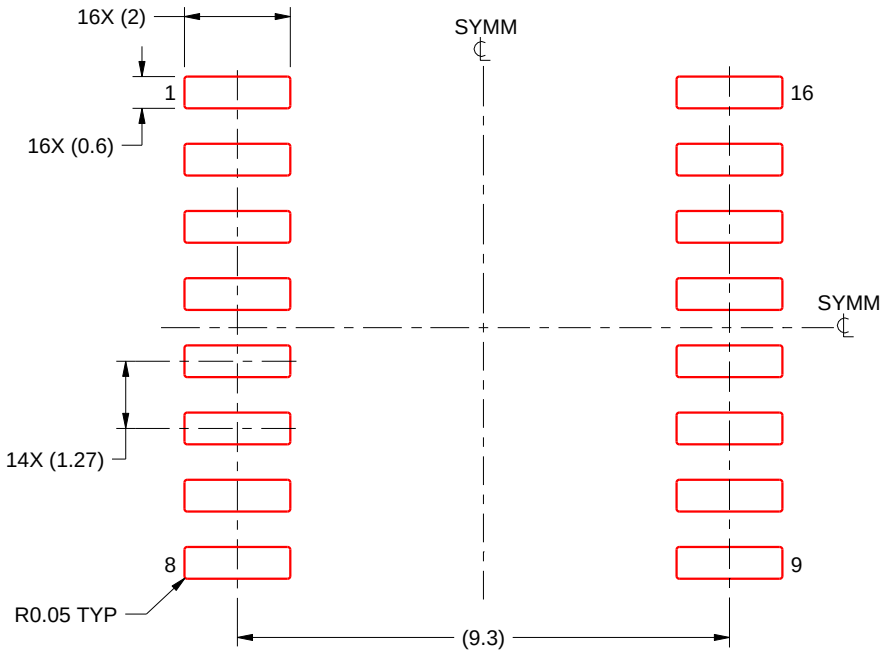


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

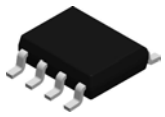


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

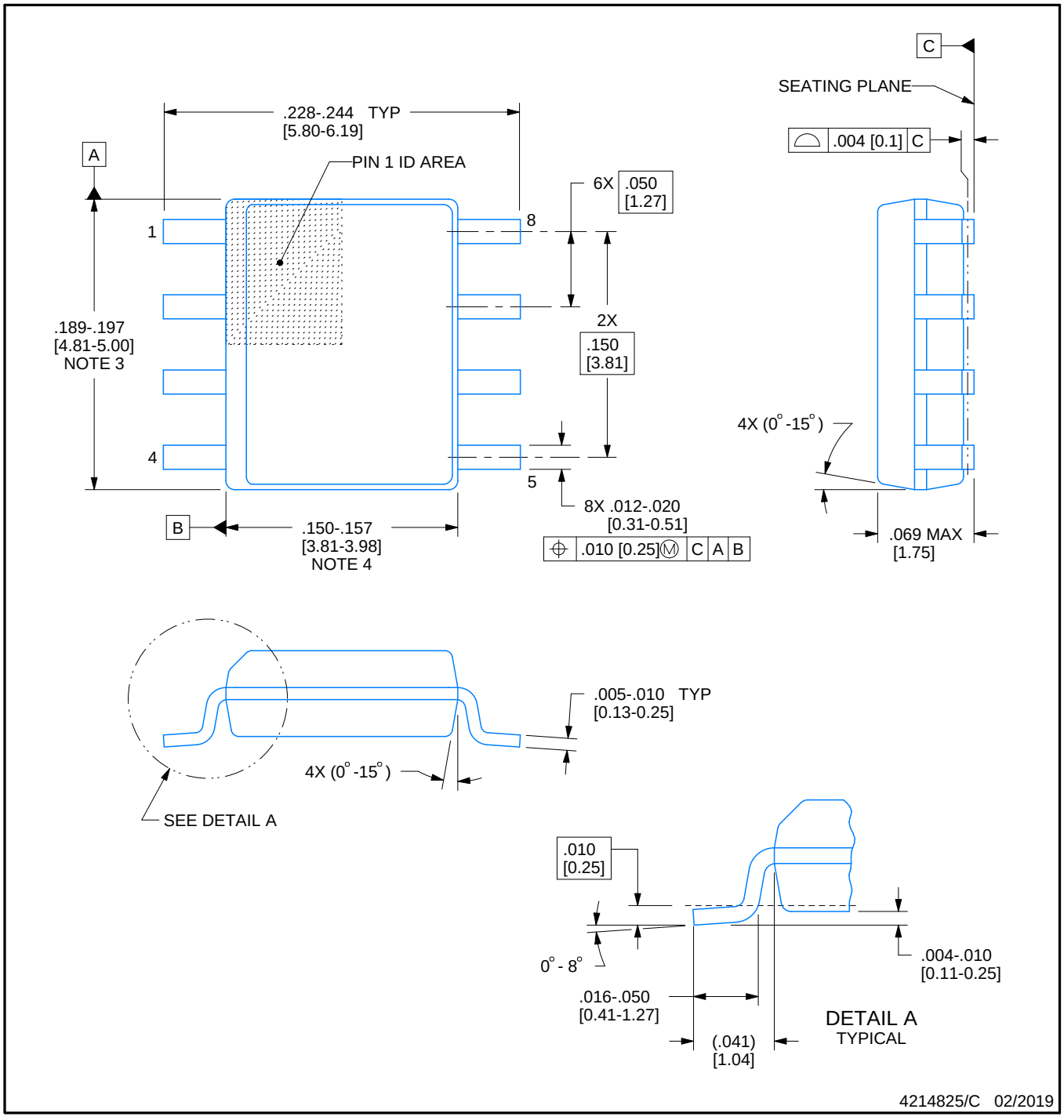


PACKAGE OUTLINE

D0008A

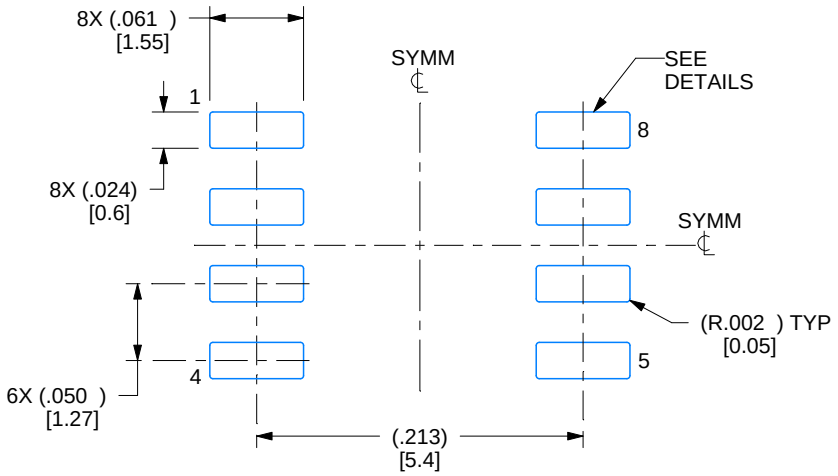
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

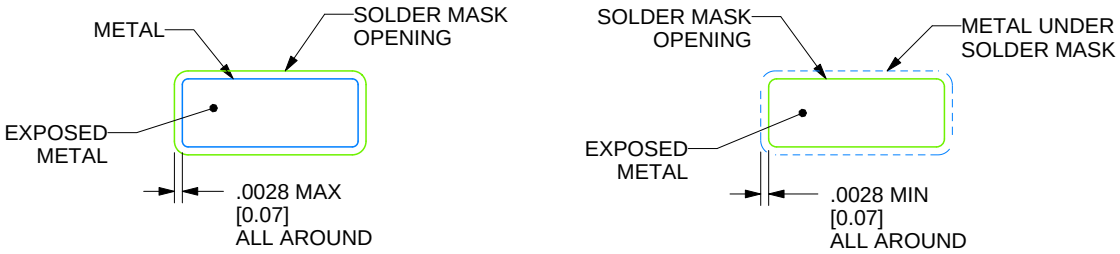


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

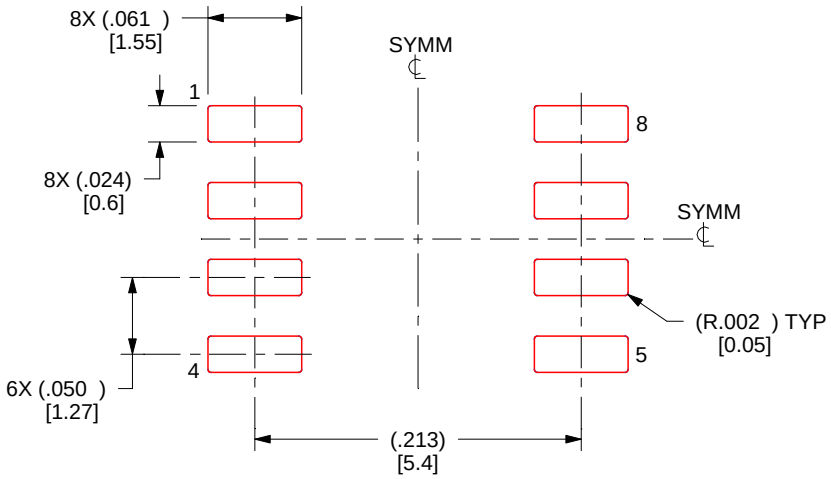
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

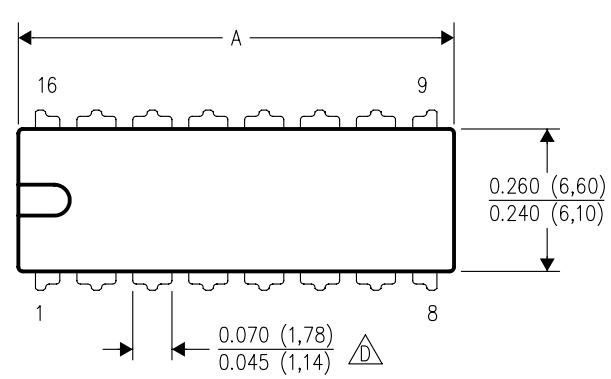
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

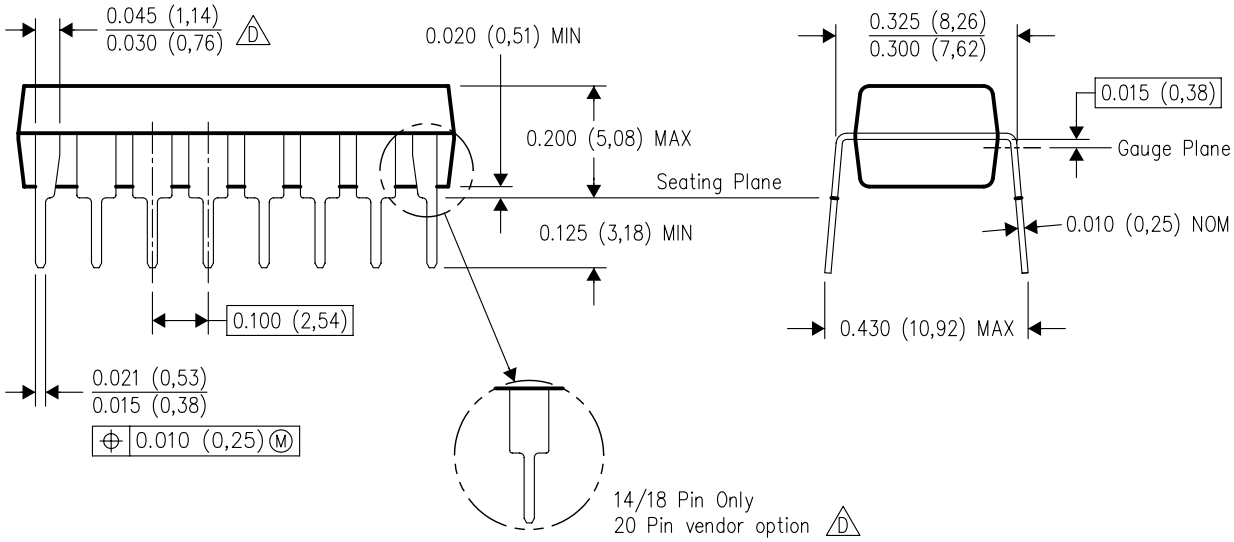
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

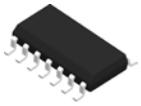


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

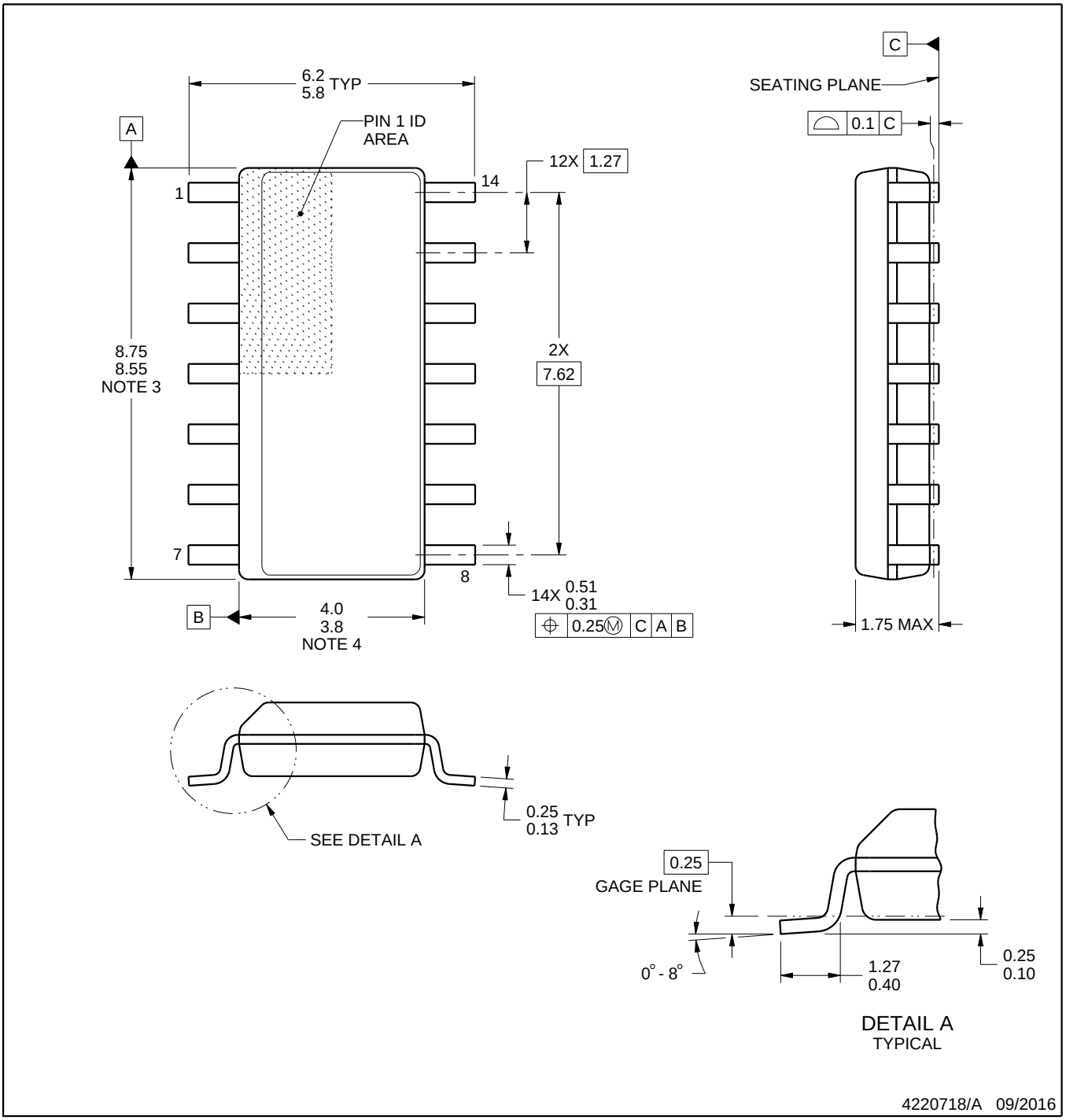


PACKAGE OUTLINE

D0014A

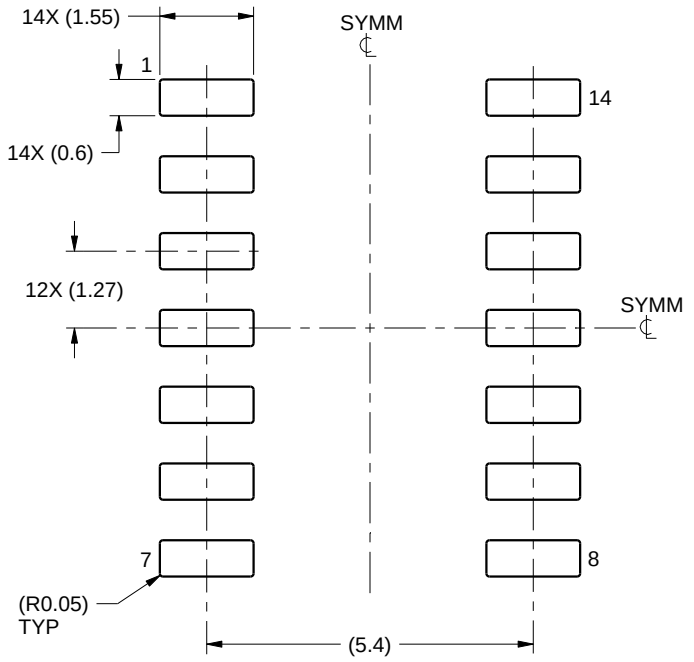
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

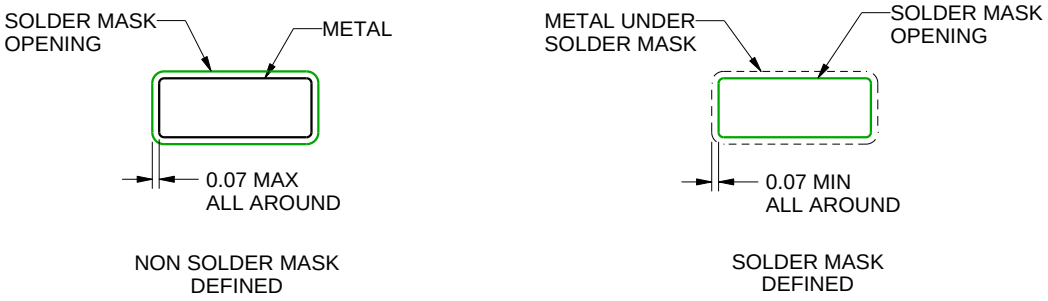


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

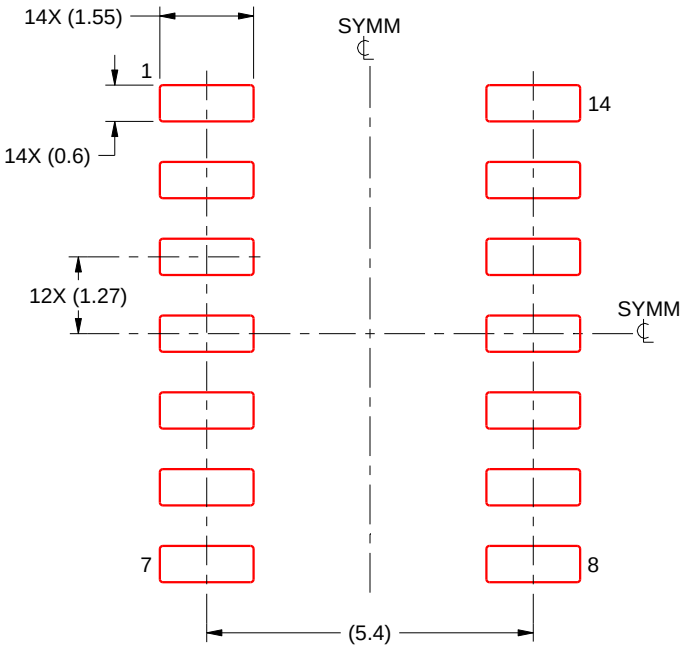
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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