LP3943 16-Channel RGB, White-LED Driver With Independent SMBUS/I²C String Control

1 Features

- Internal Power-On Reset
- Active Low Reset
- Internal Precision Oscillator
- Variable Dim Rates
  (From 6.25 ms to 1.6 s; 160 Hz to 0.625 Hz)
- 16 LED Drivers (Multiple Programmable States: ON, OFF, Input, and Dimming at a Specified Rate)
- 16 Open-Drain Outputs Capable of Driving up to 25 mA per LED

2 Applications

- Customized Flashing LED Lights for Cellular Phones
- Portable Applications
- Digital Cameras
- Indicator Lamps
- General Purpose I/O Expander
- Toys

3 Description

The LP3943 is an integrated device capable of independently driving 16 LEDs. This device also contains an internal precision oscillator that provides all the necessary timing required for driving each LED. Two prescaler registers, along with two PWM registers, provide a versatile duty-cycle control. The LP3943 contains the ability to dim LEDs in SMBUS/I²C applications where it is required, to cut down on bus traffic.

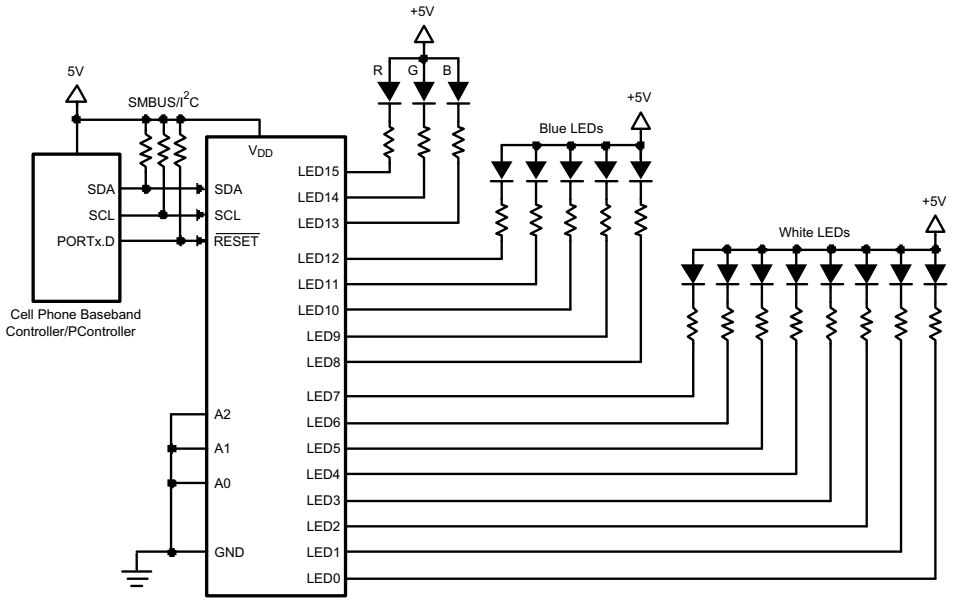
Traditionally, dimming LEDs using a serial shift register such as 74LS594/5 requires a large amount of traffic on the serial bus. The LP3943 instead requires only the setup of the frequency and duty cycle for each output pin; from then on, only a single command from the host is required to turn each individual open drain output to an ON or OFF state, or to cycle a programmed frequency and duty cycle. Maximum output sink current is 25 mA per pin and 200 mA per package. Any ports not used for controlling the LEDs can be used for general purpose input/output expansion.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3943	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (October 2015) to Revision D — **Page**

- Changed change wording of title to add SEO keywords ... 1
- Changed $R_{\theta JA}$ value from "37°C/W" to "45.0°C/W"; add additional thermal values ... 4

Changes from Revision B (September 2013) to Revision C — **Page**

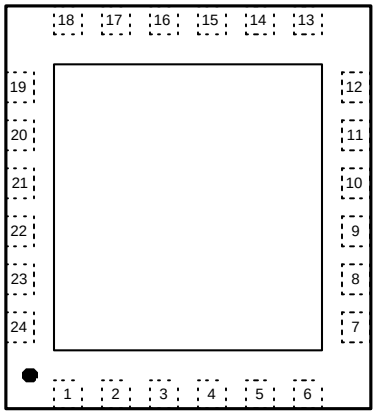
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections. ... 1

Changes from Revision A (April 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format; fixed format of Block Diagram ... 7

5 Pin Configuration and Functions

RTW Package
24-Pin WQFN With Exposed Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NUMBER	NAME		
1	LED0	Output	Output of LED0 Driver
2	LED1	Output	Output of LED1 Driver
3	LED2	Output	Output of LED2 Driver
4	LED3	Output	Output of LED3 Driver
5	LED4	Output	Output of LED4 Driver
6	LED5	Output	Output of LED5 Driver
7	LED6	Output	Output of LED6 Driver
8	LED7	Output	Output of LED7 Driver
9	GND	Ground	Ground
10	LED8	Output	Output of LED8 Driver
11	LED9	Output	Output of LED9 Driver
12	LED10	Output	Output of LED10 Driver
13	LED11	Output	Output of LED11 Driver
14	LED12	Output	Output of LED12 Driver
15	LED13	Output	Output of LED13 Driver
16	LED14	Output	Output of LED14 Driver
17	LED15	Output	Output of LED15 Driver
18	$\overline{\text{RST}}$	Input	Active Low Reset Input
19	SCL	Input	Clock Line for I^2C Interface
20	SDA	Input/Output	Serial Data Line for I^2C Interface
21	VDD	Power	Power Supply
22	A0	Input	Address Input 0
23	A1	Input	Address Input 1
24	A2	Input	Address Input 2
—	Exposed Pad	—	Tie internally to GND pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
V_{DD}	–0.5	6	V
A0, A1, A2, SCL, SDA, $\overline{RST}$ (Collectively called digital pins)		6	V
Voltage on LED pins	V_{SS} − 0.5	6	V
Junction temperature		150	°C
Power dissipation(4)		400	mW
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) The part cannot dissipate more than 400 mW.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	NOM	MAX	UNIT
V_{DD}	2.3		5.5	V
Junction temperature	–40		125	°C
Operating ambient temperature	–40		85	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device might occur. *Recommended Operating Conditions* are conditions under which operation of the device is ensured. *Recommended Operating Conditions* do not imply ensured performance limits. For verified performance limits and associated test conditions, see *Electrical Characteristics*.
(2) All voltages are with respect to the potential at the GND pin.

6.4 Thermal Information

THERMAL METRIC(1)		LP3943 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, V_{DD} = 5.5 V. Typical values and limits apply for T_J = 25°C. Minimum and maximum limits apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{DD}	Supply voltage		2.3	5	5.5	V
I_Q	Supply current	No load		350	550	µA
		Standby		2	5	
ΔI_Q	Additional standby current	V_{DD} = 5.5 V, every LED pin at 4.3 V			2	mA
V_{POR}	Power-On Reset voltage			1.8	1.96	V
t_w	Reset pulse width			10		ns
LED						
V_{IL}	Low level input voltage		−0.5		0.8	V
V_{IH}	High level input voltage		2		5.5	V
I_{OL}	Low level output current(2)	V_{OL} = 0.4 V, V_{DD} = 2.3 V	9			mA
		V_{OL} = 0.4 V, V_{DD} = 3 V	12			
		V_{OL} = 0.4 V, V_{DD} = 5 V	15			
		V_{OL} = 0.7 V, V_{DD} = 2.3 V	15			
		V_{OL} = 0.7 V, V_{DD} = 3 V	20			
		V_{OL} = 0.7 V, V_{DD} = 5 V	25			
I_{LEAK}	Input leakage current	V_{DD} = 3.6 V, V_{IN} = 0 V or V_{DD}	−1		1	µA
$C_{I/O}$	Input/output capacitance	See(3)		2.6	5	pF
ALL DIGITAL PINS (EXCEPT SCL AND SDA PINS)						
V_{IL}	LOW level input voltage		−0.5		0.8	V
V_{IH}	HIGH level input voltage		2		5.5	V
I_{LEAK}	Input leakage current		−1		1	µA
C_{IN}	Input capacitance	V_{IN} = 0 V(3)		2.3	5	pF
I^2C INTERFACE (SCL AND SDA PINS)						
V_{IL}	LOW level input voltage		–0.5		$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$		5.5	V
V_{OL}	LOW level output voltage		0		$0.2V_{DD}$	V
I_{OL}	LOW level output current	V_{OL} = 0.4 V	3	6.5		mA
f_{CLK}	Clock frequency				400	kHz

(1) Limits are ensured. All electrical characteristics having room-temperature limits are tested during production with T_J = 25°C. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) Each LED pin must not exceed 25 mA and each octal (LED0–LED7; LED8–LED15) must not exceed 100 mA. The package must not exceed a total of 200 mA.
(3) Verified by design.

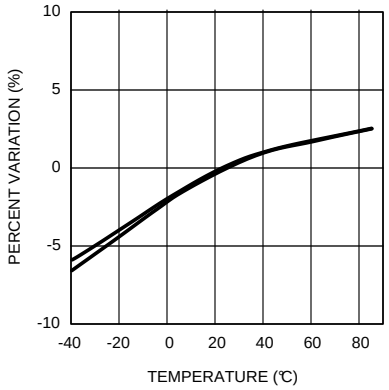
6.6 I²C Interface (SCL and SDA Pins) Timing Requirements

See (1)

		MIN	NOM	MAX	UNIT
t_{HOLD}	Hold time repeated START condition	0.6			µs
t_{CLK-LP}	CLK low period	1.3			µs
t_{CLK-HP}	CLK high period	0.6			µs
t_{SU}	Setup time repeated START condition	0.6			µs
$t_{DATA-HOLD}$	Data hold time	300			ns
$t_{DATA-SU}$	Data setup time	100			ns
t_{SU}	Setup time for STOP condition	0.6			µs
t_{TRANS}	Maximum pulse width of spikes that must be suppressed by the input filter of both DATA and CLK signals		50		ns

(1) All values verified by design.

6.7 Typical Characteristic



T_A = −40°C to +85°C V_{DD} = 2.3 V to 3 V

Figure 1. Frequency vs. Temperature

7 Detailed Description

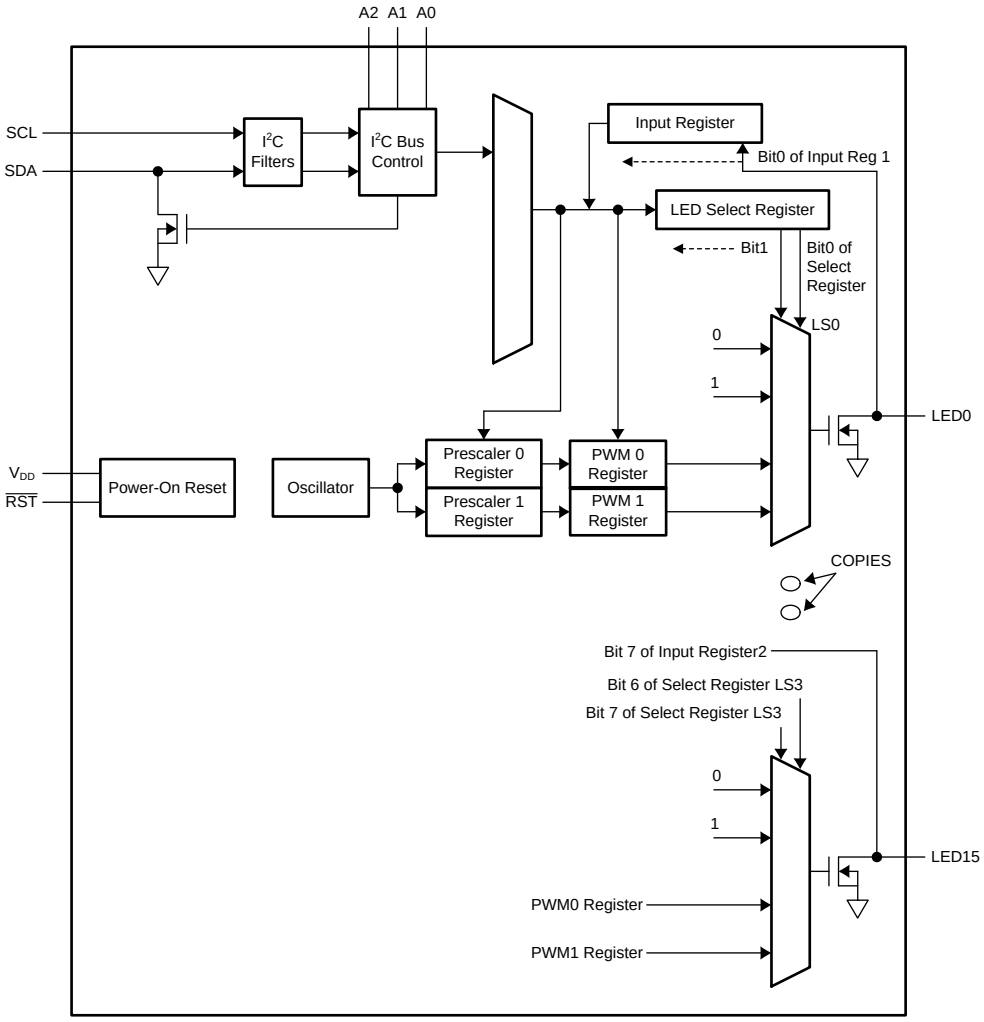
7.1 Overview

The LP3943 takes incoming data from the baseband controller and feeds them into several registers that control the frequency and the duty cycle of the LEDs. Two prescaler registers and two PWM registers provide two individual rates to dim or blink the LEDs (for more information on these registers, refer to Table 1). Each LED can be programmed in one of four states: ON, OFF, DIM0 rate, or DIM1 rate. Two read-only registers provide status on all 16 LEDs. The LP3943 can be used to drive RGB LEDs and/or single-color LEDs to create a colorful, entertaining, and informative setting. Alternatively, it can also drive RGB LED as a flashlight. This is particularly suitable for accessory functions in cellular phones and toys. Any LED pins not used to drive LED can be used for general purpose parallel input/output (GPIO) expansion.

The LP3943 is equipped with power-on reset that holds the chip in a reset state until V_{DD} reaches V_{POR} during power up. Once V_{POR} is achieved, the LP3943 comes out of reset and initializes itself to the default state.

To bring the LP3943 into reset, hold the $\overline{\text{RST}}$ pin LOW for a period of TW. This puts the chip into its default state. The LP3943 can only be programmed after $\overline{\text{RST}}$ signal is HIGH again.

7.2 Functional Block Diagram



7.3 Feature Description

Some of the features of the LP3943 device are:

1. 16 low-side switches to control the current in 16 strings of LEDs with a maximum of 25 mA per switch or a maximum of 200 mA total.
2. Programmable internal PWM dimming:
   (a) Duty cycle control (8 bits). Any of the 16 current switches can be mapped to either PWM0 register or PWM1 register. Each register offers 8-bit PWM duty cycle control.
   (b) PWM Frequency control (8 bits). Any of the 16 current switches can be mapped to either PSC0 register or PSC1 register. Each register offers 8-bit PWM frequency control from 0.625 Hz to 160 Hz.
3. $\overline{\text{RESET}}$ input.
4. Auto increment for I2C writes to reduce number of I2C clock pulses .
5. The LP3943 provides for an externally selectable I2C slave address via the ADR0, ADR1, and ADR2 inputs. See Figure 4.

7.4 Device Functional Modes

1. Output set to high impedance. This is set by programming bits [B0 and B1] to 00 in the LS0, LS1, LS2, or LS3 registers (see Table 2)
2. Output set to ON state (current switch pulls low). This turns the LED on at the full current in the specified current switch bits [B0 and B1] set to 01 in the LS0, LS1, LS2, or LS3 registers (see Table 12).
3. Output set to toggle at the programmed PWM duty cycle and PWM frequency. This turns on or off the specified current switch at the programmed PWM frequency and duty cycle. Each current switch is mapped to either of the PWM0/PSC0 or PWM1/PSC1 pairs by setting [B0 and B1] to 10 or 11 in the LS0, LS1, LS2, or LS3 registers (see Table 12).

7.5 Programming

7.5.1 I²C Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

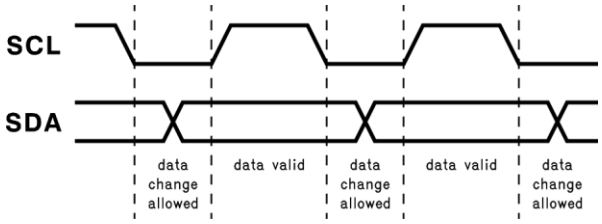


Figure 2. I²C Data Validity

7.5.2 I²C START and STOP Conditions

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

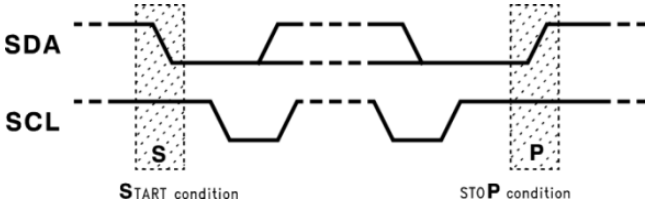


Figure 3. I²C START and STOP Conditions

7.5.3 Transferring Data

Every byte put on the SDA line must be eight bits long with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3943 hardwires bits 7 to 4 and leaves bits 3 to 1 selectable, as shown in Figure 4. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The LP3943 supports only a WRITE during chip addressing. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

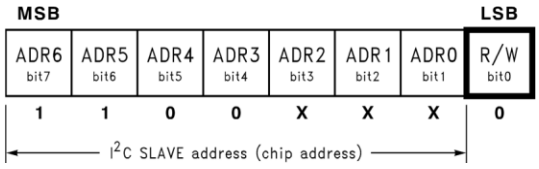
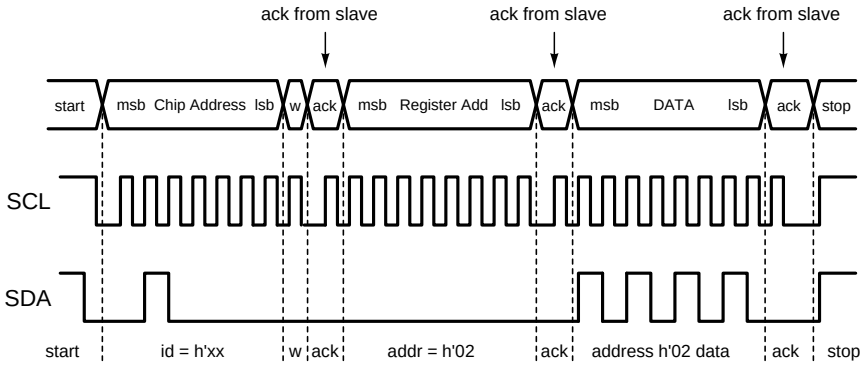


Figure 4. Chip Address Byte

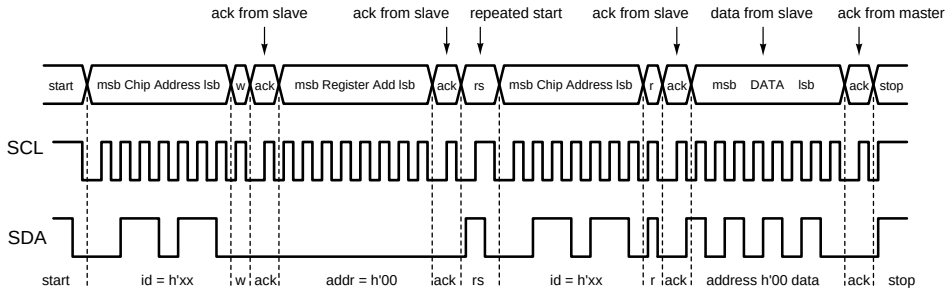
Programming (continued)



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled LOW by either master or slave)
rs = repeated start
xx = 60 to 67

Figure 5. LP3943 Register Write

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in Figure 6.



w = write (SDA = “0”)
r = read (SDA = “1”)
ack = acknowledge (SDA pulled LOW by either master or slave)
rs = repeated start
xx = 60 to 67

Figure 6. LP3943 Register Read

7.5.4 Auto Increment

Auto increment is a special feature supported by the LP3943 to eliminate repeated chip and register addressing when data are to be written to or read from registers in sequential order. The auto increment bit is inside the register address byte, as shown in Figure 7. Auto increment is enabled when this bit is programmed to “1” and disabled when it is programmed to “0”.

Bits 5, 6 and 7 in the register address byte must always be zero.

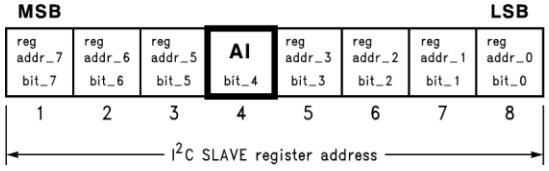


Figure 7. Register Address Byte

Programming (continued)

In the READ mode, when auto increment is enabled, I^2C master could receive any number of bytes from LP3943 without selecting chip address and register address again. Every time the I^2C master reads a register, the LP3943 increments the register address, and the next data register is read. When I^2C master reaches the last register (09H), the register address rolls over to 00H.

In the WRITE mode, when auto increment is enabled, the LP3943 increments the register address every time I^2C master writes to register. When the last register (09H register) is reached, the register address rolls over to 02H, not 00H, because the first two registers in LP3943 are read-only registers. It is possible to write to the first two registers independently, and the LP3943 device will acknowledge, but the data is ignored.

If auto increment is disabled, and the I^2C master does not change register address, it continues to write data into the same register.

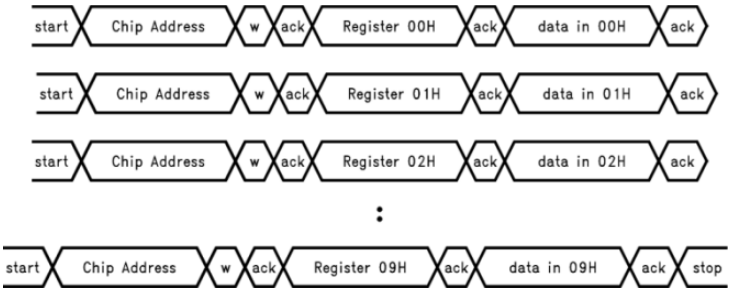


Figure 8. Programming With Auto Increment Disabled (in WRITE Mode)

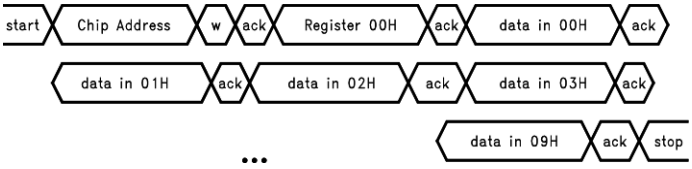


Figure 9. Programming With Auto Increment Enabled (in WRITE Mode)

7.6 Register Maps

Table 1. LP3943 Register Table

Address (Hex)	Register Name	Read/Write	Register Function
0x00	Input 1	Read Only	LED0–7 Input Register
0x01	Input 2	Read Only	LED8–15 Input Register
0x02	PSC0	R/W	Frequency Prescaler 0
0x03	PWM0	R/W	PWM Register 0
0x04	PSC1	R/W	Frequency Prescaler 1
0x05	PWM1	R/W	PWM Register 1
0x06	LS0	R/W	LED0–3 Selector
0x07	LS1	R/W	LED4–7 Selector
0x08	LS2	R/W	LED8–11 Selector
0x09	LS3	R/W	LED12–15 Selector

7.6.1 Binary Format for Input Registers (Read-only)—Address 0x00 and 0x01

Table 2. Address 0x00

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED7	LED6	LED5	LED4	LED3	LED2	LED1	LED0

Table 3. Address 0x01

Bit #	7	6	5	4	3	2	1	0
Default value	X	X	X	X	X	X	X	X
	LED15	LED14	LED13	LED12	LED11	LED10	LED9	LED8

7.6.2 Binary Format for Frequency Prescaler and PWM Registers — Address 0x02 to 0x05

Table 4. Address 0x02 (PSC0)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

Table 5. Address 0x03 (PWM0)

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

Table 6. Address 0x04 (PSC1)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0

Table 7. Address 0x05 (PWM1)

Bit #	7	6	5	4	3	2	1	0
Default value	1	0	0	0	0	0	0	0

7.6.3 Binary Format for Selector Registers — Address 0x06 to 0x09

Table 8. Address 0x06 (LS0)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED3		LED2		LED1		LED0	

Table 9. Address 0x07 (LS1)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED7		LED6		LED5		LED4	

Table 10. Address 0x08 (LS2)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED11		LED10		LED9		LED8	

Table 11. Address 0x09 (LS3)

Bit #	7	6	5	4	3	2	1	0
Default value	0	0	0	0	0	0	0	0
	B1	B0	B1	B0	B1	B0	B1	B0
	LED15		LED14		LED13		LED12	

Table 12. LED States With Respect To Values in B1 and B0

B1	B0	Function
0	0	Output Hi-Z (LED off)
0	1	Output LOW (LED on)
1	0	Output dims (DIM0 rate)
1	1	Output dims (DIM1 rate)

Programming Example:

- Dim LEDs 0 to 7 at 1 Hz at 25% duty cycle
- Dim LEDs 8 to 12 at 5 Hz at 50% duty cycle
- Set LEDs 13, 14 and 15 off
- Step 1: Set PSC0 to achieve DIM0 of 1 s
- Step 2: Set PWM0 duty cycle to 25%
- Step 3: Set PSC1 to achieve DIM1 of 0.2 s
- Step 4: Set PWM1 duty cycle to 50%
- Step 5: Set LEDs 13, 14 and 15 off by loading the data into LS3 register
- Step 6: Set LEDs 0 to 7 to point to DIM0
- Step 7: Set LEDs 8 to 12 to point to DIM1

Table 13. Programming Details

STEP	DESCRIPTION	REGISTER NAME	SET TO (HEX)
1	Set DIM0 = 1 s 1 = (PSC0 + 1)/160 PSC0 = 159	PSC0	0x09F
2	Set duty cycle to 25% Duty Cycle = PWM0/256 PWM0 = 64	PWM0	0x40
3	Set DIM1 = 0.2s 0.2 = (PSC1 + 1)/160 PSC1 = 31	PSC1	0x1F
4	Set duty cycle to 50% Duty Cycle = PWM1/256 PWM1 = 128	PWM1	0x80
5	LEDs 13, 14 and 15 off Output = HIGH	LS3	0x03
6	LEDs 0 to 7 Output = DIM0	LS0, LS1	LS0 = 0xAA LS1 = 0xAA
7	LEDs 8 to 12 Output = DIM1	LS2, LS3	LS2 = 0xFF LS3 = 0x03

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3943 is a 16-channel LED controller which has 16 low-side current switches. Each switch can control the LED current in its respective LED or LEDs by modulating its duty cycle and frequency.

8.2 Typical Application

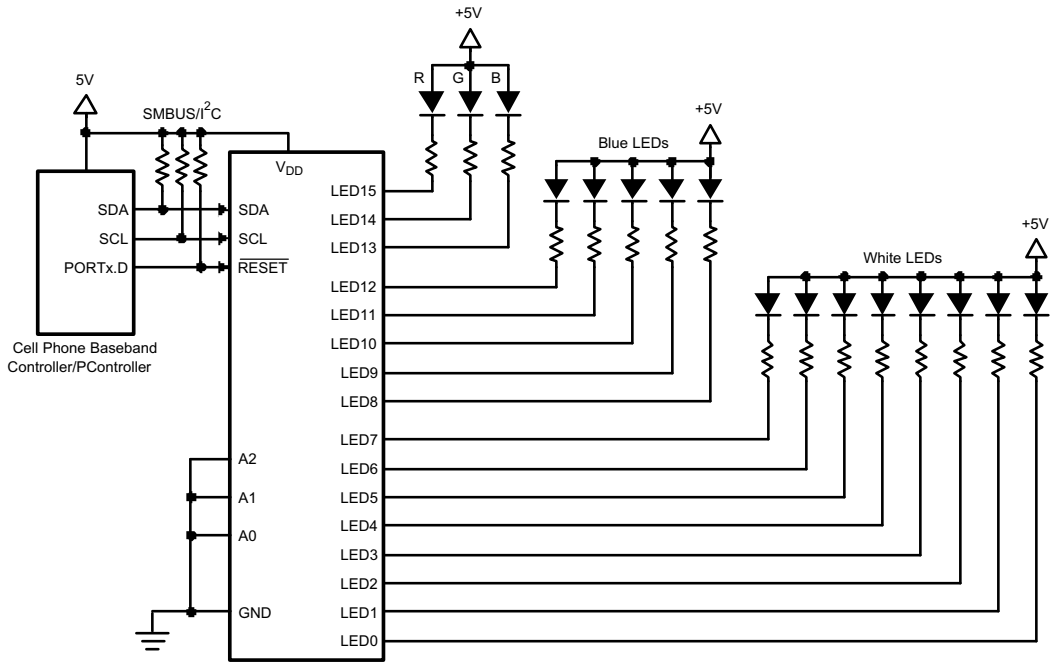


Figure 10. LP3943 Typical Application

8.2.1 Design Requirements

For typical RGB LED light-driver applications, use the parameters listed in Table 14.

Table 14. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.3 V
Typical output voltage	5 V
Output current	20 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Reducing I_Q When LEDs are OFF

In many applications, the LEDs and the LP3943 share the same V_{DD}, as shown in Figure 10. When the LEDs are off, the LED pins are at a lower potential than V_{DD}, causing extra supply current (ΔI_Q). To minimize this current, consider keeping the LED pins at a voltage equal to or greater than V_{DD}.

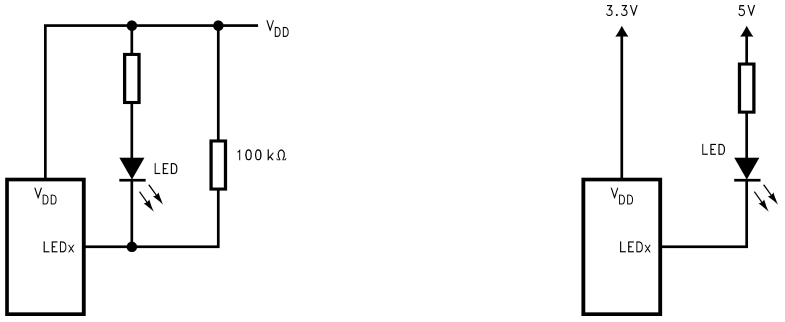


Figure 11. Methods to Reduce I_Q When LEDs are in OFF State

8.2.3 Application Curve

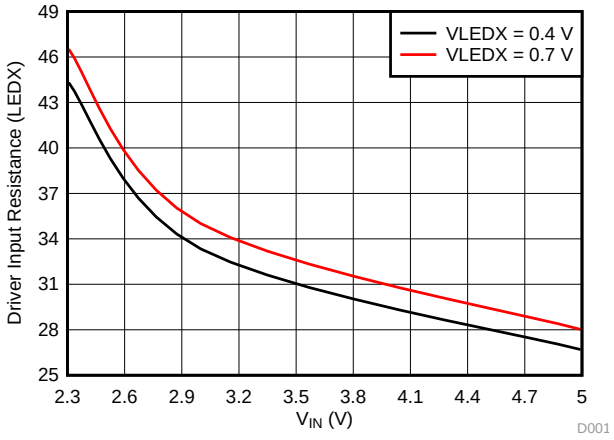


Figure 12. Typical LED Switch Resistance

8.3 System Examples

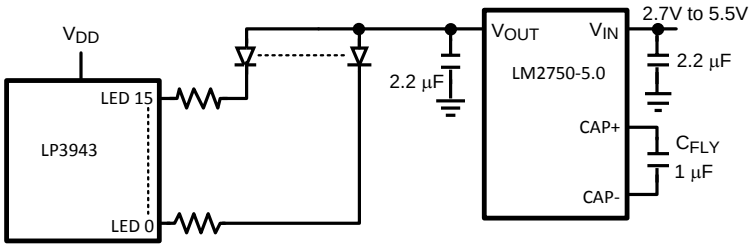


Figure 13. LP3943 With 5-V Booster

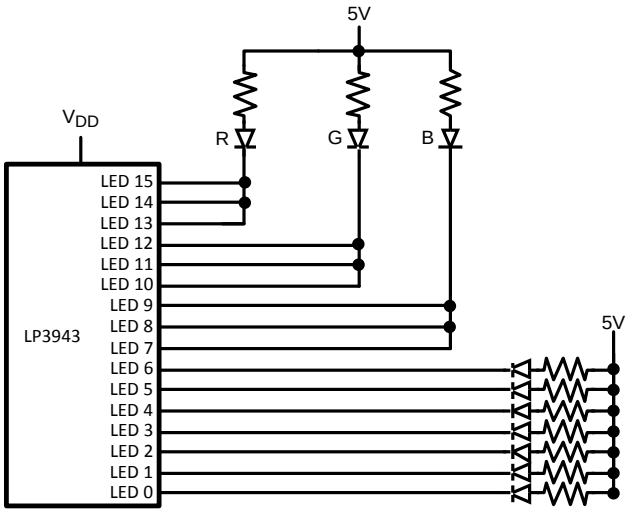


Figure 14. LP3943 Driving RGB LED as a Flash

9 Power Supply Recommendations

The LP3943 is designed to be powered from a 2.3-V minimum to a 5.5-V maximum supply input.

10 Layout

10.1 Layout Guidelines

The LP3943 layout is not critical, but TI recommends providing a noise-free supply input at V_{DD}. This typically would require a 1-µF capacitor placed close to the VDD pin and ground.

10.2 Layout Example

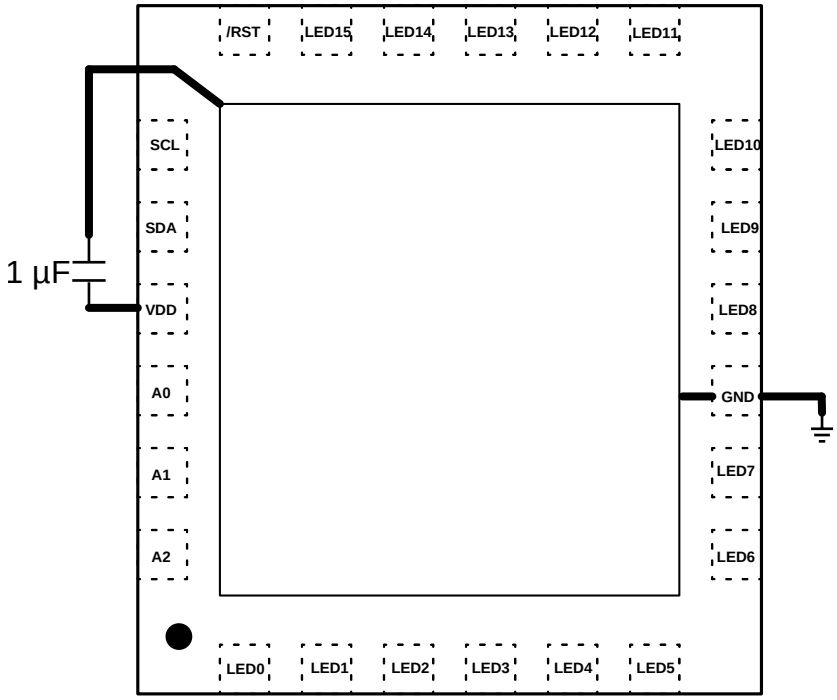


Figure 15. LP3943 Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3943ISQ/NOPB	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3943SQ	Samples
LP3943ISQX/NOPB	ACTIVE	WQFN	RTW	24	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3943SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

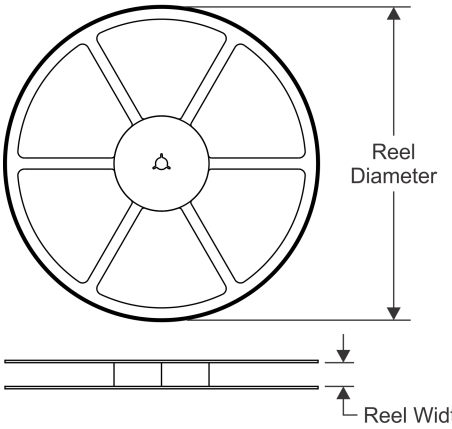
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

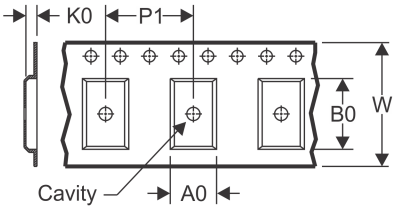
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

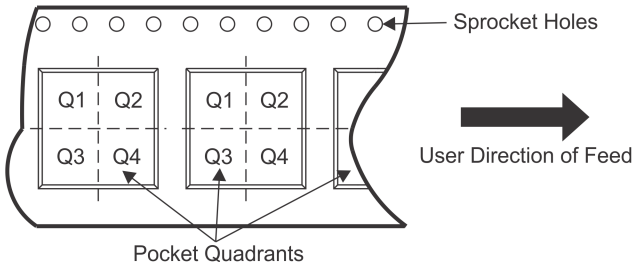


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

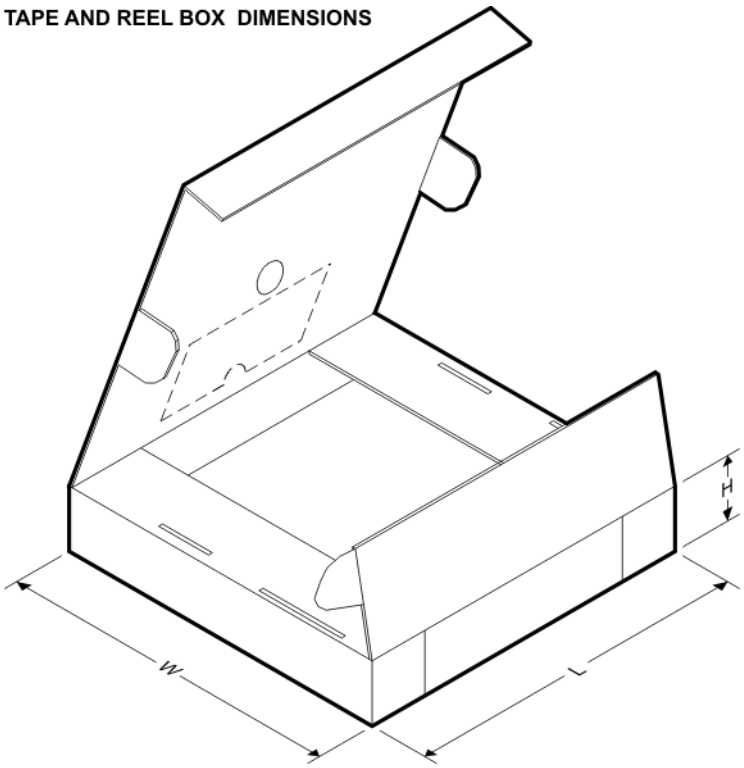
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3943ISQ	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3943ISQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP3943ISQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3943ISQ	WQFN	RTW	24	1000	208.0	191.0	35.0
LP3943ISQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LP3943ISQX/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

GENERIC PACKAGE VIEW

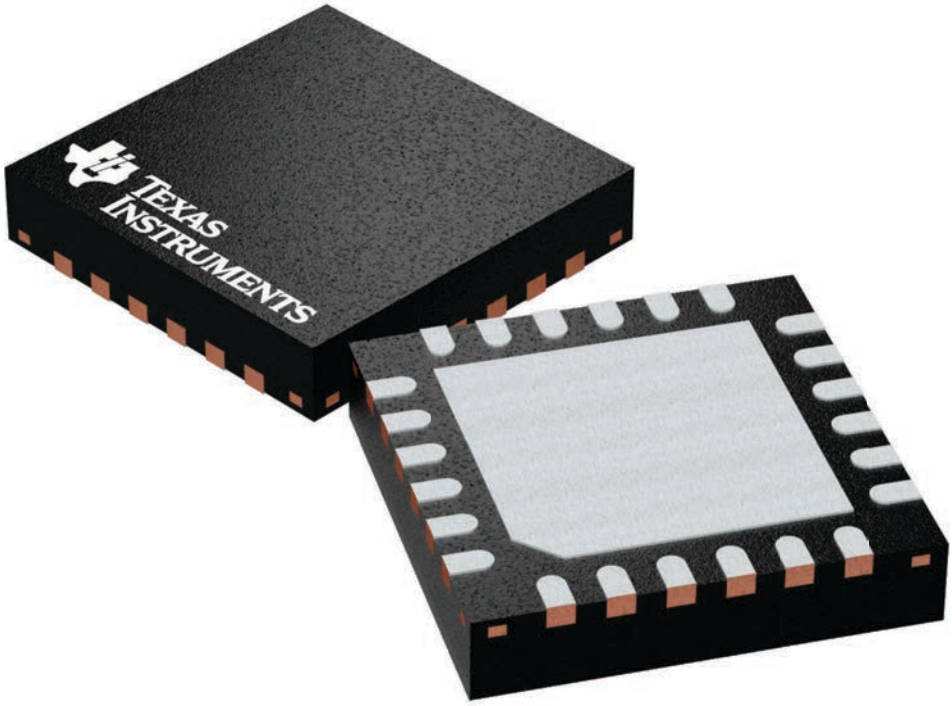
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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