

LM4808 Boomer® Audio Power Amplifier Series

Low Voltage High Power Audio Power Amplifier

Check for Samples: [LM4808](#)

FEATURES

- **WSON, VSSOP, and SOIC Surface Mount Packaging**
- **Switch On/Off Click Suppression**
- **Excellent Power Supply Ripple Rejection**
- **Unity-Gain Stable**
- **Minimum External Components**

APPLICATIONS

- **Headphone Amplifier**
- **Personal Computers**
- **Portable Electronic Devices**

KEY SPECIFICATIONS

- **THD+N at 1kHz at 105mW Continuous Average Output Power Into 16Ω 0.1 % (typ)**
- **THD+N at 1kHz at 70mW Continuous Average Output Power Into 32Ω 0.1 % (typ)**
- **Output Power at 0.1% THD+N at 1kHz Into 32Ω 70 mW (typ)**

DESCRIPTION

The LM4808 is a dual audio power amplifier capable of delivering 105mW per channel of continuous average power into a 16Ω load with 0.1% (THD+N) from a 5V power supply.

Boomer audio power amplifiers were designed specifically to provide high quality output power with a minimal amount of external components using surface mount packaging. Since the LM4808 does not require bootstrap capacitors or snubber networks, it is optimally suited for low-power portable systems.

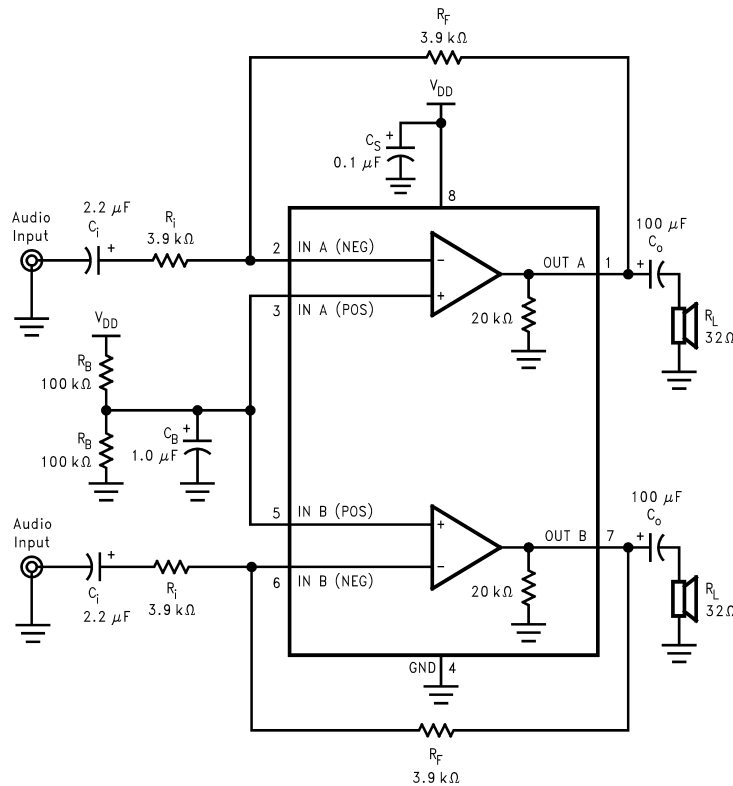
The unity-gain stable LM4808 can be configured by external gain-setting resistors.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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Typical Application



*Refer to the [APPLICATION INFORMATION](#) section for information concerning proper selection of the input and output coupling capacitors.

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

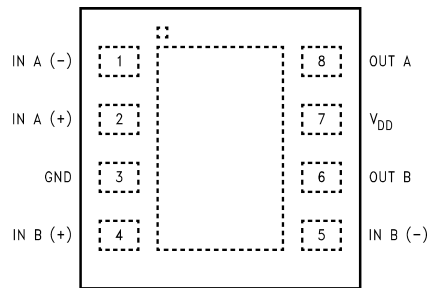


Figure 2. Top View
WSON Package
See Package Number NGL0008B

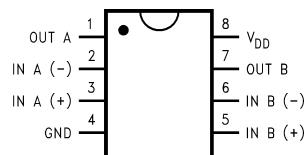


Figure 3. Top View
SOIC & VSSOP Package
See Package Number D0008A, DGK0008A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Supply Voltage		6.0V	
Storage Temperature		-65°C to +150°C	
Input Voltage		-0.3V to $V_{DD} + 0.3V$	
Power Dissipation ⁽³⁾		Internally limited	
ESD Susceptibility ⁽⁴⁾		3500V	
ESD Susceptibility ⁽⁵⁾		250V	
Junction Temperature		150°C	
Soldering Information ⁽⁶⁾	Small Outline Package	Vapor Phase (60 seconds)	215°C
		Infrared (15 seconds)	220°C
Thermal Resistance		θ_{JC} (VSSOP)	56°C/W
		θ_{JA} (VSSOP)	210°C/W
		θ_{JC} (SOIC)	35°C/W
		θ_{JA} (SOIC)	170°C/W
		θ_{JC} (WSON)	15°C/W
		θ_{JA} (WSON)	117°C/W ⁽⁷⁾
		θ_{JA} (WSON)	150°C/W ⁽⁸⁾

- (1) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature T_A . The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$. For the LM4808, $T_{JMAX} = 150^\circ\text{C}$, and the typical junction-to-ambient thermal resistance, when board mounted, is 210°C/W for package DGK0008A and 170°C/W for package D0008A.
- (4) Human body model, 100 pF discharged through a 1.5 kΩ resistor.
- (5) Machine Model, 220 pF–240 pF discharged through all pins.
- (6) See <http://www.ti.com> for other methods of soldering surface mount devices.
- (7) The given θ_{JA} is for an LM4808 packaged in an NGL0008B with the Exposed-DAP soldered to a printed circuit board copper pad with an area equivalent to that of the Exposed-DAP itself.
- (8) The given θ_{JA} is for an LM4808 packaged in an NGL0008B with the Exposed-DAP not soldered to any printed circuit board copper.

OPERATING RATINGS

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$
Supply Voltage		$2.0V \leq V_{DD} \leq 5.5V$

ELECTRICAL CHARACTERISTICS ^{(1) (2)}

The following specifications apply for $V_{DD} = 5V$ unless otherwise specified, limits apply to $T_A = 25^\circ\text{C}$.

Symbol	Parameter	Conditions	LM4808		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾	
V_{DD}	Supply Voltage			2.0	V (min)
				5.5	V (max)
I_{DD}	Supply Current	$V_{IN} = 0V, I_O = 0A$	1.2	3.0	mA (max)

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (3) Typicals are measured at 25°C and represent the parametric norm.
- (4) Tested limits are specified to AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS ⁽¹⁾ ⁽²⁾ (continued)

The following specifications apply for $V_{DD} = 5V$ unless otherwise specified, limits apply to $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	LM4808		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾	
P_{tot}	Total Power Dissipation	$V_{IN} = 0V, I_O = 0A$	6	16.5	mW (max)
V_{OS}	Input Offset Voltage	$V_{IN} = 0V$	10	50	mV (max)
I_{bias}	Input Bias Current		10		pA
V_{CM}	Common Mode Voltage		0		V
			4.3		V
G_V	Open-Loop Voltage Gain	$R_L = 5k\Omega$	67		dB
I_O	Max Output Current	THD+N < 0.1 %	70		mA
R_O	Output Resistance		0.1		Ω
V_O	Output Swing	$R_L = 32\Omega, 0.1\% \text{ THD+N, Min}$.3		V
		$R_L = 32\Omega, 0.1\% \text{ THD+N, Max}$	4.7		
PSRR	Power Supply Rejection Ratio	$C_b = 1.0\mu F, V_{ripple} = 100mV_{pp}, f = 100Hz$	89		dB
Crosstalk	Channel Separation	$R_L = 32\Omega$	75		dB
THD+N	Total Harmonic Distortion + Noise	$f = 1 \text{ kHz}$			
		$R_L = 16\Omega, V_O = 3.5V_{pp}$ (at 0 dB)	0.05		%
			66		dB
		$R_L = 32\Omega, V_O = 3.5V_{pp}$ (at 0 dB)	0.05		%
			66		dB
SNR	Signal-to-Noise Ratio	$V_O = 3.5V_{pp}$ (at 0 dB)	105		dB
f_G	Unity Gain Frequency	Open Loop, $R_L = 5k\Omega$	5.5		MHz
P_O	Output Power	THD+N = 0.1%, $f = 1 \text{ kHz}$			
		$R_L = 16\Omega$	105		mW
		$R_L = 32\Omega$	70	60	mW
		THD+N = 10%, $f = 1 \text{ kHz}$			
		$R_L = 16\Omega$	150		mW
			90		mW
C_I	Input Capacitance		3		pF
C_L	Load Capacitance			200	pF
SR	Slew Rate	Unity Gain Inverting	3		V/ μs

ELECTRICAL CHARACTERISTICS ⁽¹⁾ ⁽²⁾

The following specifications apply for $V_{DD} = 3.3V$ unless otherwise specified, limits apply to $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾	
I_{DD}	Supply Current	$V_{IN} = 0V, I_O = 0A$	1.0		mA (max)
V_{OS}	Input Offset Voltage	$V_{IN} = 0V$	7		mV (max)

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (3) Typicals are measured at $25^\circ C$ and represent the parametric norm.
- (4) Tested limits are specified to AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

ELECTRICAL CHARACTERISTICS ⁽¹⁾ ⁽²⁾ (continued)

The following specifications apply for $V_{DD} = 3.3V$ unless otherwise specified, limits apply to $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾	
P _o	Output Power	THD+N = 0.1%, f = 1 kHz			
		R _L = 16Ω	40		mW
		R _L = 32Ω	28		mW
		THD+N = 10%, f = 1 kHz			
		R _L = 16Ω	56		mW
		R _L = 32Ω	38		mW

ELECTRICAL CHARACTERISTICS ⁽¹⁾ ⁽²⁾

The following specifications apply for $V_{DD} = 2.6V$ unless otherwise specified, limits apply to $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Conditions		Units (Limits)
			Typ ⁽³⁾	Limit ⁽⁴⁾	
I _{DD}	Supply Current	V _{IN} = 0V, I _O = 0A	0.9		mA (max)
V _{OS}	Input Offset Voltage	V _{IN} = 0V	5		mV (max)
P _o	Output Power	THD+N = 0.1%, f = 1 kHz			
		R _L = 16Ω	20		mW
		R _L = 32Ω	16		mW
		THD+N = 10%, f = 1 kHz			
		R _L = 16Ω	31		mW
		R _L = 32Ω	22		mW

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which ensure specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not ensured for parameters where no limit is given, however, the typical value is a good indication of device performance.
- (3) Typicals are measured at 25°C and represent the parametric norm.
- (4) Tested limits are specified to AOQL (Average Outgoing Quality Level). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

EXTERNAL COMPONENTS DESCRIPTION

(Figure 1)

Components	Functional Description
1. R _i	The inverting input resistance, along with R _f , set the closed-loop gain. R _i , along with C _i , form a high pass filter with $f_c = 1/(2\pi R_i C_i)$.
2. C _i	The input coupling capacitor blocks DC voltage at the amplifier's input terminals. C _i , along with R _i , create a highpass filter with $f_c = 1/(2\pi R_i C_i)$. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS , for an explanation of determining the value of C _i .
3. R _f	The feedback resistance, along with R _i , set closed-loop gain.
4. C _S	This is the supply bypass capacitor. It provides power supply filtering. Refer to the APPLICATION INFORMATION section for proper placement and selection of the supply bypass capacitor.
5. C _B	This is the half-supply bypass pin capacitor. It provides half-supply filtering. Refer to the section, SELECTING PROPER EXTERNAL COMPONENTS , for information concerning proper placement and selection of C _B .
6. C _O	This is the output coupling capacitor. It blocks the DC voltage at the amplifier's output and forms a high pass filter with R _L at $f_o = 1/(2\pi R_L C_O)$
7. R _B	This is the resistor which forms a voltage divider that provides 1/2 V _{DD} to the non-inverting input of the amplifier.

TYPICAL PERFORMANCE CHARACTERISTICS

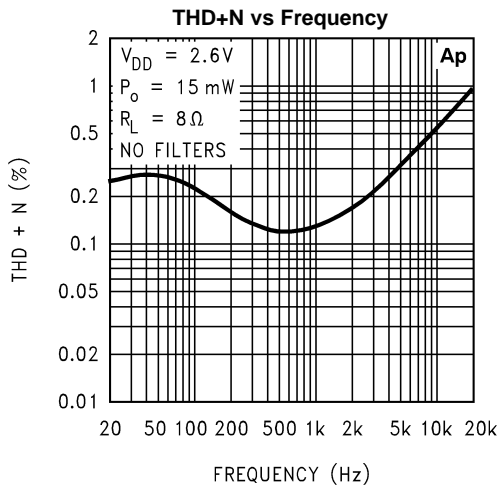


Figure 4.

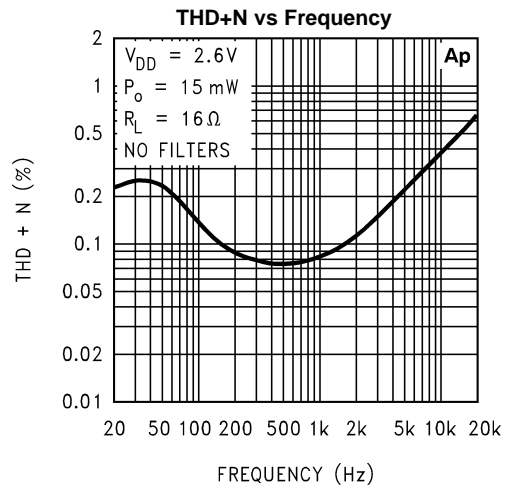


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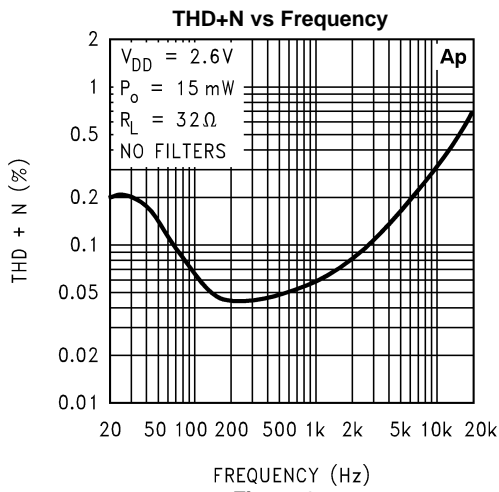


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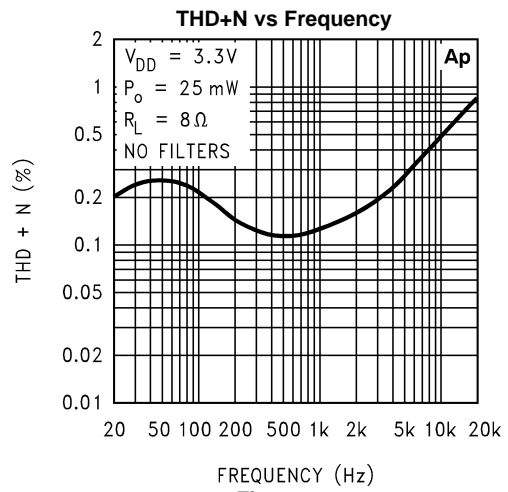


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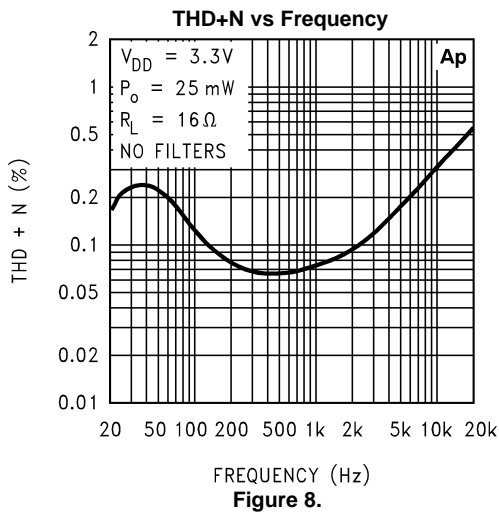


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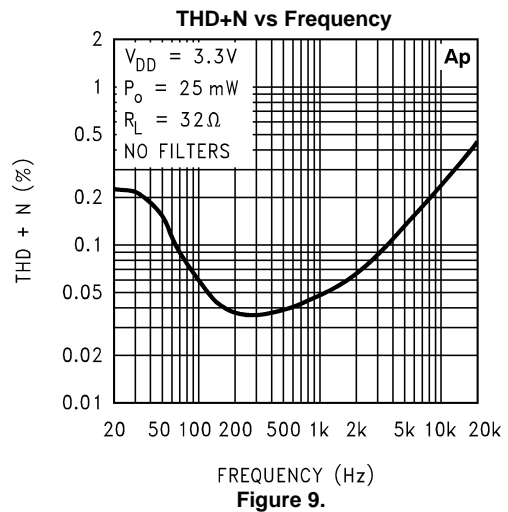
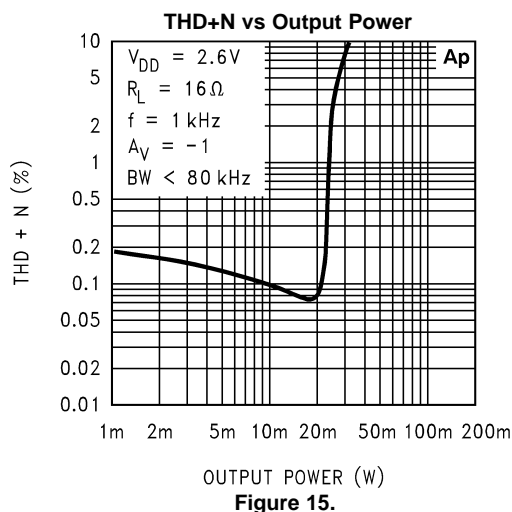
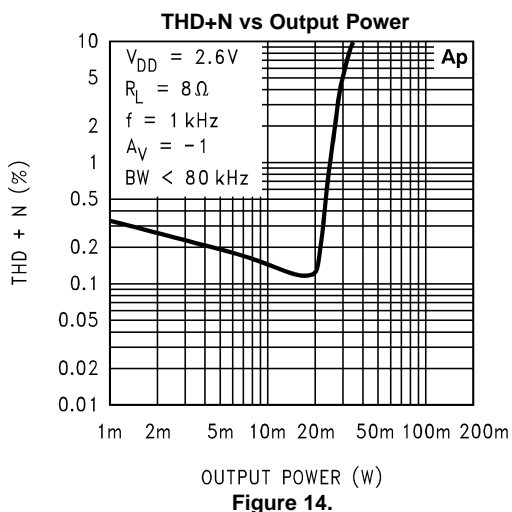
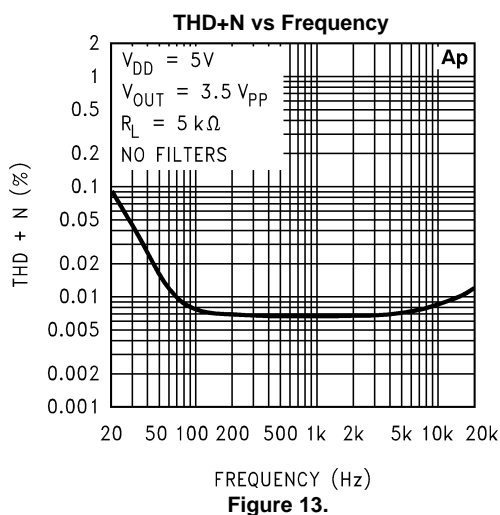
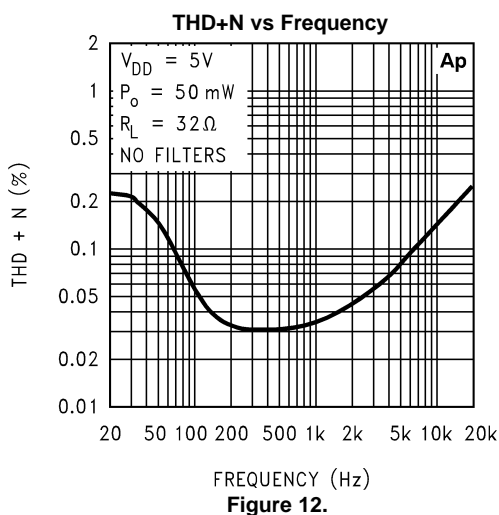
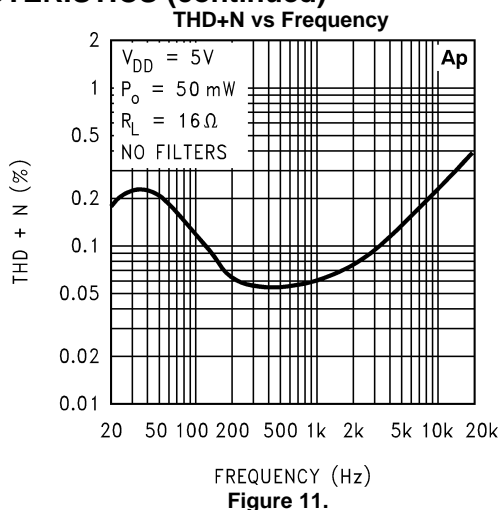
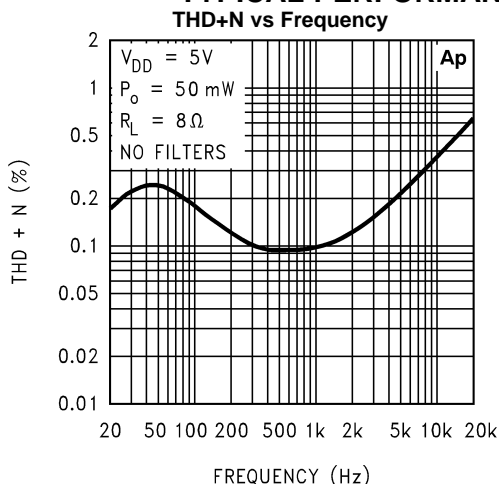


Figure 9.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

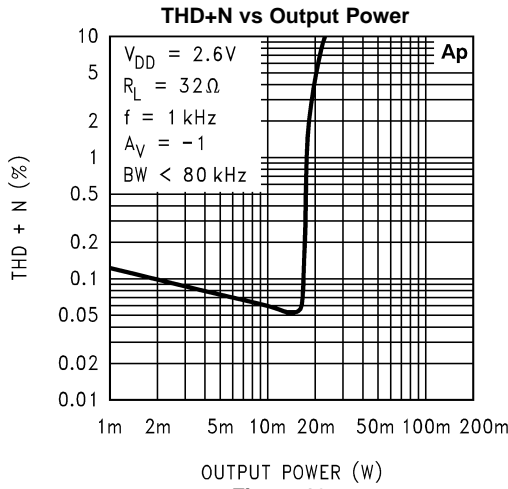


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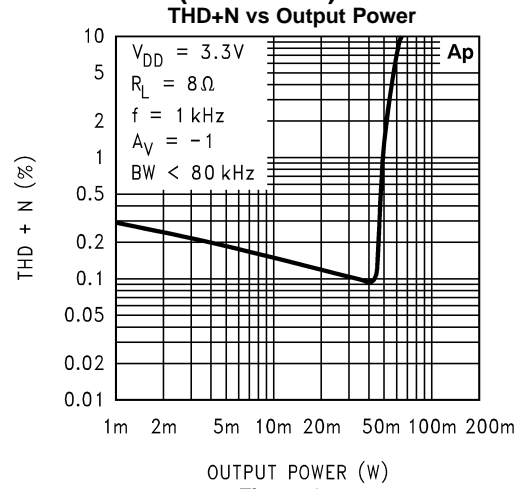


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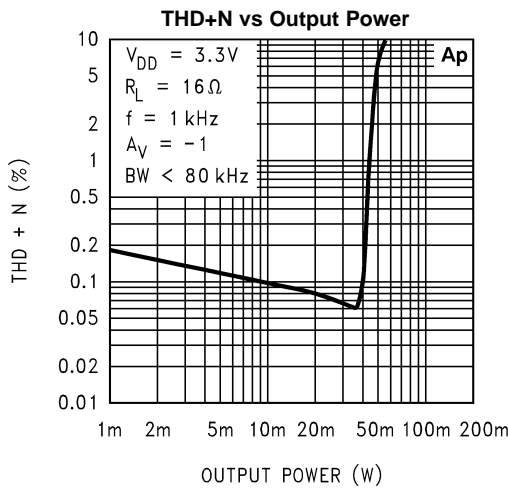


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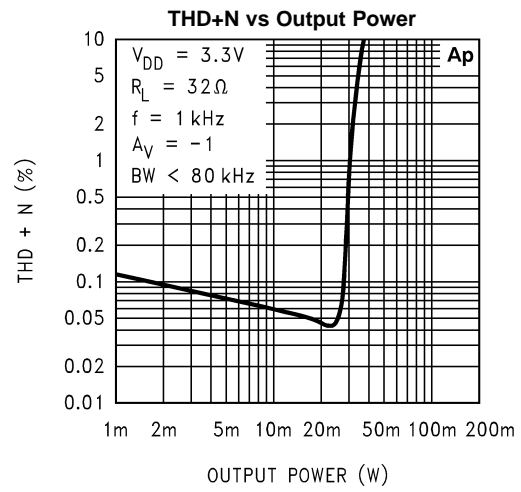


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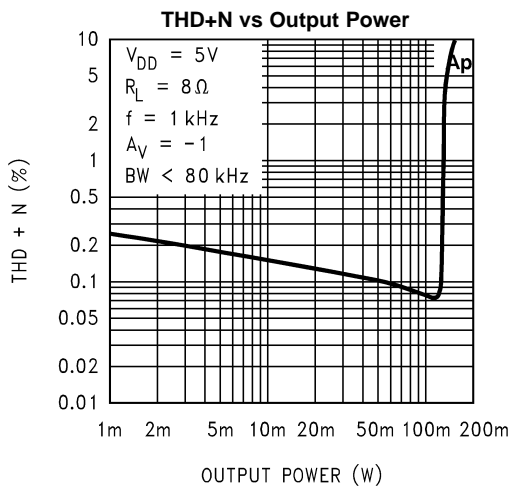


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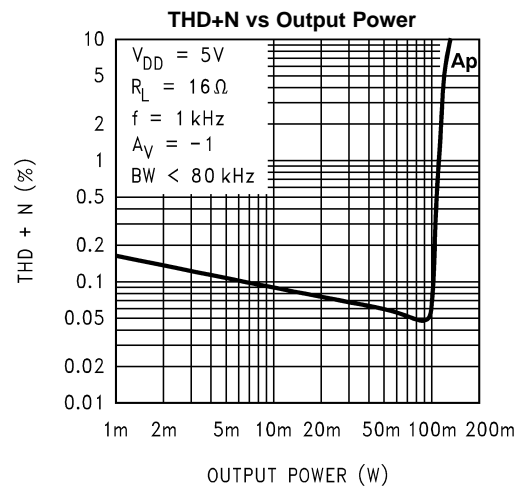


Figure 21.

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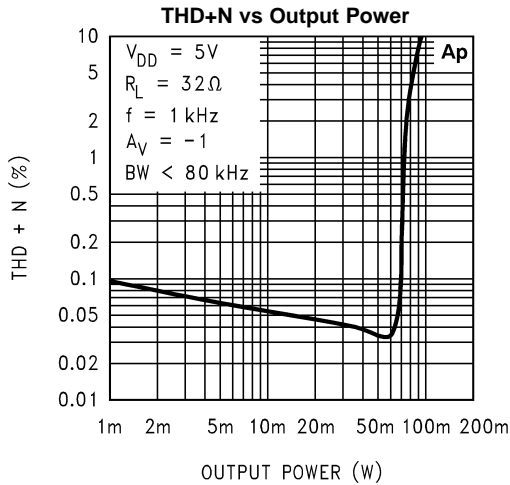


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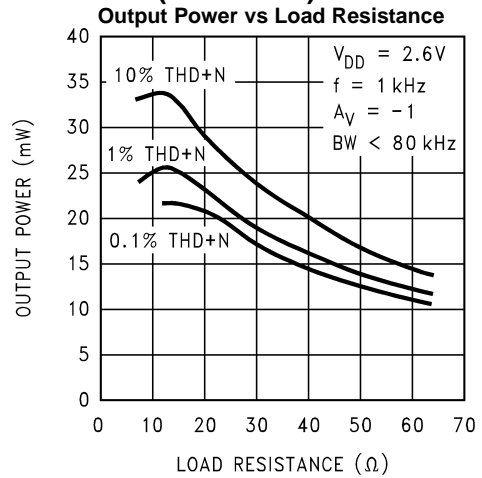


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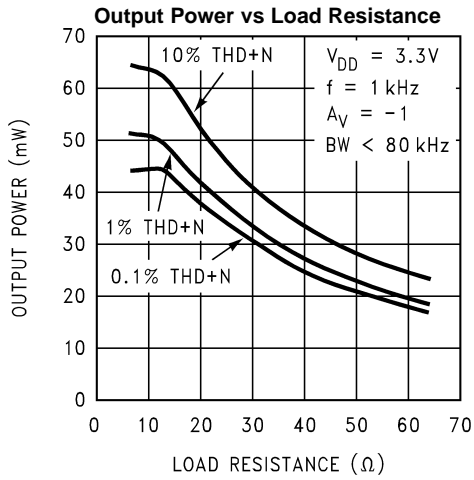


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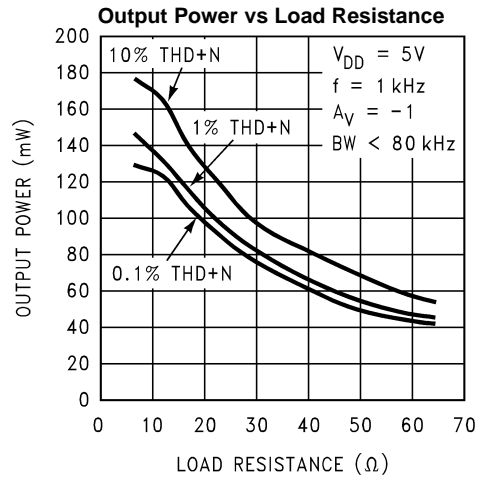


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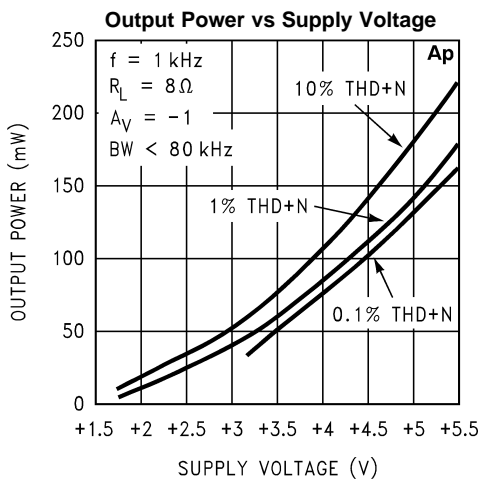


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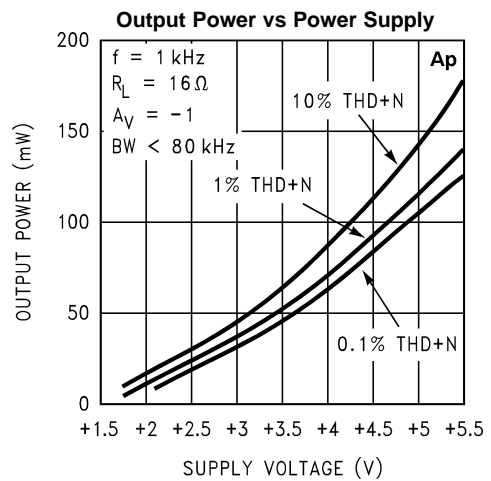


Figure 27.

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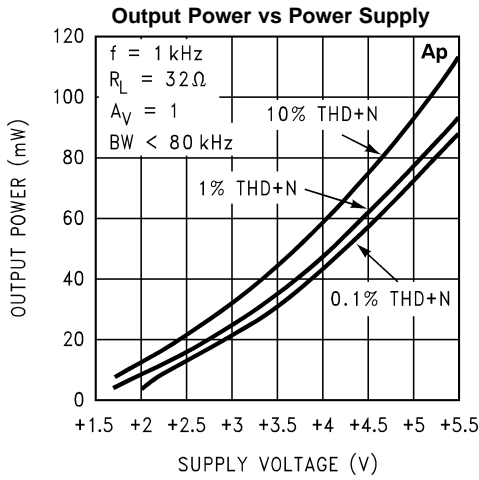


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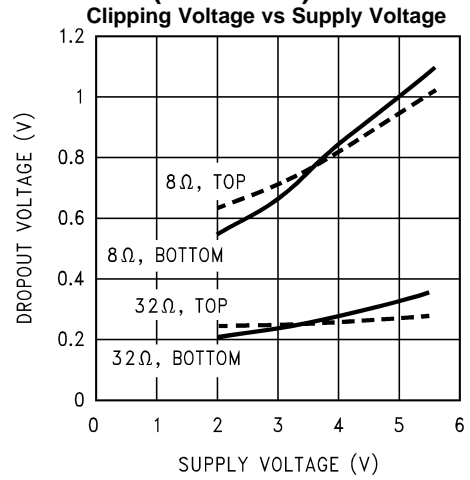


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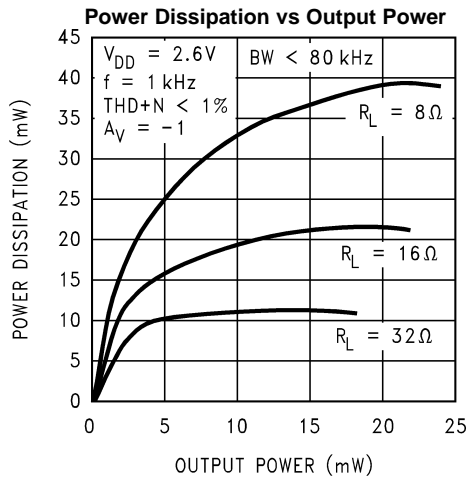


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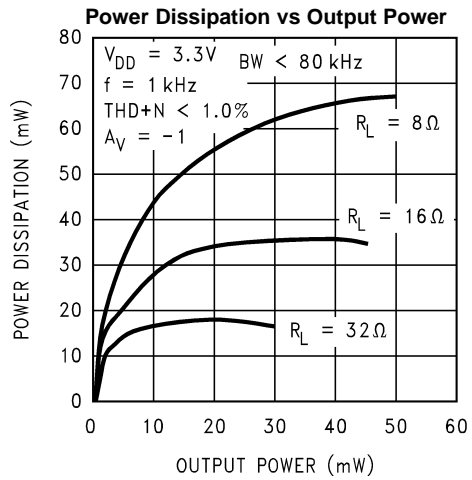


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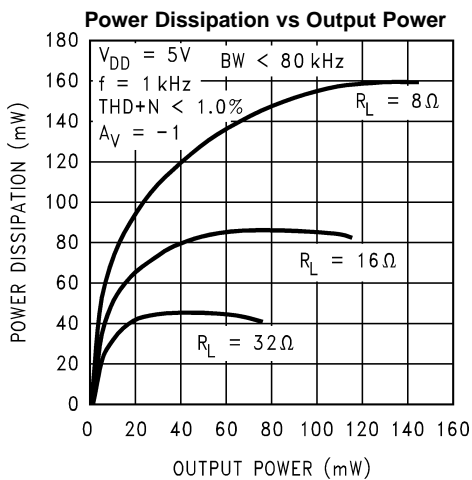


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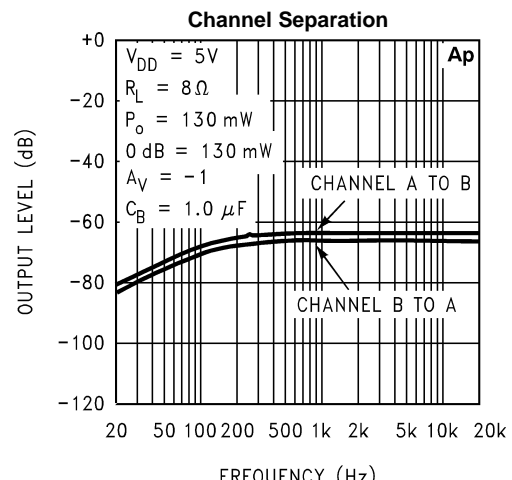


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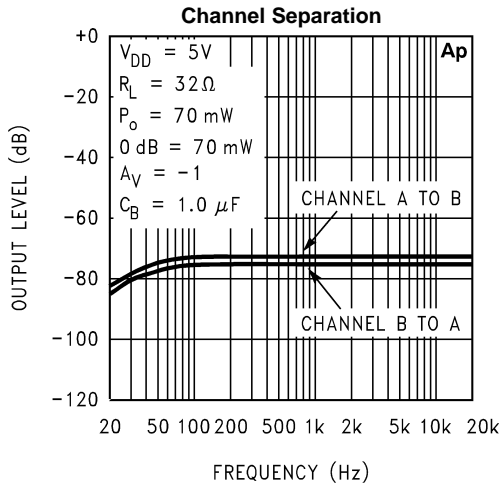


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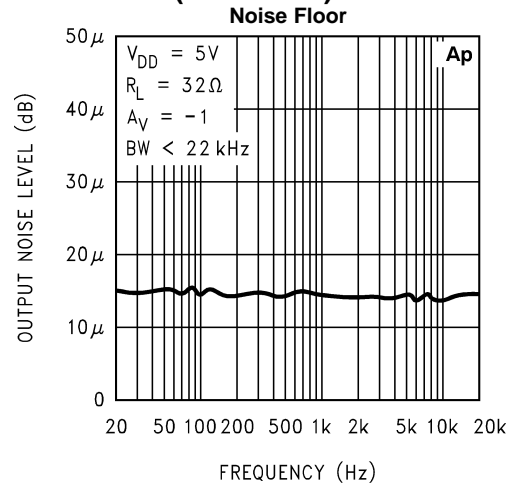


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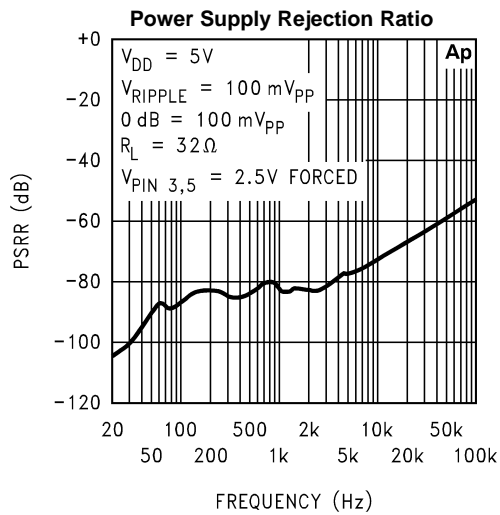


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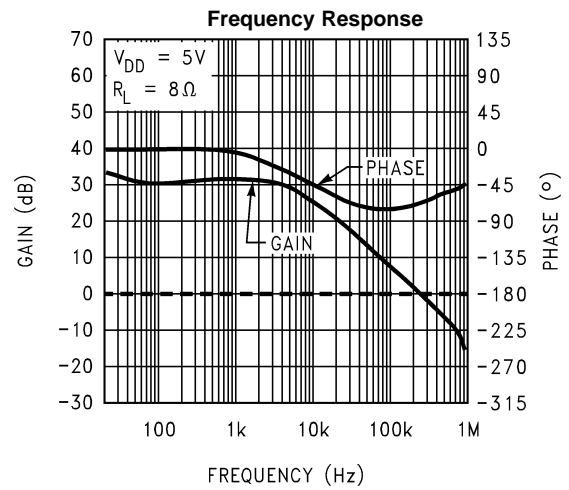


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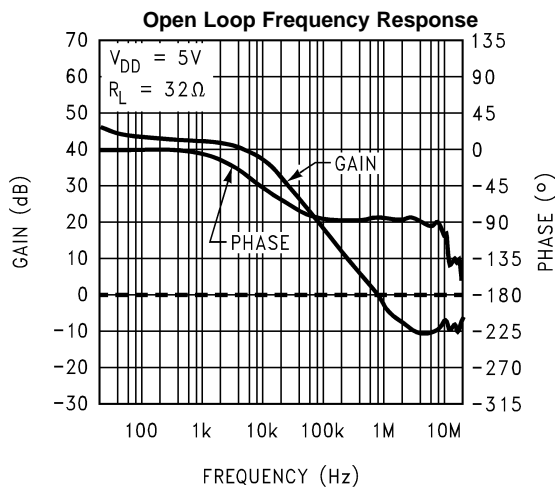


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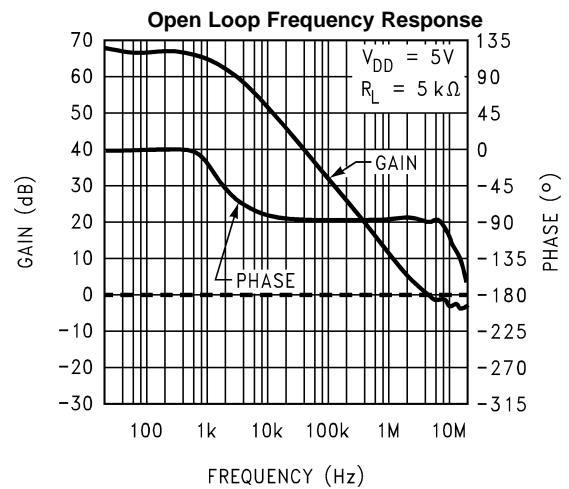


Figure 39.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

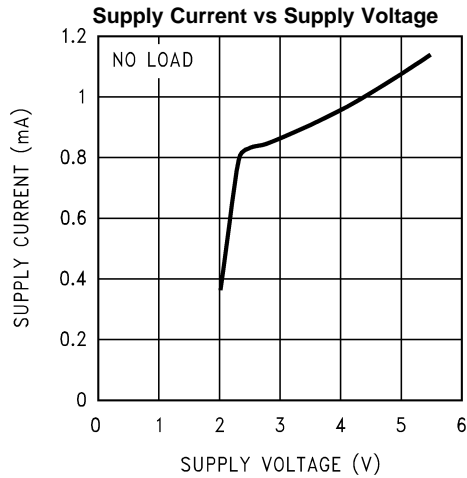


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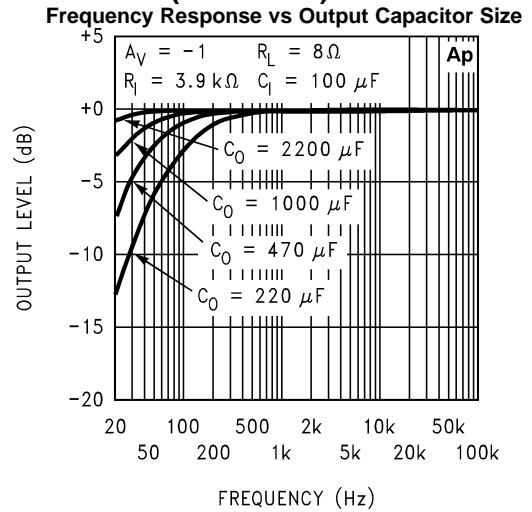


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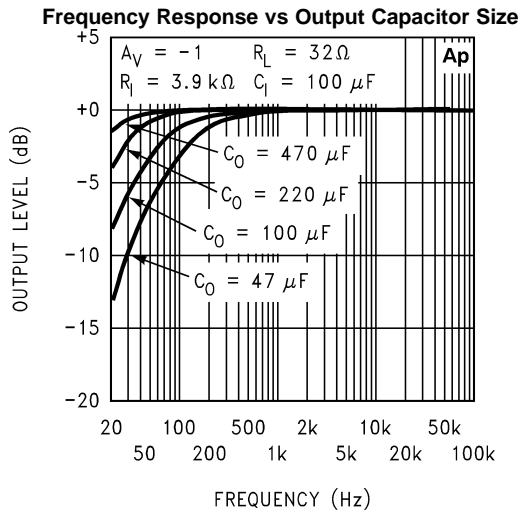


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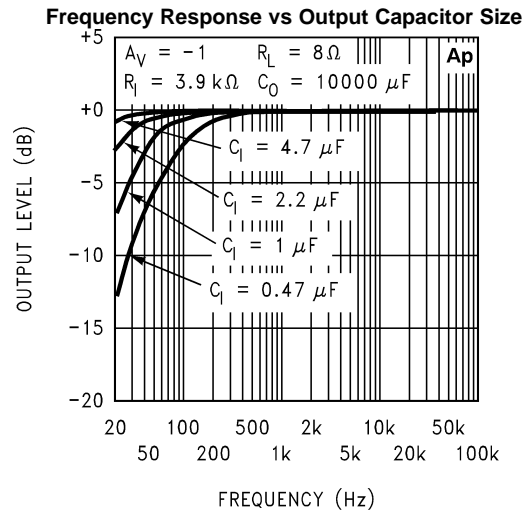


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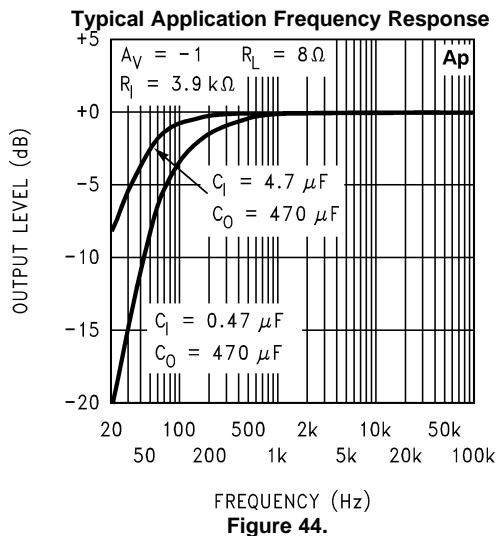


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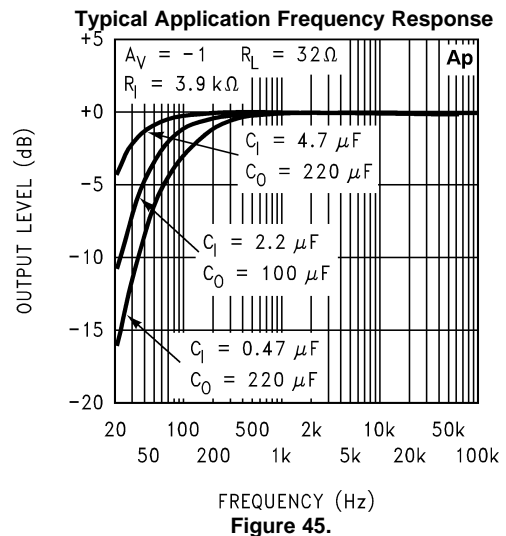


Figure 45.

APPLICATION INFORMATION

EXPOSED-DAP PACKAGE PCB MOUNTING CONSIDERATION

The LM4808's exposed-dap (die attach paddle) package (LD) provides a low thermal resistance between the die and the PCB to which the part is mounted and soldered. This allows rapid heat transfer from the die to the surrounding PCB copper traces, ground plane, and surrounding air.

The LD package should have its DAP soldered to a copper pad on the PCB. The DAP's PCB copper pad may be connected to a large plane of continuous unbroken copper. This plane forms a thermal mass, heat sink, and radiation area.

However, since the LM4808 is designed for headphone applications, connecting a copper plane to the DAP's PCB copper pad is not required. The LM4808's Power Dissipation vs Output Power Curve in the [TYPICAL PERFORMANCE CHARACTERISTICS](#) shows that the maximum power dissipated is just 45mW per amplifier with a 5V power supply and a 32Ω load.

Further detailed and specific information concerning PCB layout, fabrication, and mounting an LD (WSON) package is available from Texas Instruments' Package Engineering Group under application note AN-1187 (literature number [SNOA401](#)).

POWER DISSIPATION

Power dissipation is a major concern when using any power amplifier and must be thoroughly understood to ensure a successful design. [Equation 1](#) states the maximum power dissipation point for a single-ended amplifier operating at a given supply voltage and driving a specified output load.

$$P_{\text{DMAX}} = (V_{\text{DD}})^2 / (2\pi^2 R_L) \quad (1)$$

Since the LM4808 has two operational amplifiers in one package, the maximum internal power dissipation point is twice that of the number which results from [Equation 1](#). Even with the large internal power dissipation, the LM4808 does not require heat sinking over a large range of ambient temperature. From [Equation 1](#), assuming a 5V power supply and a 32Ω load, the maximum power dissipation point is 40mW per amplifier. Thus the maximum package dissipation point is 80mW. The maximum power dissipation point obtained must not be greater than the power dissipation that results from [Equation 2](#):

$$P_{\text{DMAX}} = (T_{\text{JMAX}} - T_A) / \theta_{\text{JA}}$$

where

- $\theta_{\text{JA}} = 210^\circ\text{C/W}$ for package DGK0008A
 - $T_{\text{JMAX}} = 150^\circ\text{C}$ for the LM4808
- (2)

Depending on the ambient temperature, T_A , of the system surroundings, [Equation 2](#) can be used to find the maximum internal power dissipation supported by the IC packaging. If the result of [Equation 1](#) is greater than that of [Equation 2](#), then either the supply voltage must be decreased, the load impedance increased or T_A reduced. For the typical application of a 5V power supply, with a 32Ω load, the maximum ambient temperature possible without violating the maximum junction temperature is approximately 133.2°C provided that device operation is around the maximum power dissipation point. Power dissipation is a function of output power and thus, if typical operation is not around the maximum power dissipation point, the ambient temperature may be increased accordingly. Refer to the [TYPICAL PERFORMANCE CHARACTERISTICS](#) curves for power dissipation information for lower output powers.

POWER SUPPLY BYPASSING

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection. Applications that employ a 5V regulator typically use a 10μF in parallel with a 0.1μF filter capacitors to stabilize the regulator's output, reduce noise on the supply line, and improve the supply's transient response. However, their presence does not eliminate the need for a local 0.1μF supply bypass capacitor, C_S , connected between the LM4808's supply pins and ground. Keep the length of leads and traces that connect capacitors between the LM4808's power supply pin and ground as short as possible. Connecting a 1.0μF capacitor, C_B , between the IN A(+) / IN B(+) node and ground improves the internal bias voltage's stability and improves the amplifier's PSRR. The PSRR improvements increase as the bypass pin capacitor value increases. Too large, however, increases the amplifier's turn-on time. The selection of bypass capacitor values, especially C_B , depends on desired PSRR requirements, click and pop performance (as explained in the section, [SELECTING PROPER EXTERNAL COMPONENTS](#)), system cost, and size constraints.

SELECTING PROPER EXTERNAL COMPONENTS

Optimizing the LM4808's performance requires properly selecting external components. Though the LM4808 operates well when using external components with wide tolerances, best performance is achieved by optimizing component values.

The LM4808 is unity-gain stable, giving a designer maximum design flexibility. The gain should be set to no more than a given application requires. This allows the amplifier to achieve minimum THD+N and maximum signal-to-noise ratio. These parameters are compromised as the closed-loop gain increases. However, low gain demands input signals with greater voltage swings to achieve maximum output power. Fortunately, many signal sources such as audio CODECs have outputs of $1V_{RMS}$ ($2.83V_{P-P}$). Please refer to the [AUDIO POWER AMPLIFIER DESIGN](#) section for more information on selecting the proper gain.

Input and Output Capacitor Value Selection

Amplifying the lowest audio frequencies requires high value input and output coupling capacitors (C_I and C_O in [Figure 1](#)). A high value capacitor can be expensive and may compromise space efficiency in portable designs. In many cases, however, the speakers used in portable systems, whether internal or external, have little ability to reproduce signals below 150Hz. Applications using speakers with this limited frequency response reap little improvement by using high value input and output capacitors.

Besides affecting system cost and size, C_I has an effect on the LM4808's click and pop performance. The magnitude of the pop is directly proportional to the input capacitor's size. Thus, pops can be minimized by selecting an input capacitor value that is no higher than necessary to meet the desired $-3dB$ frequency.

As shown in [Figure 1](#), the input resistor, R_I and the input capacitor, C_I , produce a $-3dB$ high pass filter cutoff frequency that is found using [Equation 3](#). In addition, the output load R_L , and the output capacitor C_O , produce a $-3dB$ high pass filter cutoff frequency defined by [Equation 4](#).

$$f_{i-3db} = 1/2\pi R_I C_I \quad (3)$$

$$f_{o-3db} = 1/2\pi R_L C_O \quad (4)$$

Also, careful consideration must be taken in selecting a certain type of capacitor to be used in the system. Different types of capacitors (tantalum, electrolytic, ceramic) have unique performance characteristics and may affect overall system performance.

Bypass Capacitor Value

Besides minimizing the input capacitor size, careful consideration should be paid to the value of the bypass capacitor, C_B . Since C_B determines how fast the LM4808 settles to quiescent operation, its value is critical when minimizing turn-on pops. The slower the LM4808's outputs ramp to their quiescent DC voltage (nominally $1/2 V_{DD}$), the smaller the turn-on pop. Choosing C_B equal to $1.0\mu F$ or larger, will minimize turn-on pops. As discussed above, choosing C_I no larger than necessary for the desired bandwidth helps minimize clicks and pops.

AUDIO POWER AMPLIFIER DESIGN

Design a Dual 70mW/32Ω Audio Amplifier

Given:

Power Output	70mW
Load Impedance	32Ω
Input Level	1Vrms (max)
Input Impedance	20kΩ
Bandwidth	100Hz–20kHz ± 0.5dB

The design begins by specifying the minimum supply voltage necessary to obtain the specified output power. One way to find the minimum supply voltage is to use the [Output Power vs Supply Voltage](#) curve in the [TYPICAL PERFORMANCE CHARACTERISTICS](#) section. Another way, using [Equation 5](#), is to calculate the peak output voltage necessary to achieve the desired output power for a given load impedance. To account for the amplifier's dropout voltage, two additional voltages, based on the [Dropout Voltage vs Supply Voltage](#) in the [TYPICAL PERFORMANCE CHARACTERISTICS](#) curves, must be added to the result obtained by [Equation 5](#). For a single-ended application, the result is [Equation 6](#).

$$V_{\text{opeak}} = \sqrt{(2R_L P_O)} \quad (5)$$

$$V_{\text{DD}} \geq (2V_{\text{OPEAK}} + (V_{\text{ODTOP}} + V_{\text{ODBOT}})) \quad (6)$$

The [Output Power vs Supply Voltage](#) graph for a 32Ω load indicates a minimum supply voltage of 4.8V. This is easily met by the commonly used 5V supply voltage. The additional voltage creates the benefit of headroom, allowing the LM4808 to produce peak output power in excess of 70mW without clipping or other audible distortion. The choice of supply voltage must also not create a situation that violates maximum power dissipation as explained above in the [POWER DISSIPATION](#) section. Remember that the maximum power dissipation point from [Equation 1](#) must be multiplied by two since there are two independent amplifiers inside the package. Once the power dissipation equations have been addressed, the required gain can be determined from [Equation 7](#).

$$A_V \geq \sqrt{(P_O R_L)} / (V_{\text{IN}}) = V_{\text{orms}} / V_{\text{inrms}} \quad (7)$$

Thus, a minimum gain of 1.497 allows the LM4808 to reach full output swing and maintain low noise and THD+N performance. For this example, let $A_V = 1.5$.

The amplifiers overall gain is set using the input (R_i) and feedback (R_f) resistors. With the desired input impedance set at 20kΩ, the feedback resistor is found using [Equation 8](#).

$$A_V = R_f / R_i \quad (8)$$

The value of R_f is 30kΩ.

The last step in this design is setting the amplifier's –3dB frequency bandwidth. To achieve the desired ±0.25dB pass band magnitude variation limit, the low frequency response must extend to at least one-fifth the lower bandwidth limit and the high frequency response must extend to at least five times the upper bandwidth limit. The gain variation for both response limits is 0.17dB, well within the ±0.25dB desired limit. The results are an

$$f_L = 100\text{Hz} / 5 = 20\text{Hz} \quad (9)$$

and a

$$f_H = 20\text{kHz} * 5 = 100\text{kHz} \quad (10)$$

As stated in the [EXTERNAL COMPONENTS DESCRIPTION](#) section, both R_i in conjunction with C_i , and C_o with R_L , create first order highpass filters. Thus to obtain the desired low frequency response of 100Hz within ±0.5dB, both poles must be taken into consideration. The combination of two single order filters at the same frequency forms a second order response. This results in a signal which is down 0.34dB at five times away from the single order filter –3dB point. Thus, a frequency of 20Hz is used in the following equations to ensure that the response is better than 0.5dB down at 100Hz.

$$C_i \geq 1 / (2\pi * 20 \text{ k}\Omega * 20 \text{ Hz}) = 0.397\mu\text{F}; \text{ use } 0.39\mu\text{F}.$$

$$C_o \geq 1 / (2\pi * 32\Omega * 20 \text{ Hz}) = 249\mu\text{F}; \text{ use } 330\mu\text{F}.$$

The high frequency pole is determined by the product of the desired high frequency pole, f_H , and the closed-loop gain, A_V . With a closed-loop gain of 1.5 and $f_H = 100\text{kHz}$, the resulting $\text{GBWP} = 150\text{kHz}$ which is much smaller than the LM4808's GBWP of 900kHz . This figure displays that if a designer has a need to design an amplifier with a higher gain, the LM4808 can still be used without running into bandwidth limitations.

Demonstration Board Layout

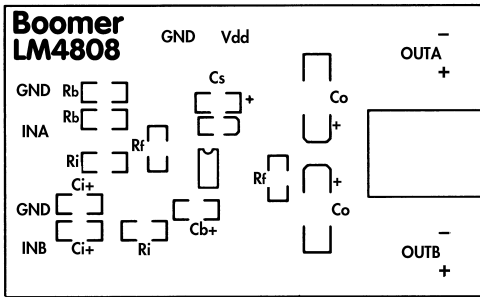


Figure 46. Recommended SO PC Board Layout: Top Silkscreen

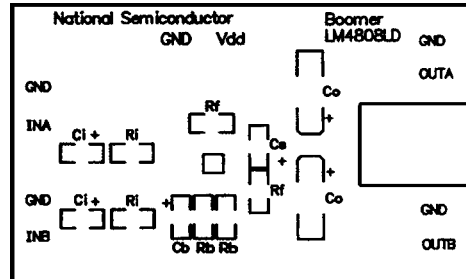


Figure 47. Recommended LD PC Board Layout: Top Silkscreen

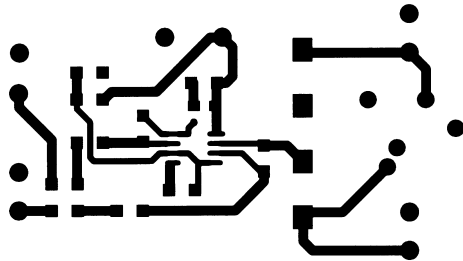


Figure 48. Recommended SOIC PC Board Layout: Top Layer

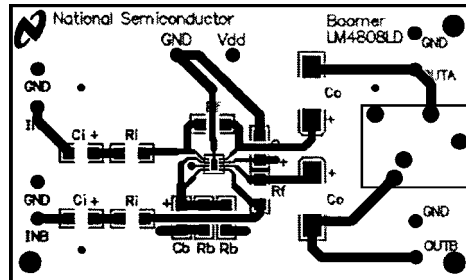


Figure 49. Recommended LD PC Board Layout: Top Layer

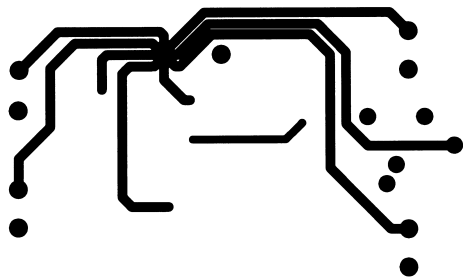


Figure 50. Recommended SOIC PC Board Layout: Bottom Layer

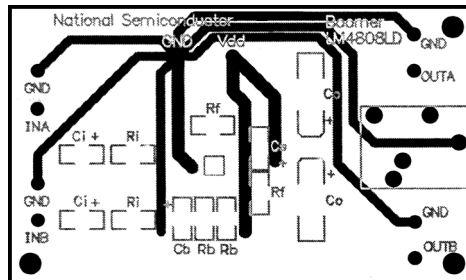


Figure 51. Recommended LD PC Board Layout: Bottom Layer

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
<hr/> <ul style="list-style-type: none">• Changed layout of National Data Sheet to TI format	<hr/> 16

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM4808M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4808M	Samples
LM4808MM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	G08	Samples
LM4808MMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	G08	Samples
LM4808MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM4808M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

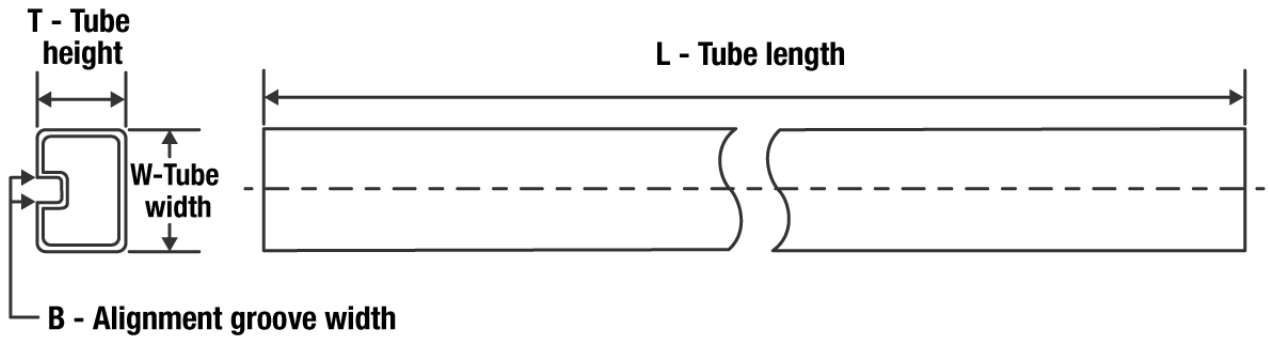

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM4808MM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4808MMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM4808MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM4808MM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM4808MMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LM4808MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LM4808M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LM4808M/NOPB	D	SOIC	8	95	495	8	4064	3.05



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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