CC1175 高性能射频 (RF) 发射器，用于窄带系统

1 器件概述

1.1 特性

- 高性能，单片发射器
  - 极低相位噪声：10kHz 偏移时为 -111dBc/Hz
- 高频谱效率（12.5kHz 信道中为 9.6kbps，符合 FCC 窄带要求）
- 128 字节 TX 先入先出 (FIFO)
- 支持与 CC1190 器件无缝集成以实现范围扩展，从而实现高达 +27dBm 的输出功率
- 步长为 0.4dB 时可编程输出功率高达 +16dBm
- 电源
  - 宽电源电压范围（2.0V 至 3.6V）
  - 低流耗：
    - TX: +14dBm 时为 45mA
  - 断电：0.12μA（定时器运行时为 0.5μA）
- 自动输出功率递增
- 可配置数据速率：0 至 200kbps
- 所支持的调制格式：2 - 频移键控 (FSK)，2 - 高斯频移监控 (GFSK)，4-FSK，4-GFSK，最小频移键控 (MSK)，开关键控 (OOK)
- 符合 RoHS 标准的 5mm × 5mm 无脚四方扁平无引线 (QFN) 32 引脚封装 (RHB)
- 法规 - 适用于符合下列标准的系统
  - 欧洲： ETSI EN 300 220，ETSI EN 54-25
  - 美国： FCC CFR47 部分 15，FCC CFR47 部分 90，24 和 101
  - 日本： ARIB RCR STD-T30，ARIB STD-T67，ARIB STD-T108
- 外设和支持功能
  - TCXO 支持和控制，同样适用于功率模式
  - 用于扩展范围和增强耐用性的可选编码增益特性
  - 温度传感器

1.2 应用

- 信道间隔低至 6.25kHz 的单向窄带超低功率无线系统
- 169、315、433、868、915、920、950MHz ISM/SRD 频带系统
- 无线计量和无线智能电网（自动计量读取 (AMR) 和自动计量基础设施 (AMI)）
- IEEE 802.15.4g 系统
- 家庭和楼宇自动化
- 无线警报和安全系统
- 工业用监控和控制
- 无线医疗应用
- 无线传感器网络和有源射频识别 (RFID)

1.3 说明

CC1175 器件是一款全集成单芯片无线电发射器，此器件设计用于在成本有效无线系统中实现极低功耗和低压运行的高性能。 所有滤波器都已集成，因此无需昂贵的外部表面声波 (SAW) 和中频 (IF) 滤波器。 该器件主要用于 ISM（工业、科学和医疗）以及处于 164-192MHz，274-320MHz，410-480MHz 和 820-960MHz 的 SRD（短程设备）频带。

CC1175 器件提供广泛硬件支持，以实现数据包处理、数据缓冲、突发传输。 CC1175 器件的主要运行参数可由 SPI 接口控制。 在典型系统中，CC1175 器件将与微控制器和极少的外部无源组件配合使用。

器件信息 (1)

部件号	封装	封装尺寸
CC1175RHB	超薄四方扁平无引线 (VQFN) (32)	5.00mm x 5.00mm

(1) 更多信息请参见 节 8，*机械封装和可订购产品信息*

1.4 功能方框图

图 1-1 显示 CC1175 器件的系统方框图。

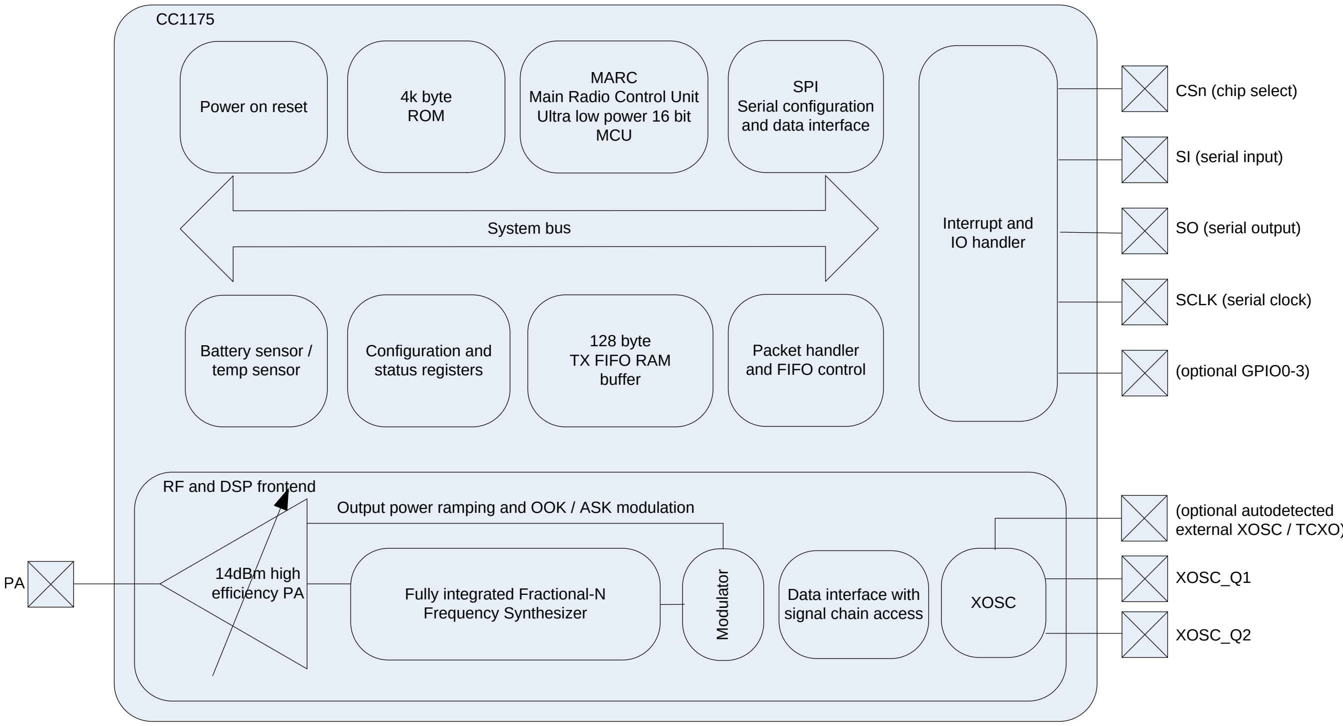


图 **1-1.** 功能方框图

内容

2 修订历史记录

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

本数据手册修订历史记录强调了使 SWRS116E 器件专用数据手册变为 SWRS116F 修订版本所做的更改。

Changes from Revision E (June 2014) to Revision F	Page
• Added Ambient to the temperature range condition and removed Tj from Temperature range	7
• Added data to TCXO table	13

3 Terminal Configuration and Functions

3.1 Pin Diagram

Figure 3-1 shows pin names and locations for the CC1175 device.

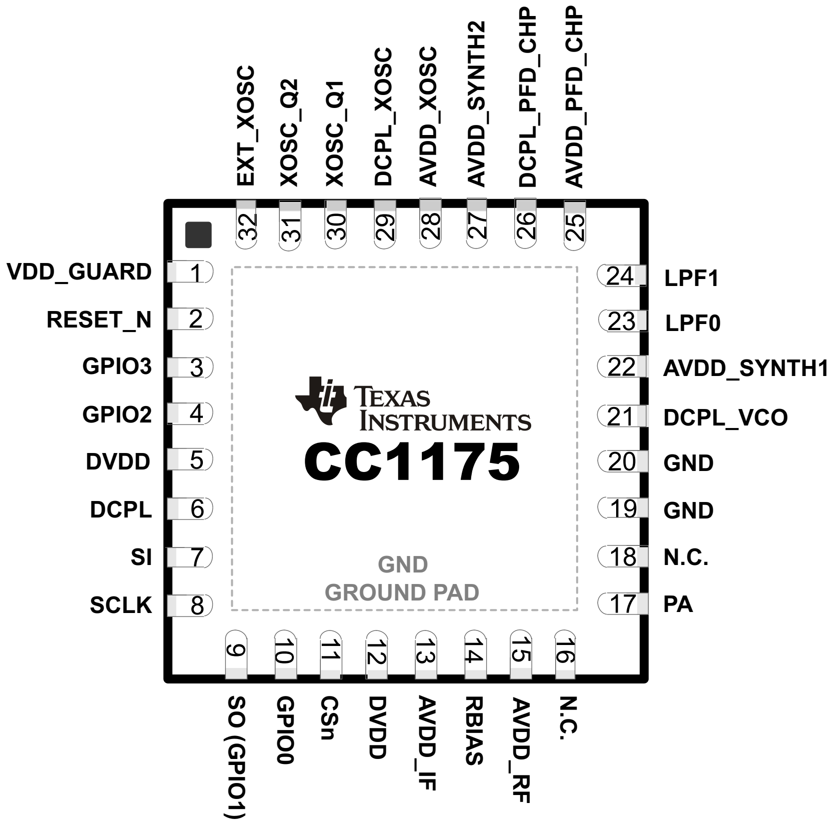


Figure 3-1. Package 5-mm × 5-mm QFN

3.2 Pin Configuration

The following table lists the pin-out configuration for the CC1175 device.

PIN NO.	PIN NAME	TYPE / DIRECTION	DESCRIPTION
1	VDD_GUARD	Power	2.0–3.6 V VDD
2	RESET_N	Digital input	Asynchronous, active-low digital reset
3	GPIO3	Digital I/O	General-purpose I/O
4	GPIO2	Digital I/O	General-purpose I/O
5	DVDD	Power	2.0–3.6 VDD to internal digital regulator
6	DCPL	Power	Digital regulator output to external decoupling capacitor
7	SI	Digital input	Serial data in
8	SCLK	Digital input	Serial data clock
9	SO(GPIO1)	Digital I/O	Serial data out (general-purpose I/O)
10	GPIO0	Digital I/O	General-purpose I/O
11	CSn	Digital input	Active-low chip select
12	DVDD	Power	2.0–3.6 V VDD
13	AVDD_IF	Power	2.0–3.6 V VDD
14	RBIAS	Analog	External high-precision resistor
15	AVDD_RF	Power	2.0–3.6 V VDD
16	N.C.		Not connected
17	PA	Analog	Single-ended TX output (requires DC path to VDD)
18	N.C.		Not connected
19	GND1	Analog	Analog ground
20	GND0	Analog	Analog ground
21	DCPL_VCO	Power	Pin for external decoupling of VCO supply regulator
22	AVDD_SYNTH1	Power	2.0–3.6 V VDD
23	LPF0	Analog	External loop filter components
24	LPF1	Analog	External loop filter components
25	AVDD_PFD_CHP	Power	2.0–3.6 V VDD
26	DCPL_PFD_CHP	Power	Pin for external decoupling of PFD and CHP regulator
27	AVDD_SYNTH2	Power	2.0–3.6 V VDD
28	AVDD_XOSC	Power	2.0–3.6 V VDD
29	DCPL_XOSC	Power	Pin for external decoupling of XOSC supply regulator
30	XOSC_Q1	Analog	Crystal oscillator pin 1 (must be grounded if a TCXO or other external clock connected to EXT_XOSC is used)
31	XOSC_Q2	Analog	Crystal oscillator pin 2 (must be left floating if a TCXO or other external clock connected to EXT_XOSC is used)
32	EXT_XOSC	Digital input	Pin for external clock input (must be grounded if a regular crystal connected to XOSC_Q1 and XOSC_Q2 is used)
–	GND	Ground pad	The ground pad must be connected to a solid ground plane.

4 Specifications

All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1, or CC1120EM_169 rev.1.2.

4.1 Absolute Maximum Ratings[(1)(2)]

PARAMETER	MIN	MAX	UNIT	CONDITION
Supply voltage (VDD, AVDD_x)	–0.3	3.9	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3	V	max 3.9
Voltage on analog pins (including DCPL pins)	–0.3	2.0	V	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under general characteristics is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.

4.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–40	125	°C
V_{ESD}	Electrostatic discharge (ESD) performance:	Human body model (HBM), per ANSI/ESDA/JEDEC JS001[(1)]		–2	2	kV
		Charged device model (CDM), per JESD22-C101[(2)]	All pins	–500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V HBM allows safe manufacturing with a standard ESD control process.

4.3 Recommended Operating Conditions (General Characteristics)

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Voltage supply range	2.0		3.6	V	All supply pins must have the same voltage
Voltage on digital inputs	0		VDD	V	
Temperature range	–40		85	°C	Ambient

4.4 Thermal Resistance Characteristics for RHB Package

		°C/W[(1)]	AIR FLOW (m/s)[(2)]
$R\theta_{JC}$	Junction-to-case (top)	21.1	0.00
$R\theta_{JB}$	Junction-to-board	5.3	0.00
$R\theta_{JA}$	Junction-to-free air	31.3	0.00
Psi_{JT}	Junction-to-package top	0.2	0.00
Psi_{JB}	Junction-to-board	5.3	0.00
$R\theta_{JC}$	Junction-to-case (bottom)	0.8	0.00

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

Power dissipation of 40 mW and an ambient temperature of 25ºC is assumed.
(2) m/s = meters per second

4.5 RF Characteristics

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Frequency bands	820		960	MHz	
	410		480	MHz	
	(273.3)		(320)	MHz	For more information, see SWRA398, *Using the CC112x/CC1175 at 274 to 320 MHz.*
	164		192	MHz	
	(205)		(240)	MHz	Contact TI for more information about the use of these frequency bands.
	(136.7)		(160)	MHz	
Frequency resolution		30		Hz	In 820– to 960–MHz band
		15		Hz	In 410– to 480–MHz band
		6		Hz	In 164– to 192–MHz band
Data rate	0		200	kbps	Packet mode
	0		100	kbps	Transparent mode
Data rate step size		1e-4		bps	

4.6 Regulatory Standards

PERFORMANCE MODE	FREQUENCY BAND	SUITABLE FOR COMPLIANCE WITH	COMMENTS
High-performance mode	820–960 MHz	ARIB T-108 ARIB T-96 ETSI EN 300 220 ETSI EN 54-25 FCC Part 101 FCC Part 24 Submask D FCC Part 15.247 FCC Part 15.249 FCC Part 90 Mask G FCC Part 90 Mask J	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender such as the CC1190 device
	410–480 MHz	ARIB T-67 ARIB RCR STD-30 ETSI EN 300 220 FCC Part 90 Mask D FCC Part 90 Mask G	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
	164–192 MHz	ETSI EN 300 220 FCC Part 90 Mask D	Performance also suitable for systems targeting maximum allowed output power in the respective bands, using a range extender
Low-power mode	820–960 MHz	ETSI EN 300 220 FCC Part 15.247 FCC Part 15.249	
	410–480 MHz	ETSI EN 300 220	
	164–192 MHz	ETSI EN 300 220	

4.7 Current Consumption, Static Modes

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Power down with retention		0.12	1	µA	
		0.5		µA	Low-power RC oscillator running
XOFF mode		170		µA	Crystal oscillator / TCXO disabled
IDLE mode		1.3		mA	Clock running, system waiting with no radio activity

4.8 Current Consumption, Transmit Modes

4.8.1 950-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +10 dBm		37		mA	
TX current consumption 0 dBm		26		mA	

4.8.2 868-, 915-, and 920-MHz Bands (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +14 dBm		45		mA	
TX current consumption +10 dBm		34		mA	

4.8.3 434-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +15 dBm		50		mA	
TX current consumption +14 dBm		45		mA	
TX current consumption +10 dBm		34		mA	

4.8.4 169-MHz Band (High-Performance Mode)

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +15 dBm		54		mA	
TX current consumption +14 dBm		49		mA	
TX current consumption +10 dBm		41		mA	

4.8.5 Low-Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
TX current consumption +10 dBm		32		mA	

4.9 Transmit Parameters

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Max output power		+12		dBm	At 950 MHz
		+14		dBm	At 915 and 920 MHz
		+15		dBm	At 915 and 920 MHz with VDD = 3.6 V
		+15		dBm	At 868 MHz
		+16		dBm	At 868 MHz with VDD = 3.6 V
		+15		dBm	At 433 MHz
		+16		dBm	At 433 MHz with VDD = 3.6 V
		+15		dBm	At 169 MHz
		+16		dBm	At 169 MHz with VDD = 3.6 V
Min output power		–11		dBm	Within fine step size range
		–40		dBm	Within coarse step size range
Output power step size		0.4		dB	Within fine step size range
Adjacent channel power		–75		dBc	4-GFSK 9.6 kbps in 12.5-kHz channel, measured in 100-Hz bandwidth at 434 MHz (FCC Part 90 Mask D compliant)
		–58		dBc	4-GFSK 9.6 kbps in 12.5-kHz channel, measured in 8.75-kHz bandwidth (ETSI–300 220 compliant)
		–61		dBc	2-GFSK 2.4 kbps in 12.5-kHz channel, 1.2-kHz deviation
Spurious emissions (Not including harmonics)		<–60		dBm	
Harmonics					Transmission at +14 dBm (or maximum allowed in applicable band where this is less than +14 dBm) using TI reference design Emissions measured according to ARIB T-96 in 950-MHz band, ETSI EN 300 220 in 169-, 433-, and 868-MHz bands and FCC Part 15.247 in 450- and 915-MHz band Fourth harmonic in 915-MHz band will require extra filtering to meet FCC requirements if transmitting for long intervals (>50-ms periods).
Second Harm, 169 MHz		–39		dBm	
Third Harm, 169 MHz		–58		dBm	
Second Harm, 433 MHz		–56		dBm	
Third Harm, 433 MHz		–51		dBm	
Second Harm, 450 MHz		–60		dBm	
Third Harm, 450 MHz		–45		dBm	
Second Harm, 868 MHz		–40		dBm	
Third Harm, 868 MHz		–42		dBm	
Second Harm, 915 MHz		56		dBuV/m	
Third Harm, 915 MHz		52		dBuV/m	
Fourth Harm, 915 MHz		60		dBuV/m	
Second Harm, 950 MHz		–58		dBm	
Third Harm, 950 MHz		–42		dBm	
Optimum load impedance					
868-, 915-, and 920-MHz bands		35 + j35		Ω	
433-MHz band		55 + j25		Ω	
169-MHz band		80 + j0		Ω	

4.10 PLL Parameters

4.10.1 High-Performance Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Phase noise in 950-MHz band		–99		dBc/Hz	± 10 kHz offset
		–99		dBc/Hz	± 100 kHz offset
		–123		dBc/Hz	± 1 MHz offset
Phase noise in 868-, 915-, and 920-MHz bands		–99		dBc/Hz	± 10 kHz offset
		–100		dBc/Hz	± 100 kHz offset
		–122		dBc/Hz	± 1 MHz offset
Phase noise in 433-MHz band		–106		dBc/Hz	± 10 kHz offset
		–107		dBc/Hz	± 100 kHz offset
		–127		dBc/Hz	± 1 MHz offset
Phase noise in 169-MHz band		–111		dBc/Hz	± 10 kHz offset
		–116		dBc/Hz	± 100 kHz offset
		–135		dBc/Hz	± 1 MHz offset

4.10.2 Low-Power Mode

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Phase noise in 950-MHz band		–90		dBc/Hz	± 10 kHz offset
		–92		dBc/Hz	± 100 kHz offset
		–124		dBc/Hz	± 1 MHz offset
Phase noise in 868- and 915-MHz bands		–95		dBc/Hz	± 10 kHz offset
		–95		dBc/Hz	± 100 kHz offset
		–124		dBc/Hz	± 1 MHz offset
Phase noise in 433-MHz band		–98		dBc/Hz	± 10 kHz offset
		–102		dBc/Hz	± 100 kHz offset
		–129		dBc/Hz	± 1 MHz offset
Phase noise in 169-MHz band		–106		dBc/Hz	± 10 kHz offset
		–110		dBc/Hz	± 100 kHz offset
		–136		dBc/Hz	± 1 MHz offset

4.11 Wake-up and Timing

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Powerdown to IDLE		0.4		ms	Depends on crystal
IDLE to TX		166		µs	Calibration disabled
		461		µs	Calibration enabled
TX to IDLE time		296		µs	Calibrate when leaving TX enabled
		0		µs	Calibrate when leaving TX disabled
Frequency synthesizer calibration		391		µs	When using SCAL strobe

4.12 High-Speed Crystal Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Crystal frequency	32		44	MHz	It is expected that there will be an increase in spurious emissions when the RF channel is close to multiples of XOSC in TX. We recommend that the level of spurious emissions be evaluated if the RF channel is closer than 1 MHz to multiples of XOSC in TX.
Load capacitance (C_L)		10		pF	
ESR			60	Ω	Simulated over operating conditions
Start-up time		0.4		ms	Depends on crystal

4.13 High-Speed Clock Input (TCXO)

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Clock frequency	32		44	MHz	
TCXO with CMOS output					TCXO with CMOS output directly coupled to pin EXT_OSC
High input voltage	1.4		VDD	V	
Low input voltage	0		0.6	V	
Rise / Fall time			2	ns	
Clipped sine output					TCXO clipped sine output connected to pin EXT_OSC through series capacitor
Clock input amplitude (peak-to-peak)	0.8		1.5	V	

4.14 32-kHz Clock Input

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Clock frequency		32		kHz	
32 kHz clock input pin input high voltage	0.8×VDD			V	
32 kHz clock input pin input low voltage			0.2×VDD	V	

4.15 Low-Speed RC Oscillator

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Frequency		32/40		kHz	After calibration (calibrated against the high-speed XOSC)
Frequency accuracy after calibration		±0.1		%	Relative to frequency reference (for example, 32-MHz crystal or TCXO)
Initial calibration time		1.6		ms	

4.16 I/O and Reset

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Logic input high voltage	0.8×VDD			V	
Logic input low voltage			0.2×VDD	V	
Logic output high voltage	0.8×VDD			V	At 4-mA output load or less
Logic output low voltage			0.2×VDD	V	At 4-mA output load or less
Power-on reset threshold		1.3		V	Voltage on DVDD pin

4.17 Temperature Sensor

T_A = 25°C, VDD = 3.0 V if nothing else is stated

PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
Temperature sensor range	–40		85	°C	
Temperature coefficient		2.66		mV / °C	Change in sensor output voltage versus change in temperature
Typical output voltage		794		mV	Typical sensor output voltage at T_A = 25°C, VDD = 3.0 V
VDD coefficient		1.17		mV / V	Change in sensor output voltage versus change in VDD

The CC1175 device can be configured to provide a voltage proportional to temperature on GPIO1. The temperature can be estimated by measuring this voltage (see Section 4.17). For more information, see the temperature sensor design note (SWRA415).

4.18 Typical Characteristics

T_A = 25°C, VDD = 3.0 V, f_c = 869.5 MHz if nothing else is stated.

All measurements performed on CC1120EM_868_915 rev.1.0.1, CC1120EM_955 rev.1.2.1, CC1120EM_420_470 rev.1.0.1 or CC1120EM_169 rev.1.2 (fxosc = 32 MHz), and CC1125EM_868_915 rev.1.1.0, CC1125EM_420_470 rev.1.1.0, CC1125EM_169 rev.1.1.0, CC1125EM-Cat1-868 (fxosc = 40 MHz).

Figure 4-6 was measured at the 50-Ω antenna connector.

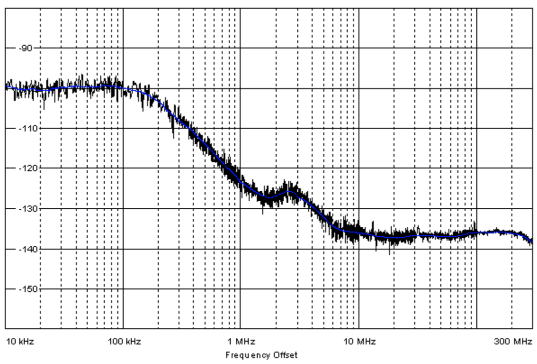


Figure 4-1. Phase Noise in 868-MHz Band

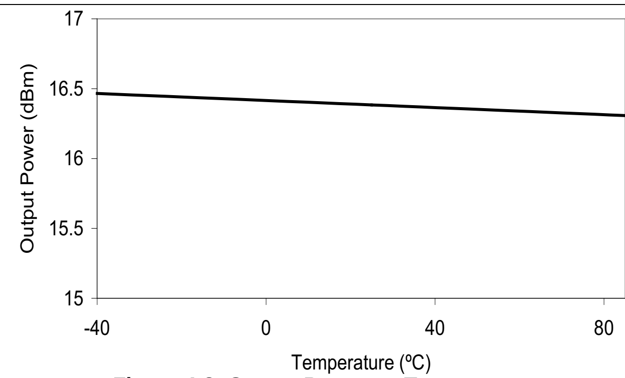


Figure 4-2. Output Power vs Temperature Max Setting, 170 MHz, 3.6 V

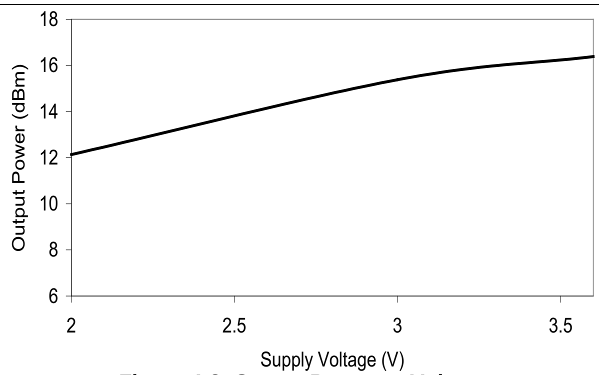


Figure 4-3. Output Power vs Voltage Max Setting, 170 MHz

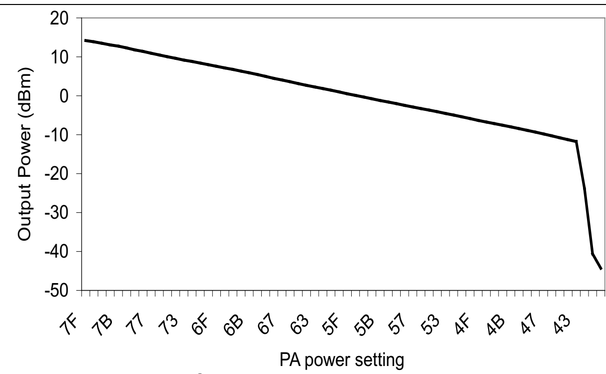


Figure 4-4. Output Power vs PA Power Setting

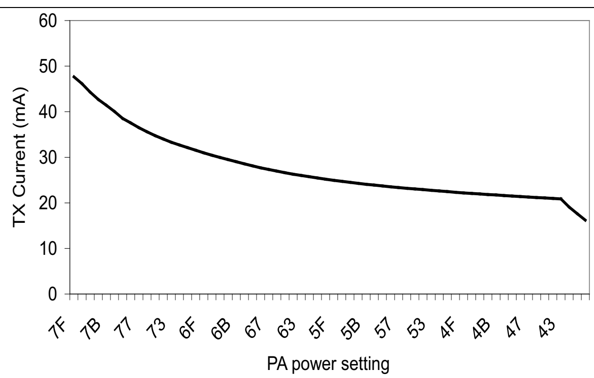


Figure 4-5. TX Current at 868 MHz vs PA Power Setting

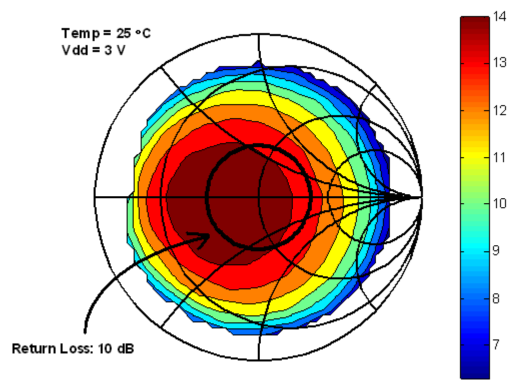
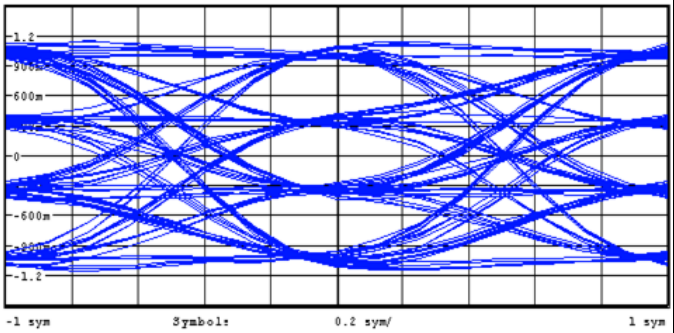
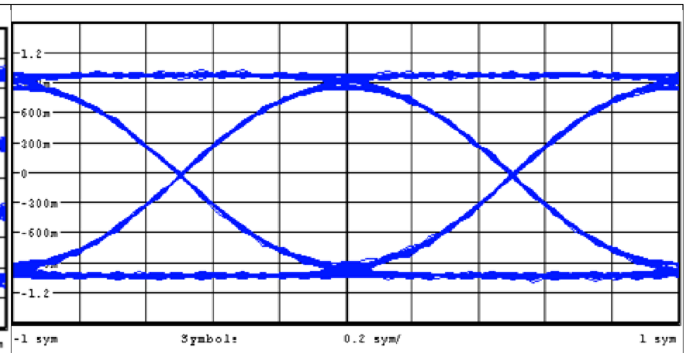


Figure 4-6. Output Power vs Load Impedance (+14-dBm Setting)

Typical Characteristics *(continued)*



200 kbps, DEV = 83 kHz (Outer Symbols), 4GFSK
Figure 4-7. Eye Diagram



1.2 kbps, 2-FSK, DEV = 4 kHz
Figure 4-8. Eye Diagram

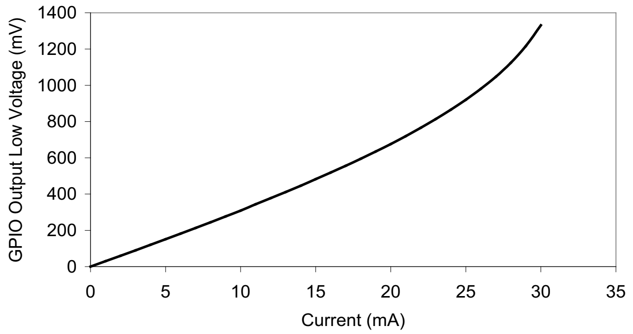


Figure 4-9. GPIO Output Low Voltage vs Current Being Sinked

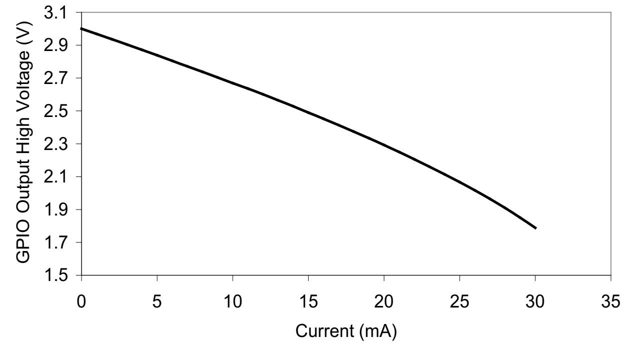
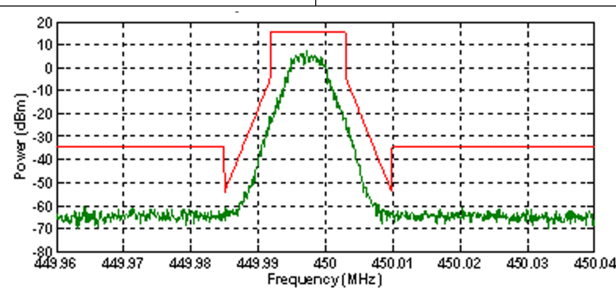


Figure 4-10. GPIO Output High Voltage vs Current Being Sourced



9.6 kbps in 12.5-kHz Channel
Figure 4-11. FCC Part 90 Mask D

5 Detailed Description

5.1 Block Diagram

Figure 5-1 shows the system block diagram of the CC1175 device.

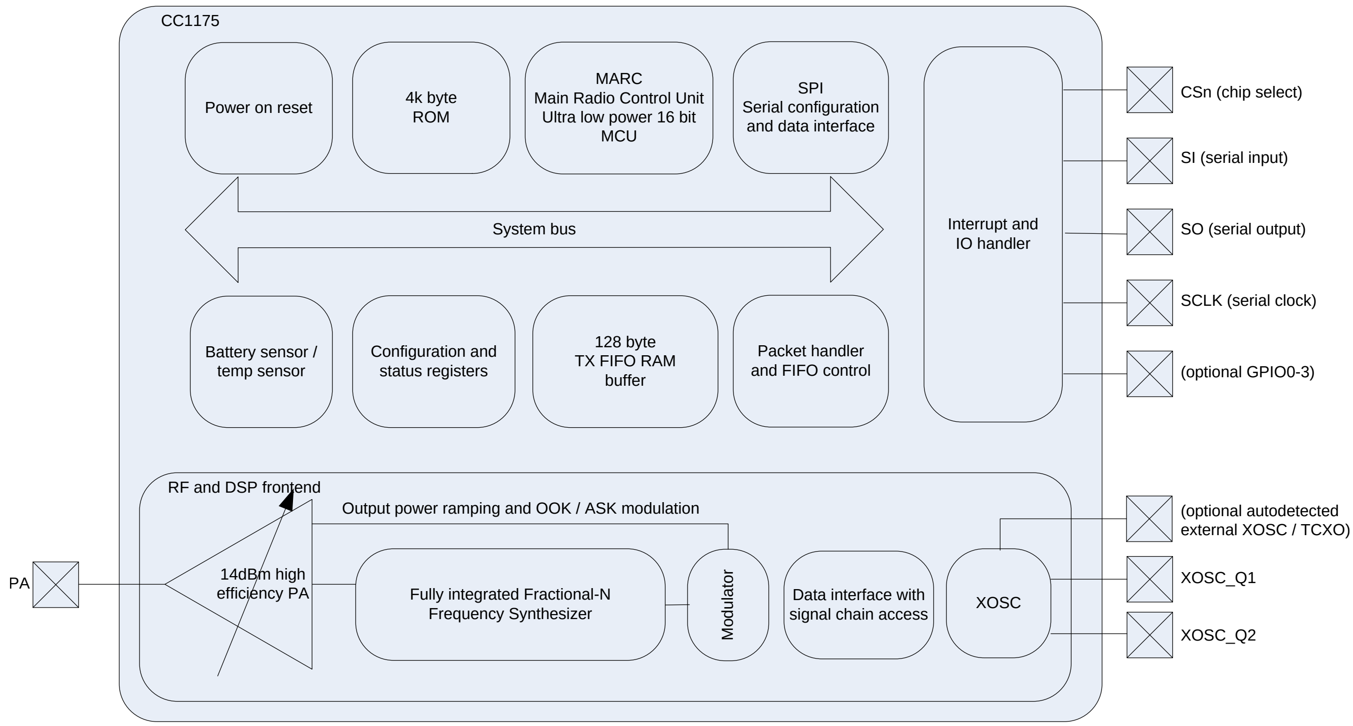


Figure 5-1. System Block Diagram

5.2 Frequency Synthesizer

At the center of the CC1175 device there is a fully integrated, fractional-N, ultra-high-performance frequency synthesizer. The frequency synthesizer is designed for excellent phase noise performance. The system is designed to comply with the most stringent regulatory spectral masks at maximum transmit power.

Either a crystal can be connected to XOSC_Q1 and XOSC_Q2, or a TCXO can be connected to the EXT_XOSC input. The oscillator generates the reference frequency for the synthesizer, as well as clocks for the digital part. If a TCXO is used, the CC1175 device automatically turns on and off the TCXO when needed to support low-power modes.

5.3 Transmitter

The CC1175 transmitter is based on direct synthesis of the RF frequency (in-loop modulation). To achieve effective spectrum usage, the CC1175 device has extensive data filtering and shaping in TX mode to support high throughput data communication in narrowband channels. The modulator also controls power ramping to remove issues such as spectral splattering when driving external high-power RF amplifiers.

The modulator also controls the PA power level to support on/off keying (OOK) and amplitude shift keying (ASK).

5.4 Radio Control and User Interface

The CC1175 digital control system is built around the main radio control (MARC), which is implemented using an internal high-performance, 16-bit ultra-low-power processor. MARC handles power modes, radio sequencing, and protocol timing.

A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering. The host MCU can stay in power-down mode until a valid RF packet is received. This greatly reduces power consumption. When the host MCU receives a valid RF packet, it burst-reads the data. This reduces the required computing power.

The CC1175 radio control and user interface are based on the widely used CC1101 transceiver. This relationship enables an easy transition between the two platforms. The command strobes and the main radio states are the same for the two platforms.

For legacy formats, the CC1175 device also supports two serial modes.

- Synchronous serial mode: The CC1175 device provides the MCU with a bit clock for sampling input data.
- Transparent mode: The CC1175 device samples the input pin at a configurable rate.

5.5 Low-Power and High-Performance Modes

The CC1175 device is highly configurable, enabling trade-offs between power and performance to be made based on the needs of the application. This data sheet describes two modes, low-power mode and high-performance mode, which represent configurations where the device is optimized for either power or performance.

6 Typical Application Circuit

NOTE

This section is intended only as an introduction.

Very few external components are required for the operation of the CC1175 device. Figure 6-1 shows a typical application circuit. The board layout will greatly influence the RF performance of the CC1175 device. Figure 6-1 does not show decoupling capacitors for power pins.

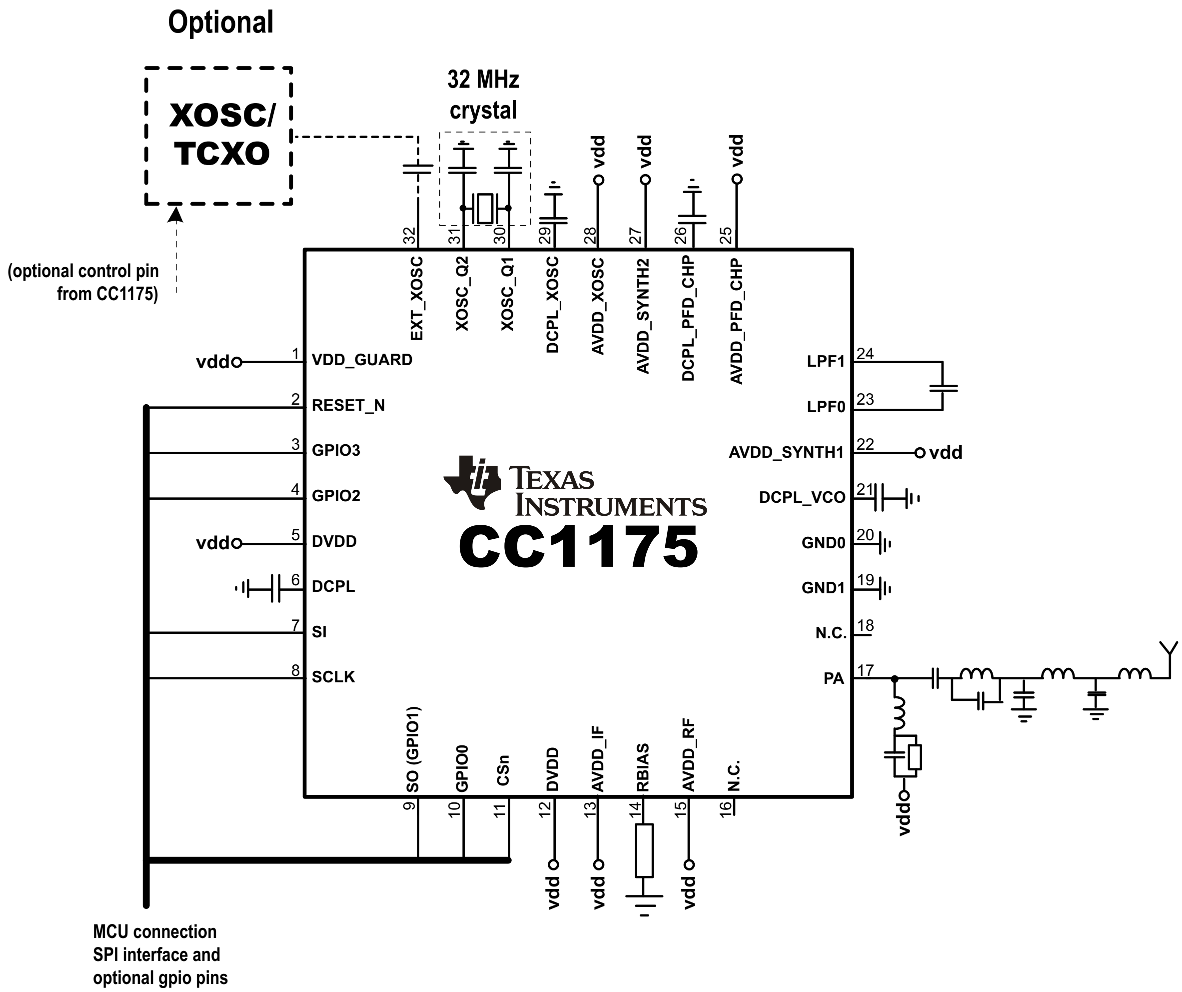


Figure 6-1. Typical Application Circuit

For more information, see the reference designs available for the CC1175 device in 节 7.2, *Documentation Support*.

7 器件和文档支持

7.1 器件支持

7.1.1 开发支持

7.1.1.1 配置软件

CC1175 器件可使用 SmartRF Studio 软件 (SWRC046) 进行配置。 强烈建议使用 SmartRF™ Studio 软件来获取最优寄存器设置并评估相关性能和功能。

7.1.2 器件和支持开发工具命名规则

为了指出产品开发周期所处的阶段，TI 为所有微处理器 (MPU) 和支持工具的产品型号分配了前缀。 每个器件都具有以下三个前缀中的一个：X、P 或无（无前缀）（例如，CC1175）。 德州仪器 (TI) 建议为其支持的工具使用三个可用前缀指示符中的两个：TMDX 和 TMDS。 这些前缀代表了产品开发的发展阶段，即从工程原型 (TMDX) 直到完全合格的生产器件和工具 (TMDS)。

器件开发进化流程：

X 试验器件不一定代表最终器件的电气规范标准并且不可使用生产组装流程。

P 原型器件不一定是最终芯片模型并且不一定符合最终电气标准规范。

无 完全合格的芯片模型的生产版本。

支持工具开发发展流程：

TMDX 还未经德州仪器 (TI) 完整内部质量测试的开发支持产品。

TMDS 完全合格的开发支持产品.

X 和 P 器件和 TMDX 开发支持工具在供货时附带如下免责条款：

“开发的产品用于内部评估用途。”

生产器件和 TMDS 开发支持工具已进行完全特性描述，并且器件的质量和可靠性已经完全论证。 TI 的标准保修证书适用。

预测显示原型器件（X 或者 P）的故障率大于标准生产器件。 由于它们的预计的最终使用故障率仍未定义，德州仪器 (TI) 建议不要将这些器件用于任何生产系统。 只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。 这个后缀表示封装类型（例如，RHB），且温度范围（例如，“空白”是默认的商业级温度范围）提供了读取任一 CC1175 器件完整器件名称的图例。

要获得 QFN 封装类型的 CC1175 器件订购部件号，请参见本文档的“封装选项附录”（TI 网站 www.ti.com），或者联系您的 TI 销售代表。

7.2 文档支持

以下文档对 CC1175 处理器加以补充。 www.ti.com 网站上提供了这些文档的副本。 *提示：*请在 www.ti.com 上提供的搜索框中输入文献编号。

SWRR093 CC1175EM 868MHz 至 915MHz 参考设计

7.3 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

TI E2E™ 在线社区 ***TI 工程师对工程师 (E2E) 社区。*** 此社区的创建目的是为了促进工程师之间协作。 在 e2e.ti.com 中，您可以咨询问题、共享知识、探索思路，在同领域工程师的帮助下解决问题。

德州仪器 **(TI)** 嵌入式处理器维基网站 *德州仪器* ***(TI)*** *嵌入式处理器维基网站。* 此网站的建立是为了帮助开发人员从德州仪器 (TI) 的嵌入式处理器入门并且也为了促进与这些器件相关的硬件和软件的总体知识的创新和增长。

7.4 商标

SmartRF, E2E are trademarks of Texas Instruments.

7.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 术语表

SLYZ022 — *TI 术语表。*

这份术语表列出并解释术语、首字母缩略词和定义。

8 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CC1175RHBR	ACTIVE	VQFN	RHB	32	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1175	Samples
CC1175RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-3-260C-168 HR	-40 to 85	CC1175	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

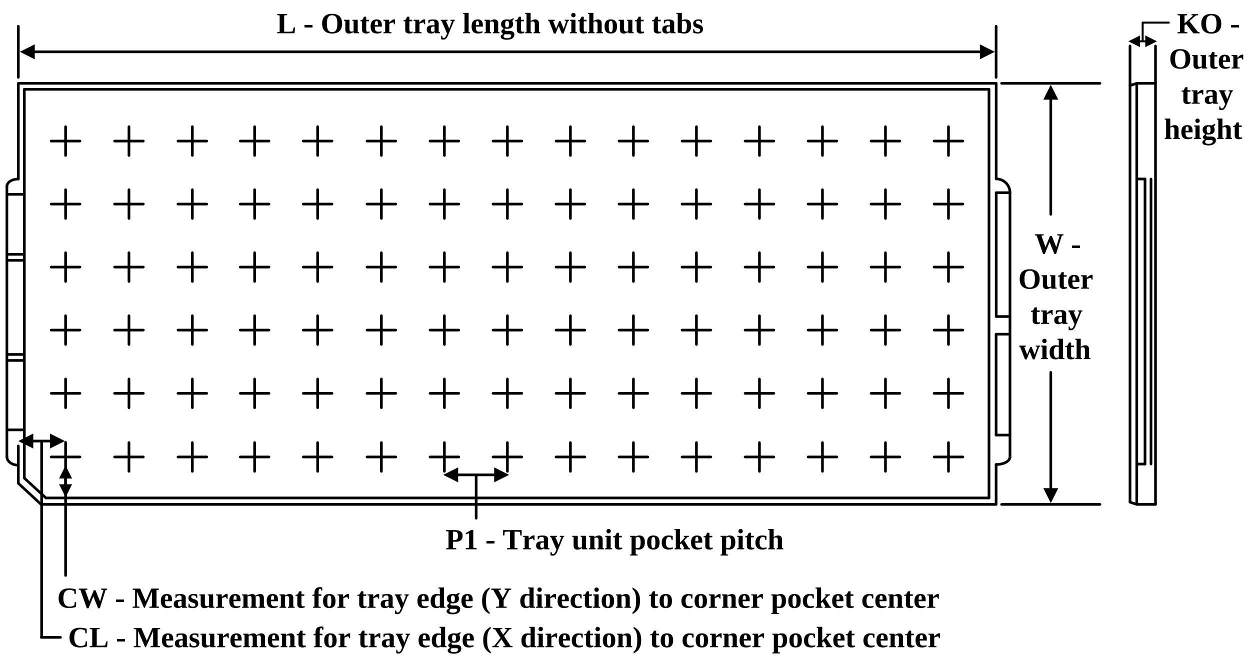
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

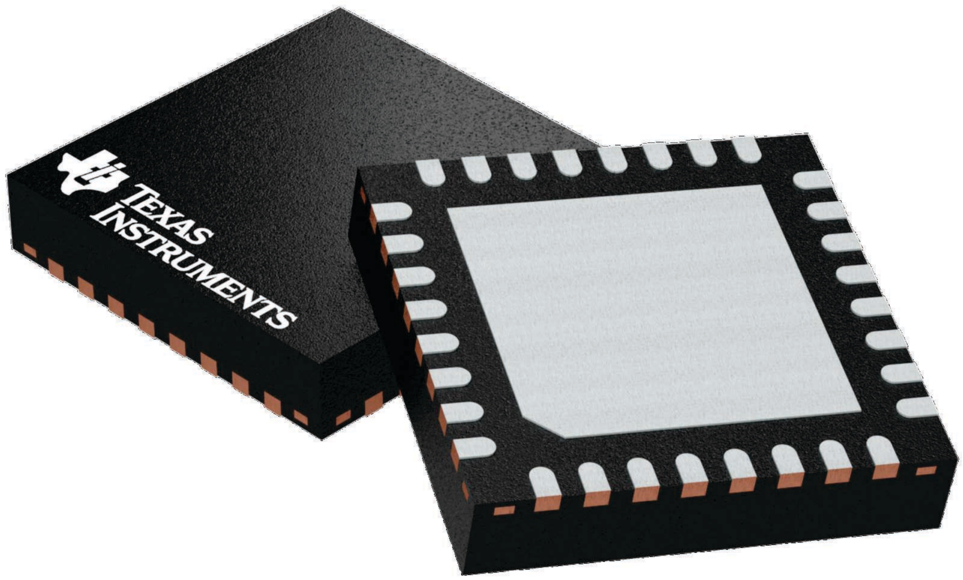
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
CC1175RHBR	RHB	VQFN	32	3000	14 x 35	150	315	135.9	7620	8.8	7.9	8.15

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

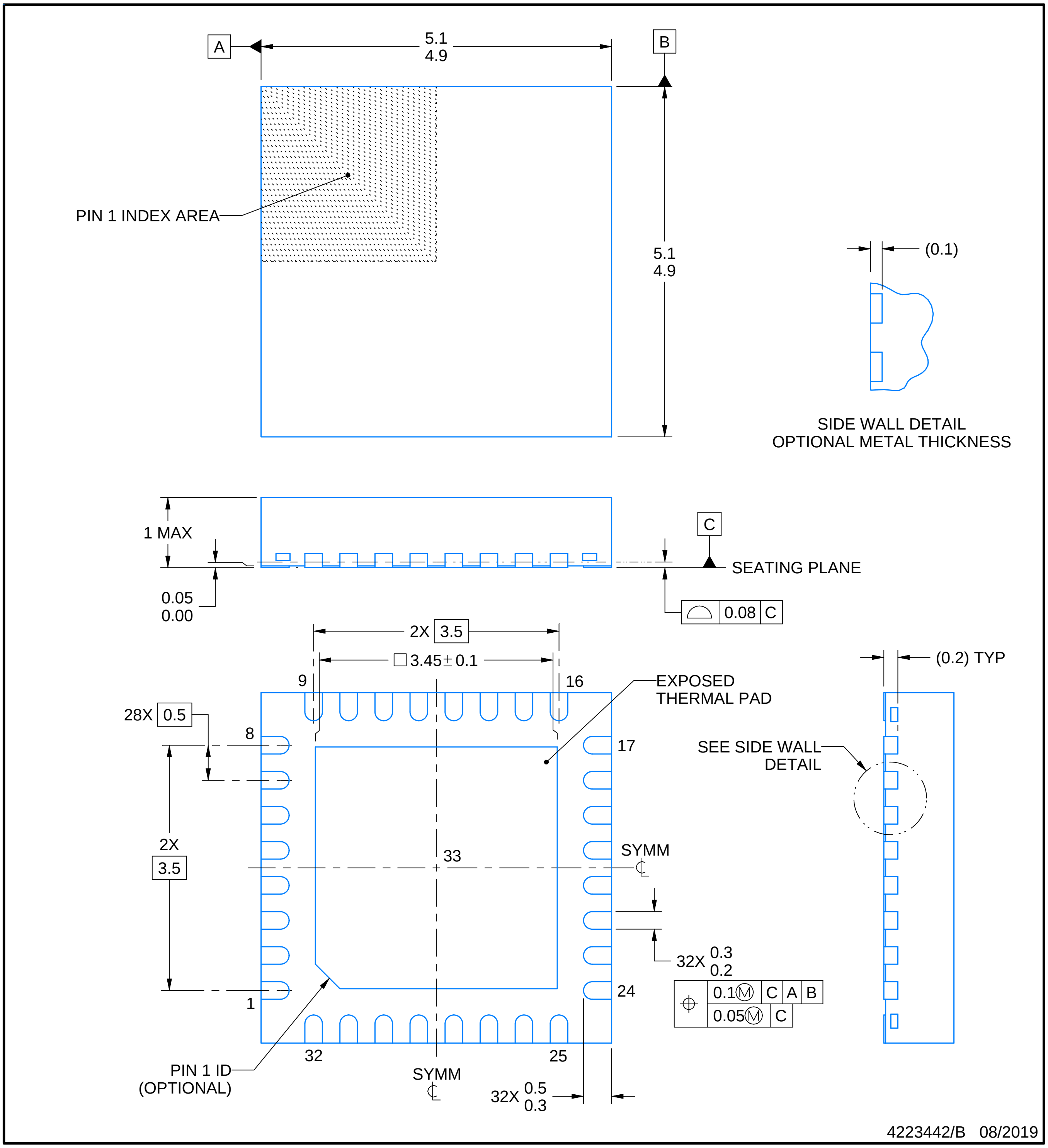
4224745/A

RHB0032E

PACKAGE OUTLINE

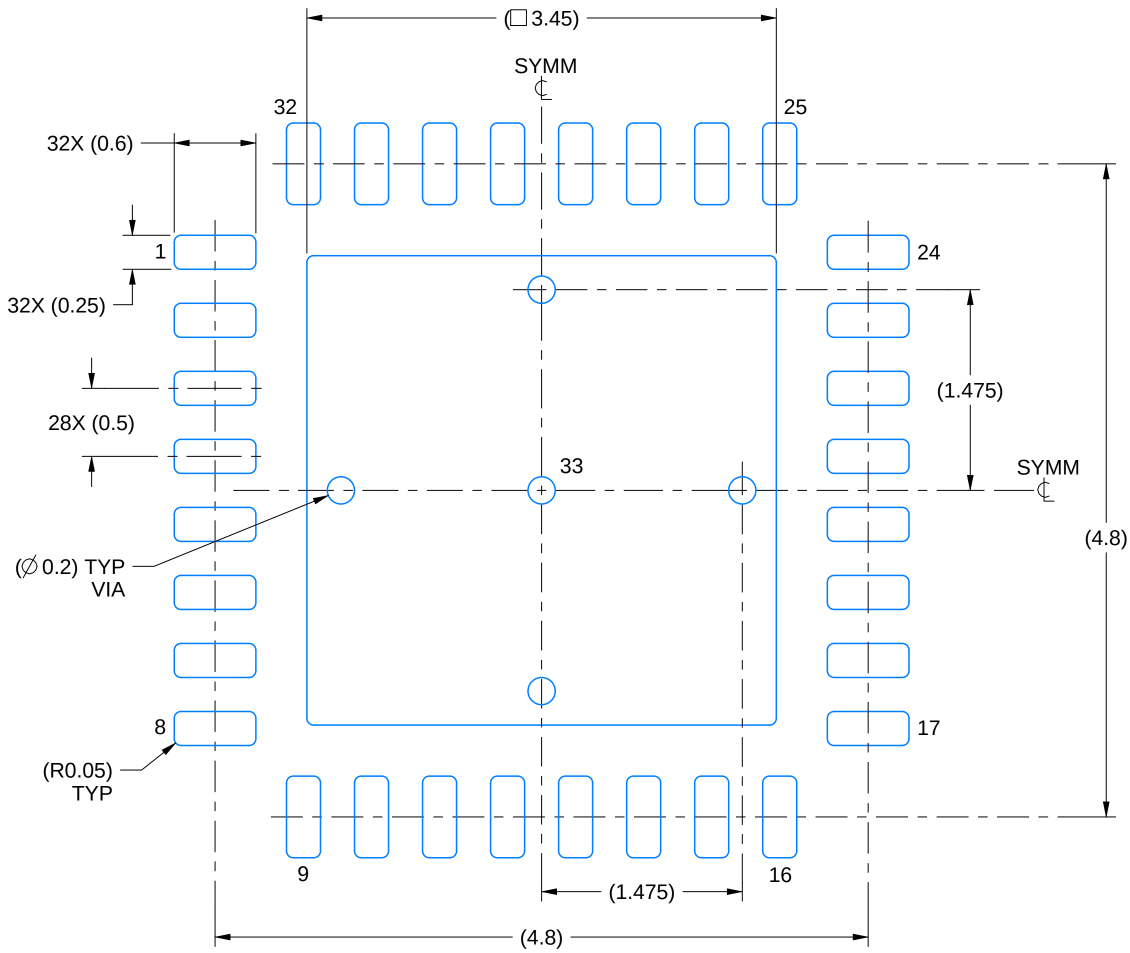
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

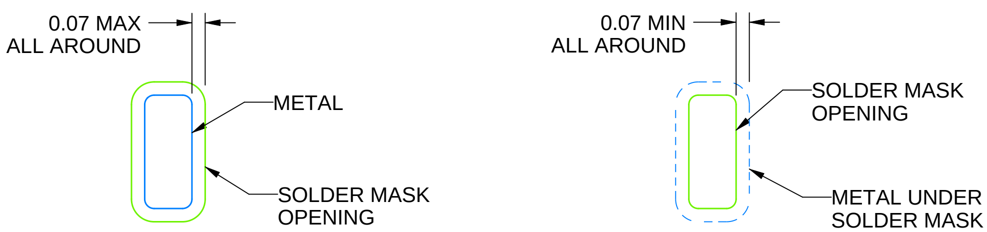


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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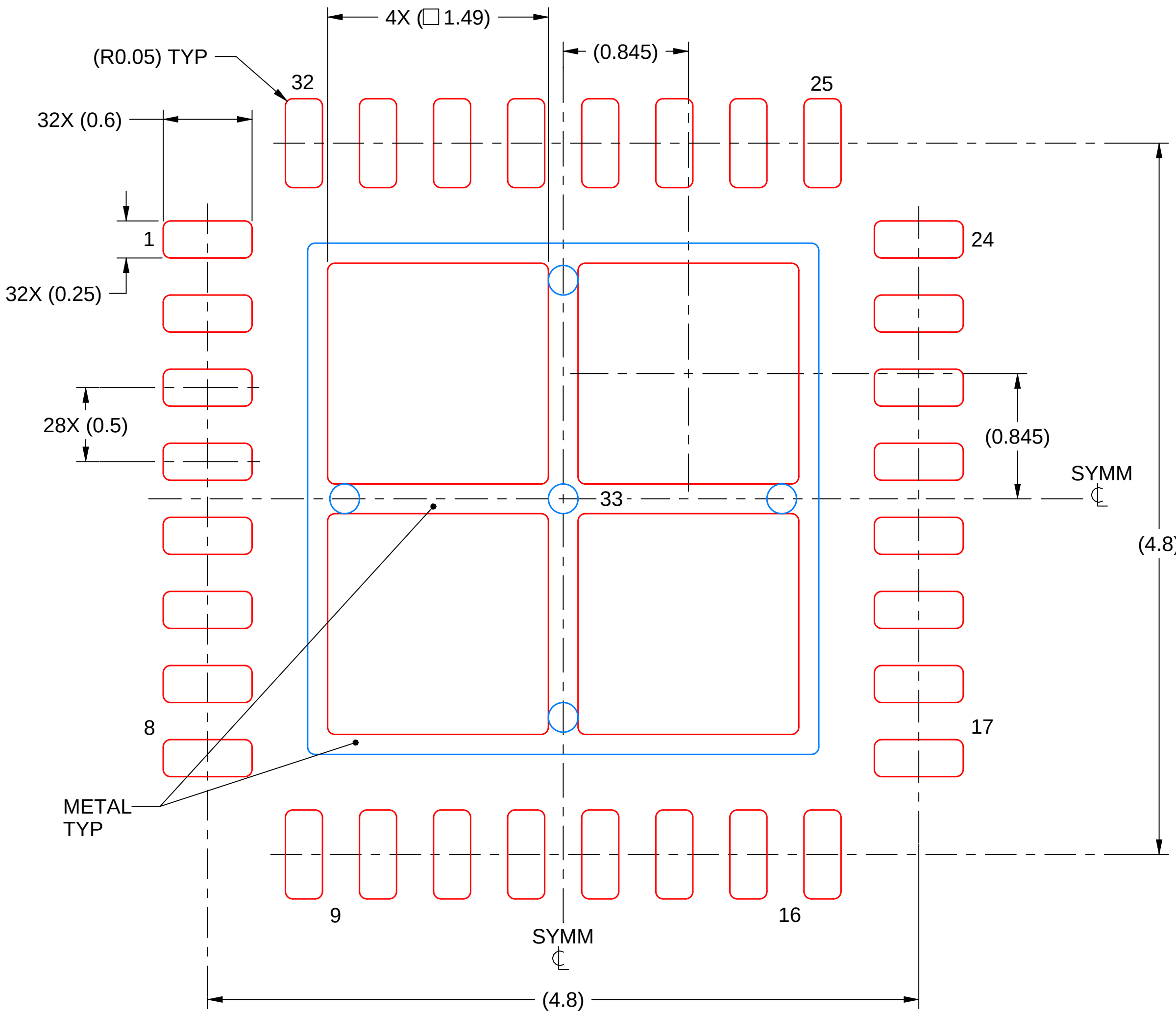
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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