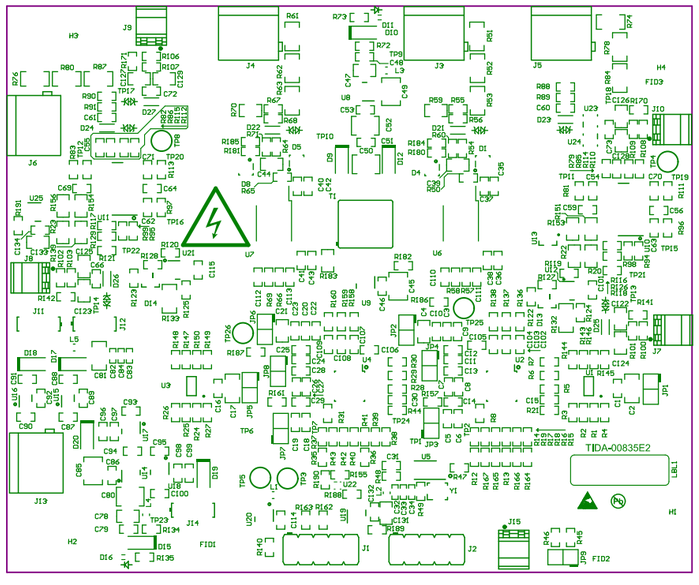
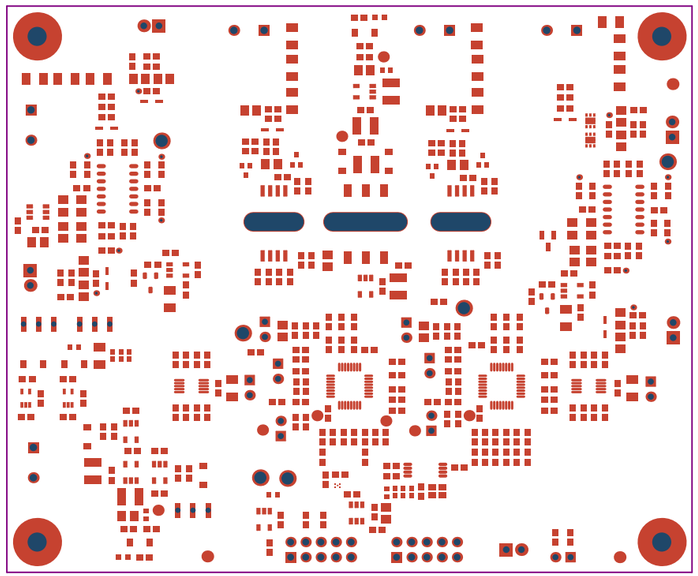
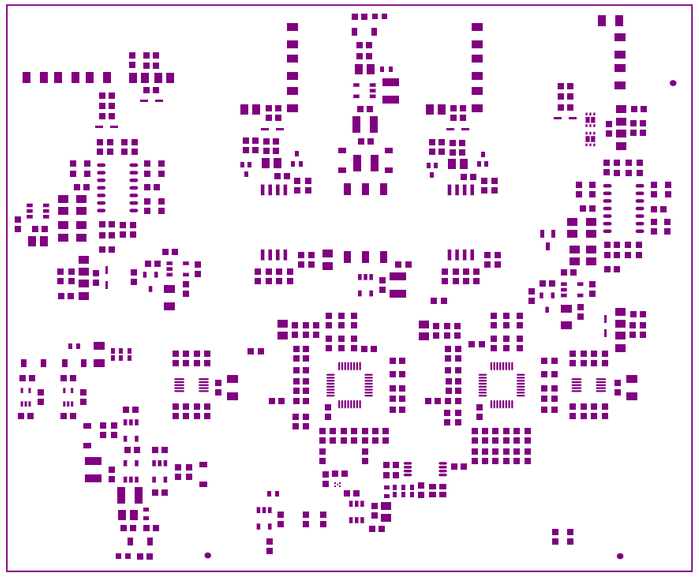


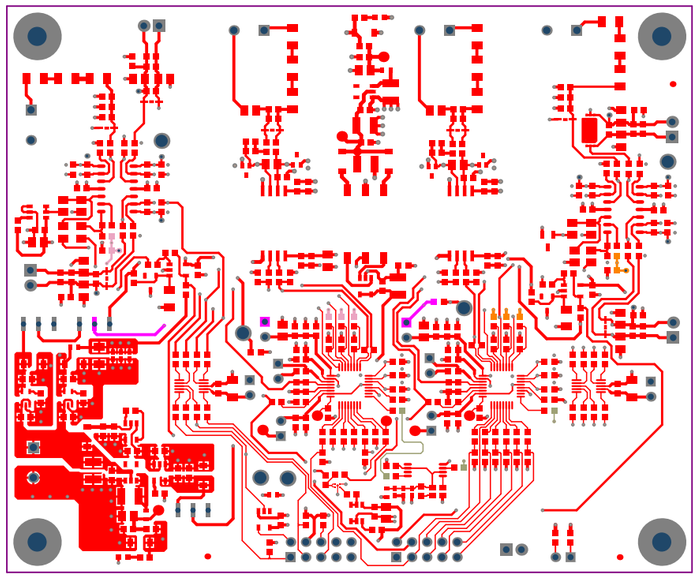
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Overlay	TID #: 00835		
PLOT NAME = Top Overlay	GENERATED : 7/24/2018 3:27:09 PM		TEXAS INSTRUMENTS



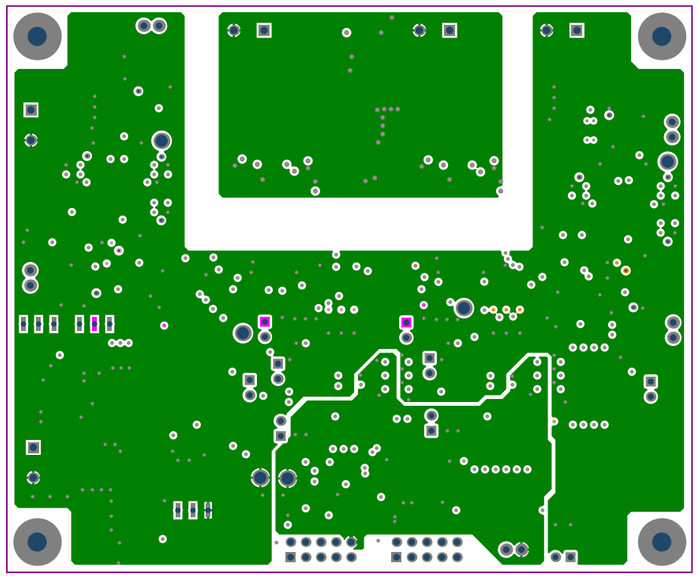
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Solder	TID #: 00835		
PLOT NAME = Top Solder Mask	GENERATED : 7/24/2018 3:27:10 PM		TEXAS INSTRUMENTS



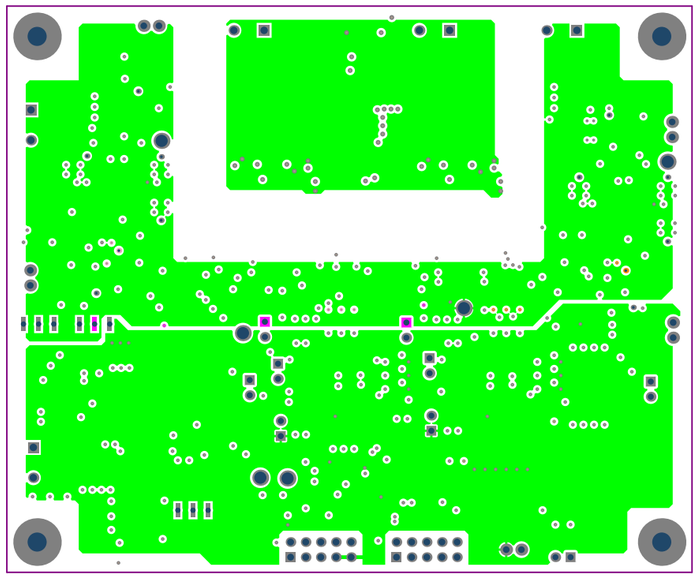
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Paste	TID #: 00835		
PLOT NAME = Top Paste	GENERATED : 7/24/2018 3:27:10 PM		TEXAS INSTRUMENTS



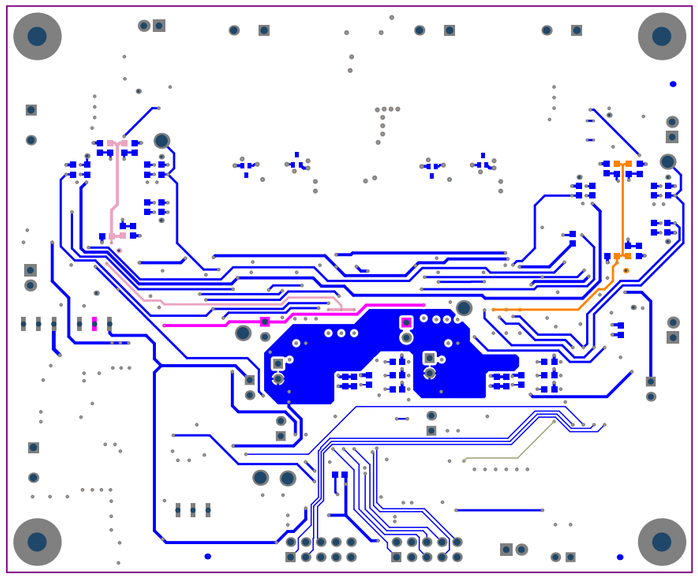
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Top Layer	TID #: 00835		
PLOT NAME = Top Layer	GENERATED : 7/24/2018 3:27:10 PM		TEXAS INSTRUMENTS



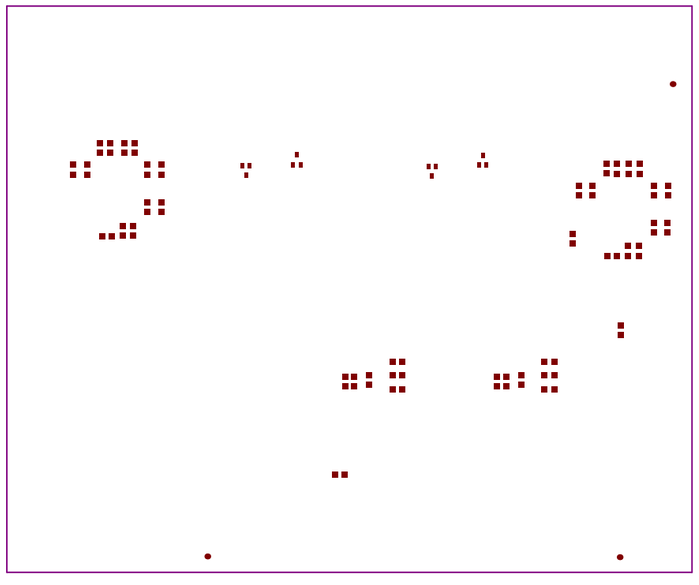
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = GND	TID #: 00835		
PLOT NAME = Signal Layer 1	GENERATED : 7/24/2018 3:27:11 PM		TEXAS INSTRUMENTS



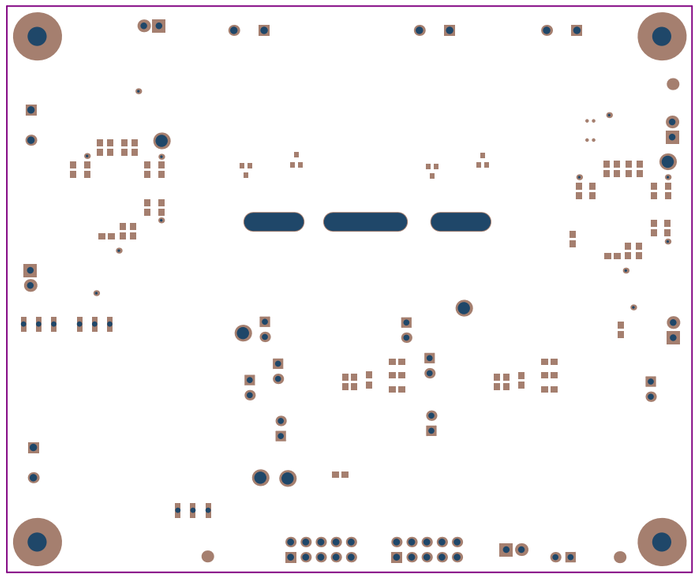
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = PWR	TID #: 00835		
PLOT NAME = Signal Layer 2	GENERATED : 7/24/2018 3:27:11 PM		TEXAS INSTRUMENTS



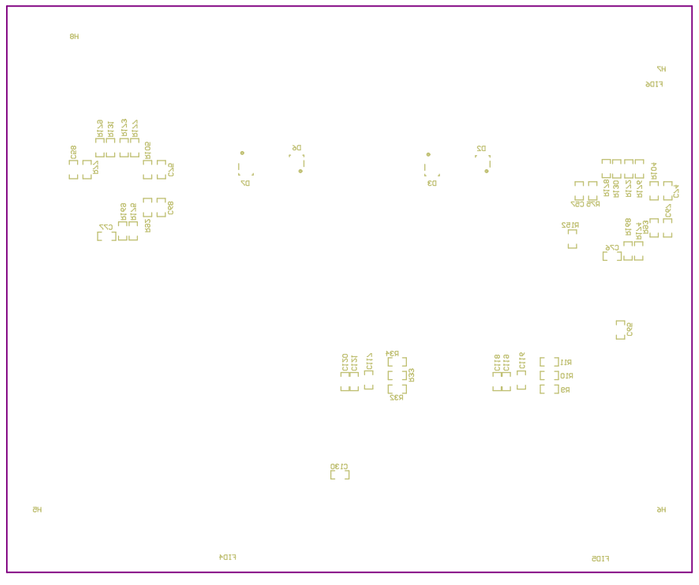
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Layer	TID #: 00835		
PLOT NAME = Bottom Layer	GENERATED : 7/24/2018 3:27:11 PM		TEXAS INSTRUMENTS



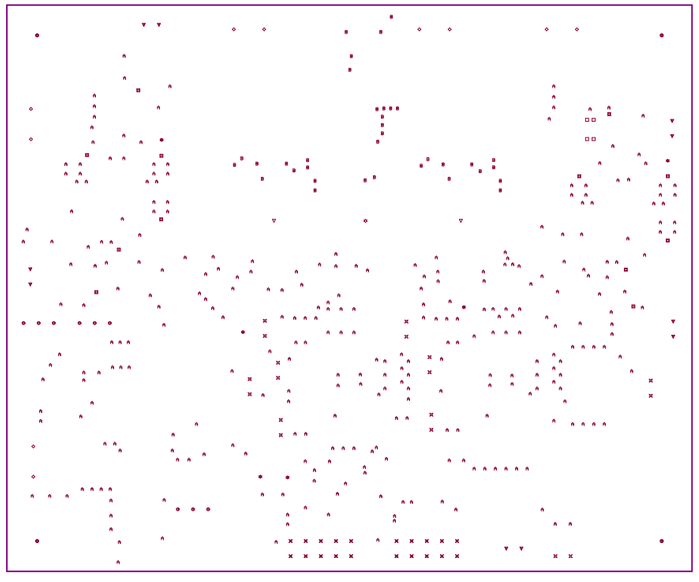
ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Paste	TID #: 00835		
PLOT NAME = Bottom Paste	GENERATED : 7/24/2018 3:27:11 PM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Solder	TID #: 00835		
PLOT NAME = Bottom Solder Mask	GENERATED : 7/24/2018 3:27:11 PM		TEXAS INSTRUMENTS



ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Bottom Overlay	TID #: 00835		
PLOT NAME = Bottom Overlay	GENERATED : 7/24/2018 3:27:11 PM		TEXAS INSTRUMENTS



Layer Stack Up Detail for: TIDA-00835-E2.Pcbdoc

Layer Name	Gerber Document	Copper Thickness	Dielectric Material
Top Solder Mask	(.GTS)		Solder Resist
Top Layer	(.GTL)	1.4mil	FR4-High Tg
GND	(.G1)	1.4mil	FR4-High Tg
PWR	(.G2)	1.4mil	FR4-High Tg
Bottom Layer	(.GBL)	1.4mil	FR4-High Tg
Bottom Solder Mask	(.GBS)		Solder Resist

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
115 MM X 95 MM

Number of Layers : 4
MIN. TRACK WIDTH: 6 MIL
MIN. CLEARANCE: 6 MIL
MIN. VIA DRILL SIZE: 12 MIL

MINIMUM ANNULAR RING 6 MIL (0.1524 mm) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 63 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
COPPER THICKNESS (FINISHED):
OUTER: [X] 1.4MIL (1oz) [ ] 2MIL (1.4oz) [ ] 2.8MIL (2oz)
INNER SIGNAL: [X] 1.4MIL (1oz) [ ] 2.8MIL (2oz) [ ] N/A
DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR:
[X] GREEN [ ] BLUE [ ] OTHER
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER
ARRAY/PANEL: [ ] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS --> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
ADDITIONAL REQUIREMENTS: VIA TENTING: YES [X] NO [ ]
MICROSECTION: [ ] YES IMPEDANCE CONTROL: YES [ ] NO [X]
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK

Drill Table

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Length	Routed Path Length
□	4	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	-	-
A	307	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	-	-
B	35	16.00mil (0.406mm)	PTH	Round	Top Layer - Bottom Layer	-	-
◘	12	17.72mil (0.450mm)	PTH	Round	Top Layer - Bottom Layer	-	-
⊙	9	35.04mil (0.890mm)	PTH	Round	Top Layer - Bottom Layer	-	-
⌑	18	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	-	-
▽	10	44.00mil (1.118mm)	PTH	Round	Top Layer - Bottom Layer	-	-
✖	20	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	-	-
◇	10	49.21mil (1.250mm)	PTH	Round	Top Layer - Bottom Layer	-	-
✿	6	80.71mil (2.050mm)	PTH	Round	Top Layer - Bottom Layer	-	-
✚	4	125.98mil (3.200mm)	PTH	Round	Top Layer - Bottom Layer	-	-
▽	2	120.00mil (3.048mm)	NPTH	Slot	Top Layer - Bottom Layer	394.00mil (10.008mm)	274.00mil (6.960mm)
✿	1	120.00mil (3.048mm)	NPTH	Slot	Top Layer - Bottom Layer	550.00mil (13.970mm)	430.00mil (10.922mm)
	438 Total						

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

FOR 12MIL DRILL +0/-12MIL
FOR PTH DRILL +/-3MIL
FOR NPTH DRILL +/-2MIL
FOR 16MIL DRILL +0/-16MIL

TEXAS INSTRUMENTS

PROJECT TITLE: ADS131 A04_AFE
DESIGNED FOR: Public Release
FILE NAME: TIDA-00835-E2.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = Drill Drawing	TID #: 00835		
PLOT NAME = Drill Drawing	GENERATED : 7/24/2018 3:27:12 PM	TEXAS INSTRUMENTS	

ENGINEER:	LAYOUT BY:
Sreenivasa	Avinash N
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.1.9.221

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: TIDA-00835	REV: E2	SVN REV: Not In VersionControl
LAYER NAME =	TID #: 00835		
PLOT NAME = Board Dimensions	GENERATED : 7/24/2018 3:27:13 PM		TEXAS INSTRUMENTS

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265