Application Report
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Minimizing Output Ripple During Startup

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ABSTRACT

A buck DC/DC switching converter has a minimum on-time at which it can operate. This limits the minimum output voltage a converter can regulate to while keeping a fixed frequency. The limitation of the minimum on-time is often only considered for the steady-state output voltage; however, when the output voltage ramps up, in most cases the output voltage ramps up from 0 V. When the converter tries to regulate to a voltage below the minimum set by the minimum on-time, many converters will pulse-skip to keep the output voltage regulated. Pulse-skipping results in a larger than usual output ripple and this can reduce how monotonic the output voltage ramp is. This application note uses the TPS54620 as an example to provide recommendations to reduce the ripple caused by pulse-skipping during startup and shows some newer parts which use different circuits during startup to reduce the output voltage ripple.

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1 Introduction

The TPS54620 is a peak current-mode control converter. For a peak current-mode control converter, the minimum on-time is set predominately by leading-edge blanking time and other internal circuit propagation delays in turning off the high-side MOSFET. For the TPS54620, during startup, the error amplifier compares the VSENSE pin to the SS/TR pin creating the control voltage at the COMP pin. The TPS54620 ramps up the output voltage by outputting a constant current from the SS/TR pin to charge up an external capacitor placed on this pin to ground. The COMP pin voltage sets the peak current output by the high-side MOSFET.

Figure 1 shows the output voltage for a standard TPS54620EVM-374 during startup. Only some noise at the beginning of the output voltage ramp can be seen here. Figure 2 shows the same waveform but with a smaller voltage scale and timescale to better see the ripple behavior at the beginning of the output voltage ramp. To judge how monotonic the output voltage ramp is, the *magnitude* of the drop in the output voltage when pulse-skipping will be used. In this waveform the magnitude of the largest drop in the output voltage is approximately 100 mV. Once the output voltage is above the minimum output voltage supported by the minimum on-time, the TPS54620 stops pulse-skipping and the output ripple is reduced. The output voltage where pulse-skipping stops and the output voltage ramp smooths out can be estimated using Equation 1.

Newer parts in the same family as the TPS54620 have an added feature to reduce the ripple during startup. See Section 4 for more details.

$$V_O = t_{ON_MIN} \times V_I \times f_{SW} \quad (1)$$

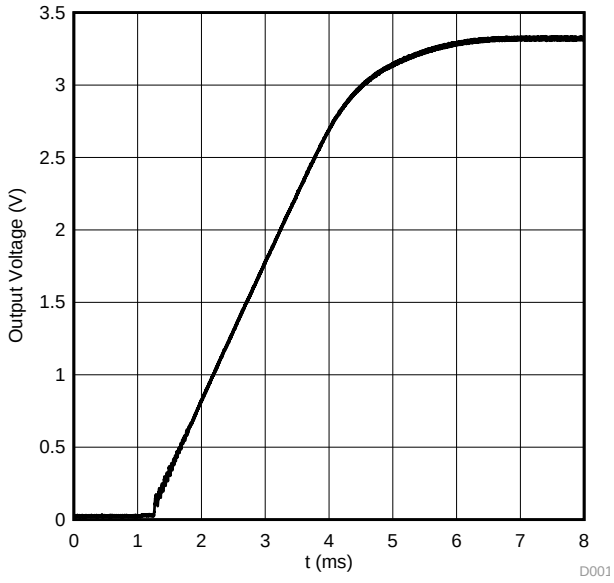

Figure 1. Full Output Voltage Ramp

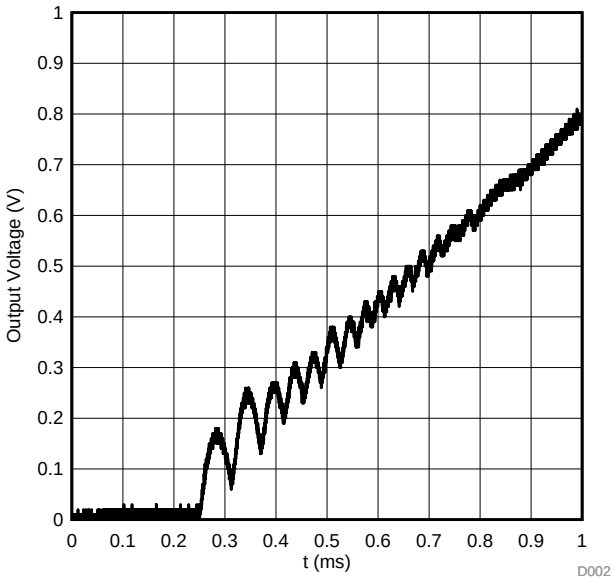

Figure 2. Beginning of Output Voltage Ramp

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Testing is done on the TPS54620EVM-374. The schematic is shown in Figure 3 and more details are found in the TPS54620EVM-374 user's guide (SLVU281).

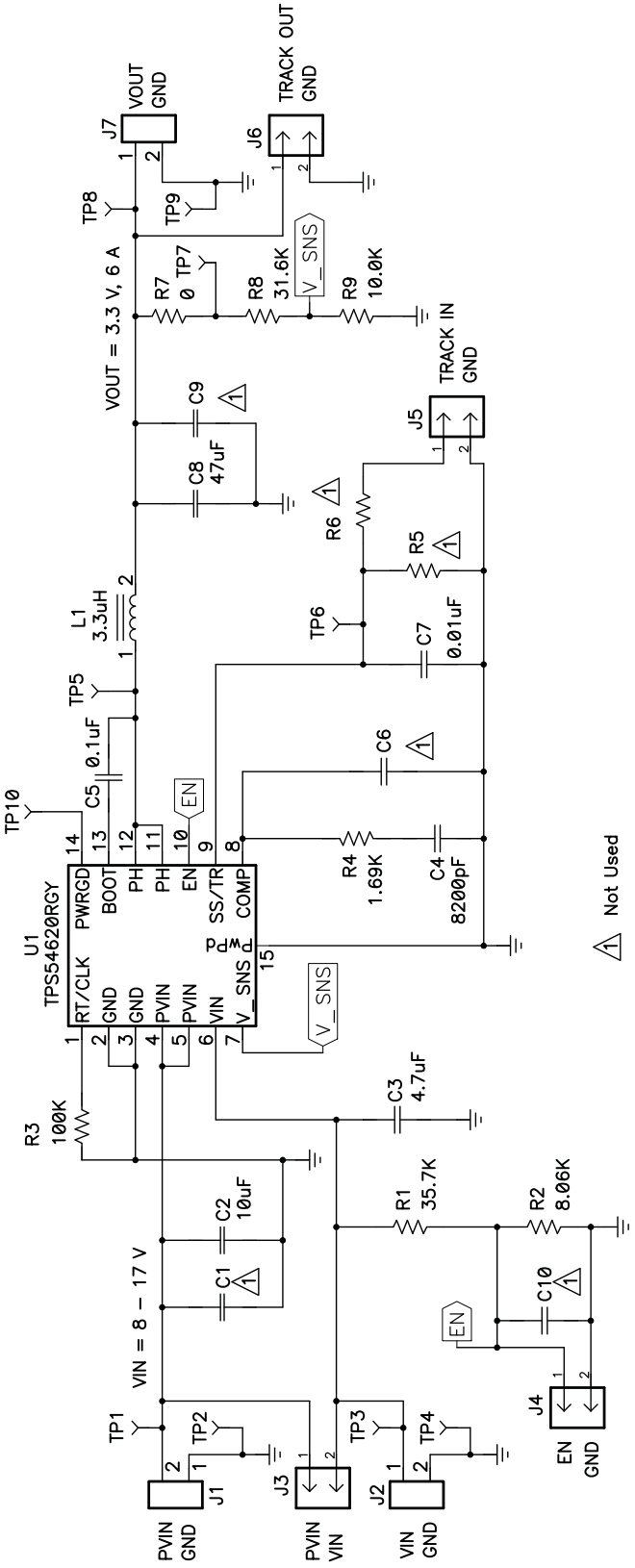

Figure 3. TPS54620EVM-374 Schematic

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2 Source of Output Ripple During Startup

Figure 4 shows the startup waveforms at the PH, COMP, VSENSE and SS/TR pins. In this figure the PH pin scale is 24 V per division and the scales of the remaining waveforms are 1 V per division. There is an internal offset between SS/TR and the regulated VSENSE voltage. In Figure 4 the 29-mV typical offset was subtracted from the measured SS/TR pin voltage. Lastly, for this measurement, C6 was populated with a 100-pF capacitor to minimize noise picked up on the COMP pin when probing it.

The TPS54620 starts up and begins switching as follows. First the SS/TR pin voltage begins to ramp up causing a difference in voltage between the SS/TR pin and VSENSE pin. The COMP pin ramps up in response to this voltage difference. The TPS54620 does not begin switching until the COMP voltage rises above the switching threshold. When switching starts, minimum on-time high-side MOSFET pulses are output from the switching node (PH pin). When the output voltage is very low, the minimum on-time pulses overcharge the output voltage causing the VSENSE pin voltage to exceed the SS/TR voltage. In response to this voltage difference, the COMP pin voltage discharges. When the COMP voltage falls below the switching threshold, the high-side MOSFET stops switching and the low-side MOSFET remains on.

While the low-side MOSFET is on the output voltage is discharged through it. When the output voltage is discharged low enough to bring the VSENSE pin voltage below the SS/TR voltage, the loop begins to respond by charging up the COMP voltage. When the COMP voltage exceeds the switching threshold, the high-side MOSFET begins switching again with the minimum on-time. This cycle repeats until the output voltage ramps above the minimum output voltage to which the IC can regulate without pulse-skipping.

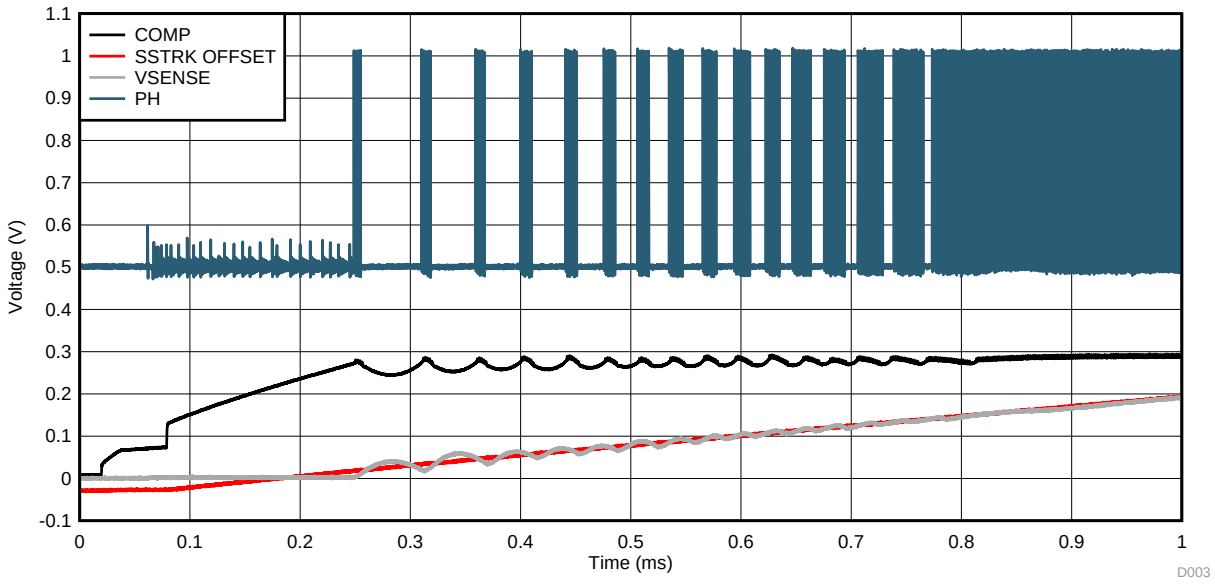

Figure 4. PH, COMP, VSENSE and SS/TR During Startup

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3 Reducing the Startup Ripple

3.1 Influence of Standard Compensation

The response of the COMP voltage to the differences between the VSENSE voltage and SS/TR depends on the loop response. Maximizing the loop crossover frequency (f_{CO}) of the design can improve the transient response and reduce the output voltage ripple during startup. The TPS54620 EVM loop is already well optimized so the effects of the compensation on the startup ripple is shown in two steps. First, to show the effect of C4 value, it is increased from 6800 pF to 15 nF, and the results are shown in Figure 5. Increasing the value of C4 reduced the largest drop in the output voltage due to pulse-skipping to approximately 70 mV. It also reduced the ripple throughout the entire startup ramp. Increasing C4 helps because it increases the RC time constant on the COMP voltage.

To show the effect of R4, it is decreased to 2.80 kΩ while keeping C4 fixed at 15 nF. Decreasing R4 reduces the gain in the compensation which also reduces the f_{CO} and slows down the transient response. The resulting waveform is shown in Figure 5. Reducing the value of R4 had almost no effect on the largest output voltage drop due to pulse-skipping but the ripple throughout the entire startup ramp is increased.

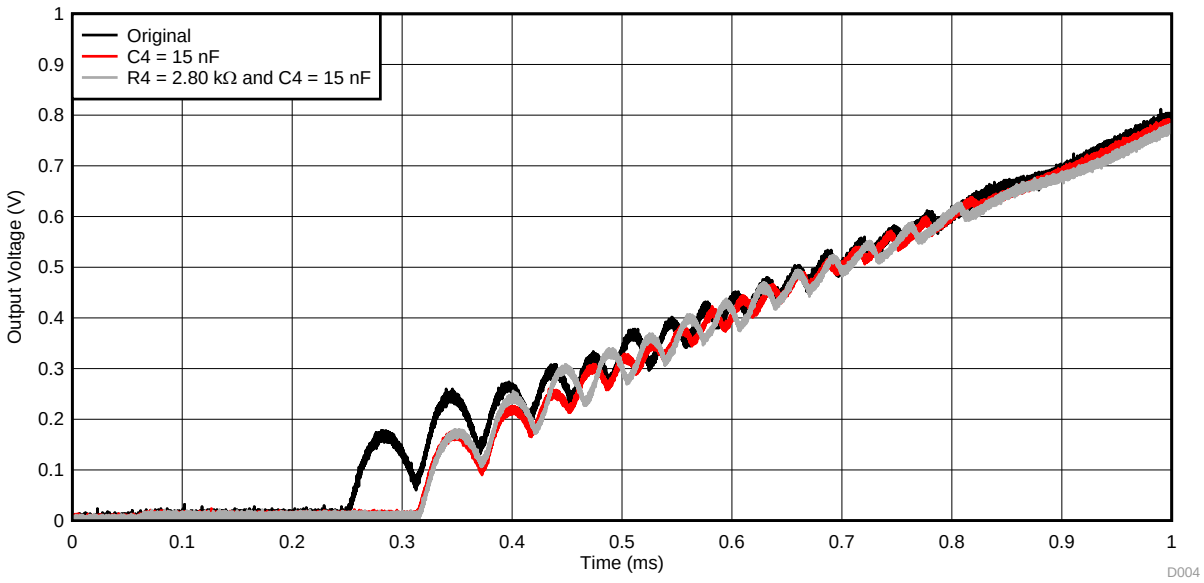

Figure 5. Startup with Different Compensation

Increasing both C4 and R4 is effective at reducing the output ripple during startup. However, there is a limit to how large both of these components can be. Increasing C4 may slow down the transient response because of the increased RC time constant for the COMP pin voltage. The error amplifier of the TPS54620 must charge and discharge this capacitor when a load step occurs. The error amplifier has a typical source and sink current of 110 µA to charge and discharge this capacitor. For the fastest transient response, the smallest value of C4 is preferred. The maximum value of R4 is limited by the phase in the loop. Increasing R4 results in higher crossover frequency and can cause the phase margin to decrease. Keeping a stable design sets the limit to the maximum value of R4 and the recommended phase margin target is 60 degrees.

The preferred and most accurate method to optimize these values is to use measurements in the final design. Real measurements are preferred because this includes behaviors that show up in a real circuit. Specifically, an important effect which should always be included is the derating of the capacitance of any ceramic output capacitors. Using a PSPICE or TINA average simulation or WEBENCH® is the next best alternative.

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3.2 Adding a Feed-Forward Capacitor

Adding a feed-forward capacitor in parallel with the upper resistor in the VSENSE pin resistor divider can help reduce the output voltage ripple during startup. The feed-forward capacitor passes any AC voltage on the output directly to the VSENSE pin. Without it, the AC voltage on the output is divided down by the resistor divider. Passing AC voltage directly to the VSENSE pin allows the control loop to see and respond more quickly to changes in the output voltage. For this example, the added feed-forward capacitor is selected to place a zero at 1.5× the EVM f_{CO} of approximately 45 kHz. The zero was placed at a higher frequency than the f_{CO} to keep the f_{CO} the same. Equation 2 shows the calculation of this capacitor value. A standard value of 68 pF was used. Figure 6 shows the change in startup ripple with the added feed-forward capacitor. With the added C_{FF} the drop in the output voltage due to pulse-skipping was reduced to 50 mV.

$$C_{FF} = \frac{1}{3 \times \pi \times f_{CO} \times R8} \quad (2)$$

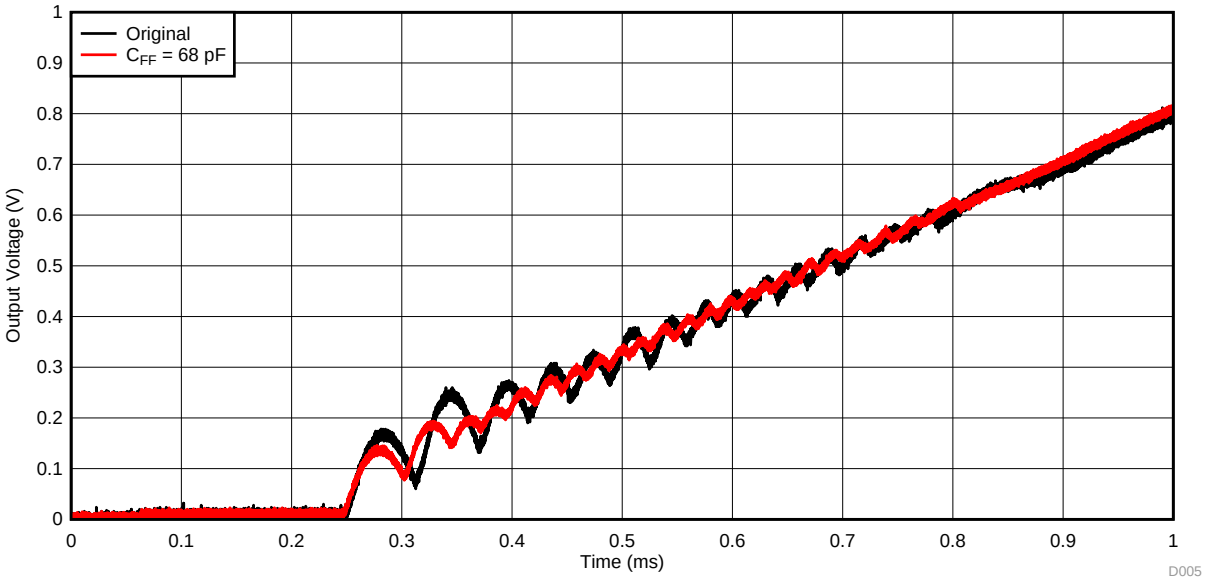

Figure 6. Startup with C_{FF}

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3.3 Influence of the LC Filter

3.3.1 Inductor

Changing the inductance of the output inductor from the original 3.3 µH can also influence the startup ripple. The inductance was decreased to 2.4 µH and increased to 4.2 µH to test its influence. Figure 7 shows the resulting waveforms.

Both increasing and decreasing the inductance reduced the drop in the output voltage while pulse-skipping in this example. A larger inductance can help because it reduces the peak-to-peak ripple current which translates to lower output voltage ripple. With a larger inductance, the drop in the output voltage due to pulse-skipping was reduced to 60 mV. A smaller inductance can help because with a smaller inductance the current can ramp more quickly, improving the transient response. With a smaller inductance, the drop in the output voltage due to pulse-skipping was reduced to 80 mV. Additionally, with a smaller inductance the frequency of the ripple on the output voltage was increased as a result of the higher inductor current ramp rate.

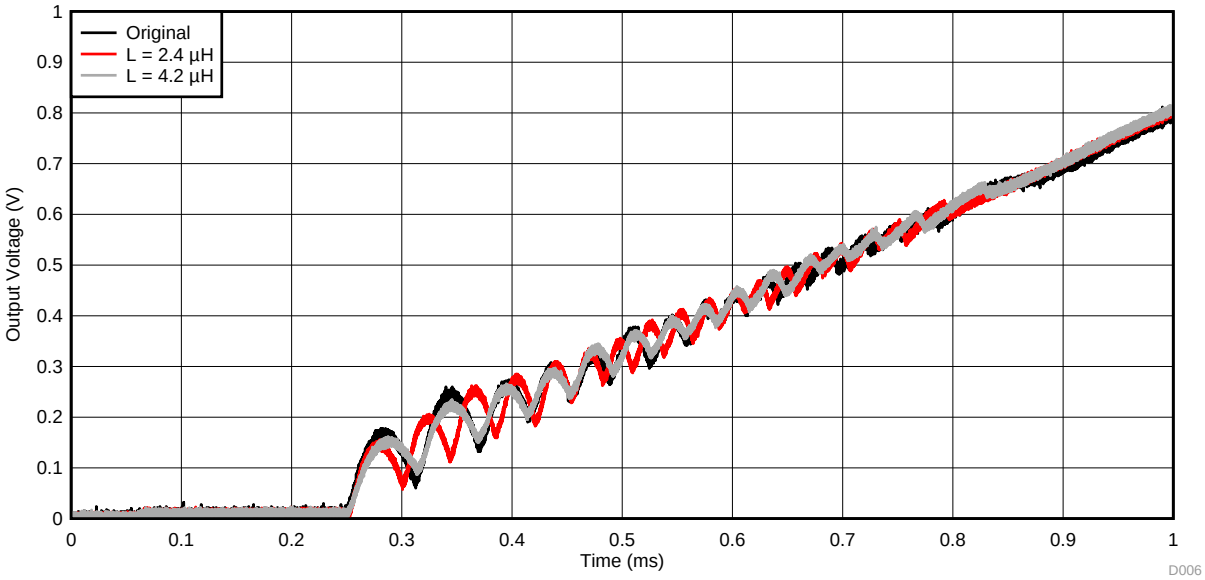

Figure 7. Startup With Different L Values

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3.3.2 Output Capacitor

Increasing the output capacitance will decrease the amount of ripple on the output. The output capacitance was increased from 200 µF to 300 µF. Figure 8 shows the resulting startup. The drop in the output voltage when pulse-skipping is reduced to 60 mV.

When the output capacitance is changed, the compensation is no longer fully optimized. Additional output capacitance moves the pole created by the output capacitor and load resistance to a lower frequency. This decreases the gain in the loop and decreases the f_{CO}. To have the same f_{CO}, the gain of the compensation should be increased by the same amount the lower frequency pole decreased it. The compensation can very simply be re-optimized by increasing the value of R4 by the same factor that the output capacitance was increased. R4 was increased by a factor of 3 / 2 to 8.45 kΩ and the startup was tested again. The largest drop in output voltage when pulse-skipping remained the same at 60 mV but the magnitude of the ripple decreased more quickly.

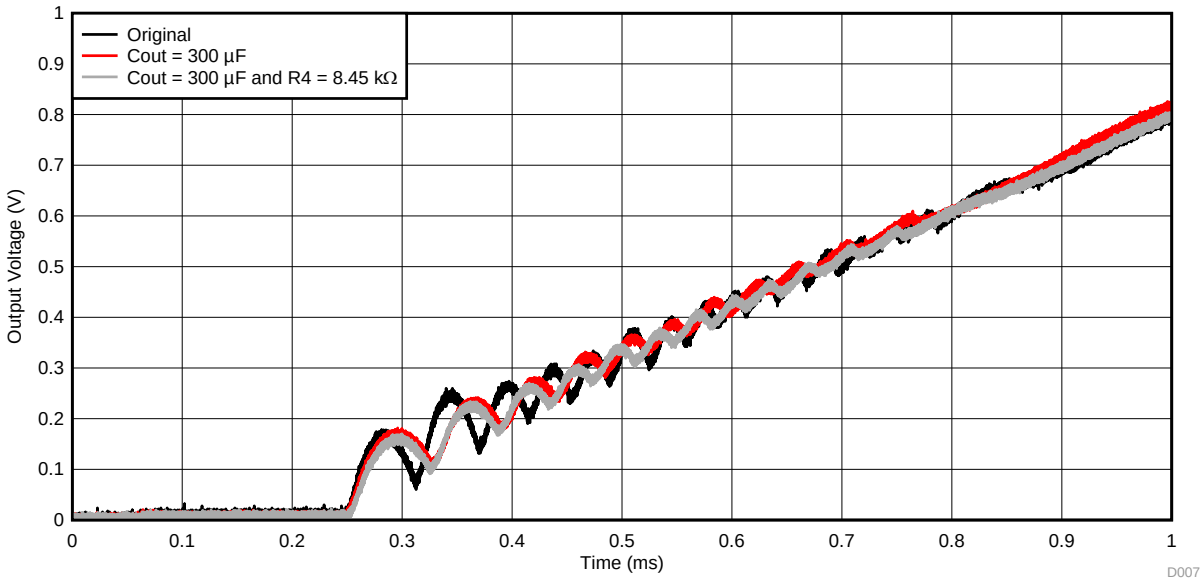

Figure 8. Startup with Added Output Capacitance

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3.4 Influence of the Switching Frequency (f_{sw})

The root source of the output ripple during startup is pulse-skipping due to the minimum on-time. Decreasing the f_{SW} can help to reduce the ripple because it will increase the operating on-time for the same output voltage. Figure 9 shows the startup with the f_{SW} reduced to 400 kHz. The largest drop in the output voltage due to pulse-skipping was reduced to 70 mV.

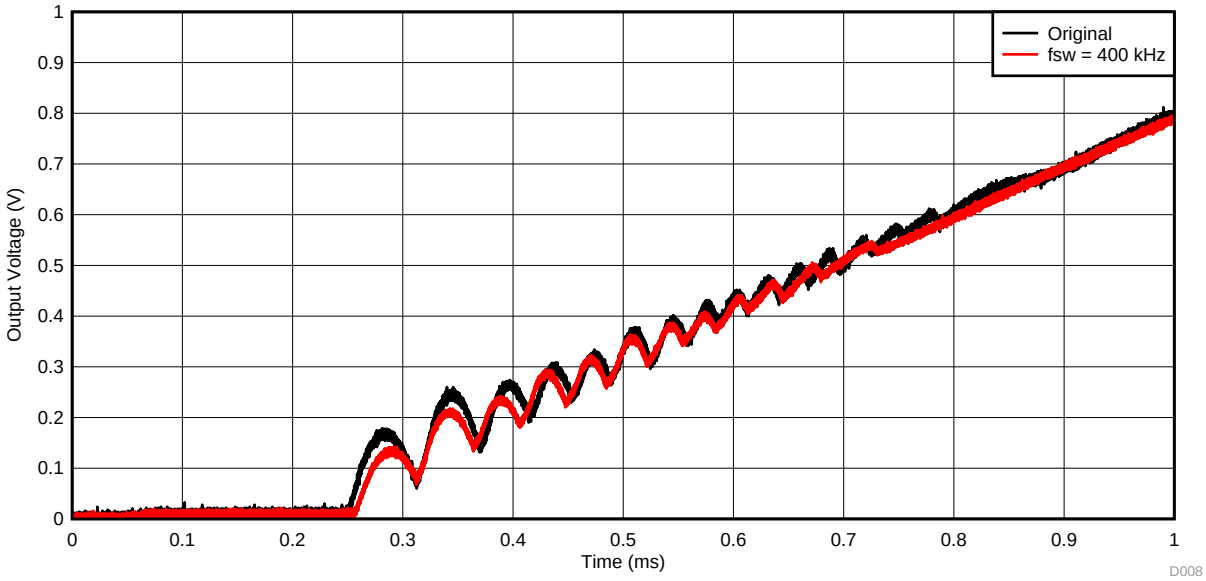

Figure 9. Startup with Lower f_{SW}

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4 Parts with Improved Startup

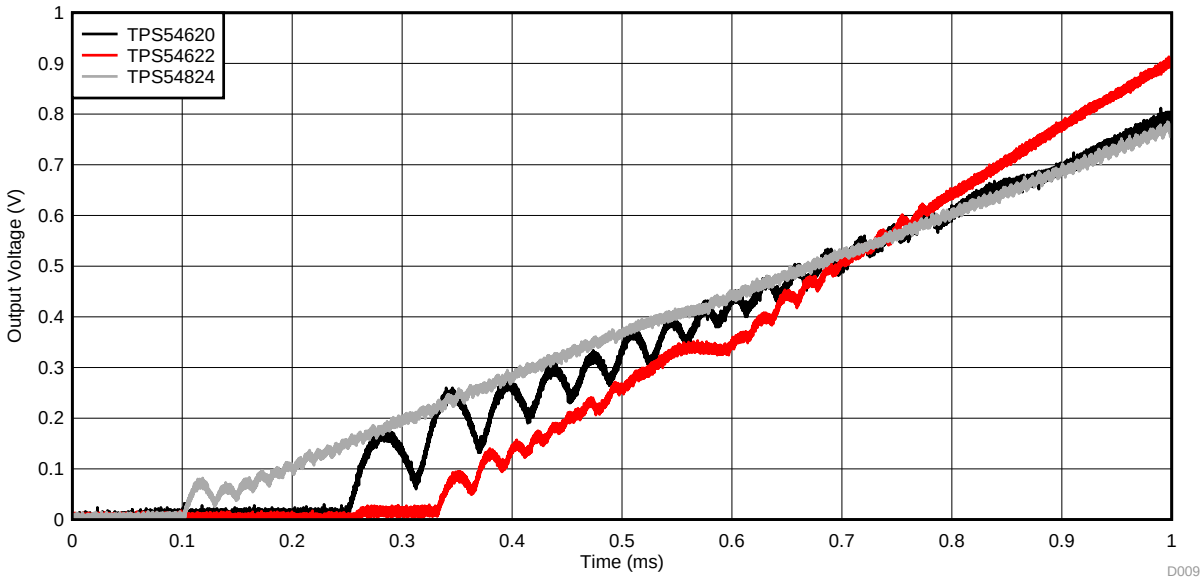

Figure 10. Improved Startup in Newer Parts

Newer parts from the same family as the TPS54620 have an additional circuit to minimize ripple during startup. This circuit is active during startup only. This circuit works by adding a quicker path to enter pulse-skip mode. This fast path compares the VSENSE voltage to the SS voltage at the beginning of each switching cycle to determine if the IC should skip a pulse or not. This fast skip path overrides the minimum COMP voltage switching threshold so the IC does not need to wait for the loop to respond to enter pulse-skipping mode. As a result, overshoot is minimized while switching at the minimum on-time.

Parts in the same family as the TPS54620 that include this feature are the TPS54424, TPS54622, TPS54623, TPS54824, and TPS54020. Table 1 gives more details on these parts. Figure 10 shows the improved startup of the TPS54622 EVM compared to the TPS54620 EVM. The TPS54622 EVM has almost no ripple during startup with half the output capacitance. Figure 10 also shows the startup of the TPS54824 EVM, the latest addition to this family of buck regulators.

Table 1. Parts with Improved Startup Feature

Part Number	Output Current (A)	Package Size and Type	Description	Datasheet Link
TPS54424	4	3.5 mm x 3.5 mm VQFN-HR (18)	High efficiency HotRod™ package.	TPS54424
TPS54622	6	3.5 mm x 3.5 mm VQFN (14)	Pin to pin with the TPS54620. 0.6 V internal reference.	TPS54622
TPS54623	6	3.5 mm x 3.5 mm VQFN (14)	Pin to pin with the TPS54620. 0.6 V internal reference and diode emulation at light load.	TPS54623
TPS54824	8	3.5 mm x 3.5 mm VQFN-HR (18)	High efficiency HotRod™ package.	TPS54824
TPS54020	10	3.5 mm x 3.5 mm VQFN-HR (15)	High efficiency HotRod™ package. Diode emulation at light load. Selectable current limit.	TPS54020

Another feature which can reduce the ripple during startup is frequency foldback, depending on how it is implemented. This feature is mainly intended for short-circuit protection but also helps reduce ripple during startup because the switching frequency is reduced in certain scenarios. In many parts, this feature works by reducing the switching frequency based on the VSENSE or FB voltage. At lower VSENSE voltage, the switching frequency is lower and with lower switching frequency the on-time is increased. A higher on-time allows the part to operate away from its minimum on-time so it does not pulse-skip as much during startup and the ripple during startup is reduced. An example part with this feature is the TPS54618.

Lastly, parts with a constant on-time based loop control mode have very fast transient response and, as a result, have low ripple during startup. Example control modes with low ripple during startup include DCAP2™ and DCAP3™.

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5 Conclusion

If an existing design has large ripple during startup that needs to be reduced, the simplest changes to make are to ensure the compensation values are optimized and add a feed-forward capacitor if one is not currently being used. Changing the inductance, adding output capacitance or reducing the f_{SW} can also be considered but these may result in a more significant change in the design. For new designs, the ripple during startup can be minimized as much as possible by using one of the parts with improved startup behavior.

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